MicDAT 2018

Microelectronic Devices and Technologies:

Proceedings of the 1st International Conference on Microelectronic Devices and Technologies (MicDAT '2018)

20-22 June 2018

Castelldefels, Barcelona,
Spain

Edited by Sergey Y. Yurish



IFSA

Sergey Y. Yurish, *Editor*
Microelectronic Devices and Technologies
MicDAT '2018 Conference Proceedings

Copyright © 2018
by International Frequency Sensor Association (IFSA) Publishing, S. L.

E-mail (for orders and customer service enquires): ifsa.books@sensorsportal.com

Visit our Home Page on http://www.sensorsportal.com

All rights reserved. This work may not be translated or copied in whole or in part without the written permission of the publisher (IFSA Publishing, S. L., Barcelona, Spain).

Neither the authors nor International Frequency Sensor Association Publishing accept any responsibility or liability for loss or damage occasioned to any person or property through using the material, instructions, methods or ideas contained herein, or acting or refraining from acting as a result of such use.

The use in this publication of trade names, trademarks, service marks, and similar terms, even if they are not identifies as such, is not to be taken as an expression of opinion as to whether or not they are subject to proprietary rights.

ISBN: 978-84-09-03153-5

Contents

Foreword **6**

A Ku-Band Power Amplifier Using Differential Transmission-Line Transformer in 0.25-μm GaN **7**
Hwann-Kaeo Chiou, and Kai-Yen Chang7

High Gain, High Bandwidth Fully Differential Operational Amplifier Design Using Self-Cascode MOSFET with Adaptive Bias and Common Mode Feedback **11**
Anu Gupta, Kalpraj Vaidya 11

The Algorithm and Software Implementation of the Thermal Transient Testing Technology Applied in High-Power Electronics **18**
Erping Deng, Yaru Shen, Zhibin Zhao, Jinyuan Li and Yongzhang Huang 18

Investigation on Multilayer Conductor Interconnects of Integrated Circuits Using Finite Element Method **23**
L. Belhimer, A. Benfdila and A. Lakhlef23

Simultaneous Read/Write Nanoelectronic SRAM with Shared Write Bit-Line Scheme **28**
B. O. Câmara, J. G. Guimarães and J. C. da Costa 28

Modeling GaAs MESFET's Using Finite Elements Method **32**
M. Djouder, A.Benfdila and A.Lakhlef 32

Increasing the Dielectric Constant of HfO_2 in MIS Structures, by Thermal Annealing Right after Deposition of the Dielectric Layer **36**
I. S. Hernández, S. I. Garduño, and M. Estrada36

Study and Simulation of Degradation of MOS Transistor Using Silvaco Athena and Matlab **39**
N. Guenifi, R. Mahamdi, T. Chenaf39

Investigation of Post-Implantation Annealing for Phosphorus-Implanted 4H-Silicon Carbide **42**
V. Šimonka, A. Hössinger, S. Selberherr, and J. Weinbub 42

TCAD Based Investigation of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) Transistor **45**
Vandana Kumari, Manoj Saxena and Mridula Gupta 45

Simplified Design of the Digital Control Logic for SAR ADC **50**
M. Borgarino, N. Verrascina and J.-B. Begueret 50

Non-Quasi-Static Large Signal Sub-Circuit Model of AlGaN/GaN HEMT **55**
Nebojsa Jankovic55

Power and Area Efficient Intelligent Hardware Design for Water Quality Applications **58**
Abheek Gupta, Anu Gupta, Rajiv Gupta 58

Investigation on Body Potential in Cylindrical Gate-All- Around MOSFET **62**
M. Kessi, A. Lakhelef, and A. Benfedila62

Simulation of Low-Temperature Crystallization in Germanium Thin Films 65
Y. Kogure, T. Funayama and Y. Uchida65

TCAD-RAD Subsystem for BJT/HBT and MOSFET Structures Simulation Taking into Account Radiation Effects 69
K. O. Petrosyants, M. V. Kozhukhov, D. A. Popov69

Monolithic III-V/CMOS Technology, Unified Device Compact Models and Hybrid Process Design Kit 75
X. Zhou and S. B. Chiah75

A Project-based Integrated Circuit Design and Characterization Course: A Case Study..... 78
A. Abusleme and M. Pérez-Sanagustín 78

Colossal Permittivity and Dielectric Relaxation in (Li, Al) Co-doped ZnO Ceramics 85
Dong Huang, Francis C. C. Ling85

Effect of Resistive Switching Cycling on the Physical Characteristics of Ni/HfO_2/n^+-Si RRAM Devices 86

Off-the-Shelf Implementation of a Memcapacitor Emulator Based on Voltage Amplifier with Flux-Controlled Gain 91
F. Romero, A. Medina, D. Gamez, A. Godoy, D. Morales, A. Ohata and N. Rodriguez 91

Investigation of the Changes in the Electronic Properties of Spray Deposited Zirconium Oxide Films as a Function of UV-Ozone Treatment..... 94
Abayomi. T Oluwabi, Ilona Oja-Acik, Atanas Katerski, Erki Kärber, Arvo Mere, Malle Krunks94

Design, Implementation and Performance Evaluation of Wireless Sensor Networks for Data Acquisition System (A Case Study of Smart Homes) 101
S. Abba and I. M. Nyam101

Fabrication and Characterization of SAW Resonators Based on Sputtered AlScN Thin Films with High Sc Content 108
A. Ding, M. Reusch, Y. Lu, N. Kurz, T. Christoph, V. Lebedev, L. Kirste, R. Driad, A. Žukauskaitė and O. Ambacher,108

140 mV-Startup Boost Converter for Thermal Energy Harvesting System..... 110
Hong-Yi Huang, Chun-Lian Chen, Jin-Sheng Chen, Chun Yi and Kuo-Hsing Cheng 110

Portable Continuous-Monitoring System Device for Monitoring the Microclimate in the Shoe-foot Interface 113
José de Jesús Sandoval-Palomares, Javier Yáñez-Mendiola, Alfonso Gómez-Espinosa and José Martin López-Vela 113

Microwave Tunable SIW Filter with Liquid Crystals..... 116
S. Missaoui, S. El Missaoui and M. Kaddour 116

A 16-Gbps Low-Power Transceiver for High-Speed Serial Links 120
Jongsun Kim and Jahyun Gu 120

Pt-functionalized AlGaN/GaN Heterojunction Hydrogen Gas Sensor for Extreme Environment Operation 123
Hyungtak Kim and Ho-Young Cha123

A PVT Insensitive Time to Digital Converter with Continuous Sampling 125
Hong-Yi Huang, Ping-Che Hsieh, Yung-Hsu Chen and Kuo-Hsing Cheng 125

GOx@ZIF-8(AuNPs): Synthesis and Application for Mediator Free Amperometric Glucose Sensor 128
Jibinlal A, Anirban Paul 128

Dynamic Threshold Compensated Organic Rectifier for RFID Applications 131
G. H. Ibrahim, U. Zschieschang, H. Klauk and L. Reindl 131

Foreword

On behalf of the MicDAT' 2018 Organizing Committee, I introduce with pleasure these proceedings devoted to contributions from the 1st International Conference on Microelectronic Devices and Technologies (MicDAT '2018) held in Barcelona, Castelldefels, Spain. The conference is organized by the International Frequency Sensor Association (IFSA) in technical cooperation with our sponsor Excelera, S.L. (Barcelona, Spain) and media partners: MDPI journals '*Micromachines*' and '*Sensors*' (Switzerland). The conference program provides an opportunity for researchers interested in microelectronics to discuss their latest results and exchange ideas on the new trends and challenges. The main objective of the MicDAT' 2018 conference is to encourage discussion on a broad range of microelectronics related topics and to stimulate new collaborations among the participants.

The MicDAT' 2018 conference has attracted researchers and practitioners in the related fields, from around the world including 3 keynote and 2 invited speakers from Africa, Asia, Europe and South America, who were invited to overview the progress in selected research trends. We have got more than 50 submissions, and finally, 33 papers have been selected for presentations (25 oral and 8 posters presentations) including keynote and invited presentations, submitted by authors from 20 countries (7 European and 13 non-European countries), covering theory, design, device technology and applications. To accommodate this range of interests, the 1st MicDAT' 2018 Conference was organized in one dedicated poster sessions and 4 oral tracks, including *'Advances in Analog & Digital'*; *'Advances in Technology'*; *'Simulation & Emulation'*, and *'Applied Microelectronics'*.

The proceedings contains all papers of oral, poster and invited presentations. We hope that these proceedings will give readers an excellent overview of important and diversity topics discussed at the conference. Based on the proceeding's contributions, selected and extended papers will be submitted by the authors to the '*Sensors & Transducers*' open access journal (ISSN: 2306-8515, e-ISSN 1726-5479) or special issue of *Journal of Low Power Electronics and Applications* (JLPEA, ISSN 2079-9268) - an MDPI international, peer-reviewed open access journal The limited number of articles, published in *'Sensors & Transducers'* journal will be invited to be extended for '*Advances in Microelectronics: Reviews'*, Vol. 2, Book Series.

We thank all authors for submitting their latest work, thus contributing to the excellent technical contents of the conference. Especially, we would like to thank the individuals and organizations that worked together diligently to make this conference a success, and to the members of the International Program Committee for the thorough and careful review of the papers. It is important to point out that the great majority of the efforts in organizing the technical program of the conference came from volunteers.



Prof., Dr. Sergey Y. Yurish
MicDAT' 2018 Chairman

(001)

A Ku-Band Power Amplifier Using Differential Transmission-Line Transformer in 0.25-μm GaN

Hwann-Kaeo Chiou and Kai-Yen Chang
Department of Electrical Engineering, National Central University,
Jhongli City, Taoyuan County 32001, Taiwan
Tel.: + 88634269021, fax: + 88634255830
E-mail: hkchiou@ee.ncu.edu.tw

Summary: This paper presents a Ku-band monolithic microwave integrated power amplifier (PA) in WIN^{TM} 0.25-μm Gallium-Nitride (GaN) and Silicon-Carbide (SiC) HEMT power device technology. The broadband performance is achieved by using low-loss Guanella-type differential transmission-line transformers (DTLTs) for both input and output matching networks. The designed PA achieves a 3-dB bandwidth from 13 to 18.2 GHz with a small signal gain of 14.7 dB. The continuous wave (CW) measurements demonstrate a maximum saturated output power of 32.3 dBm, an output 1-dB gain compression point (OP1dB) of 27.6 dBm, and a maximum power added efficiency of 14.8 %. The chip dimensions, including all pads, are 2.16 × 1.45 mm^2.

Keywords: GaN power amplifier, Ku-band, Differential Transmission-Line Transformer (DTLT).

1. Introduction

Power amplifier is a key part in RF front-end module (FEM). GaN technology became a good candidate for designing high output power and high efficiency power amplifier due to its having wider energy band gap, higher electron saturation velocity, better thermal conductivity and higher breakdown voltage than those of GaAs counterparts. Meanwhile, GaN PAs can operate at a high drain voltage which offers high optimal load impendence of the PA at high output level. These inherencies of GaN technology implies that GaN PA can be designed using low-Q matching network for the output power matching that offers wide bandwidth, high power and high power added efficiency (PAE) performance. These advantages make GaN PAs find various applications in base-station, mobile backhaul, and military and defense industries.

Recent works have reported on the GaN PAs that apply in Ku-band phase array systems and microwave T/R Front-End Modules (FEMs). A GaN dual-gate device at frequencies up to 18 GHz has been demonstrated in [1]. The Ku-band PA shows a small-signal gain of 10 dB and an output power of near 2.5 W at 18 GHz. Work [2] demonstrates an X-band fully integrated GaN switchless bidirectional amplifiers (BDAs) for phased array systems which integrates a power amplifier and a low noise amplifier with sharing matching networks. The PA presents a 27-dB average gain and about 30-dBm saturated power in transmit mode and a 15-dB gain with a 4.5-dB noise figure (NF) in receiving mode. Work [3] proposes an X-band GaN T/R FEM which comprises of a high power amplifier, a low noise amplifier and an SPDT in a chip area of 3 × 3 mm2. It presents nearly 8-W output power and 22-dB gain in transmit mode and 15-dB gain and 2.5-dB noise figure in receiver mode.

This paper designs a 1-W Ku-band wideband power amplifier for Ku-band backhaul applications. In order to achieve broadband, low-loss impedance transformer, Guanella-type differential transmission-line transformer can be utilized to transform impedance ratio [4]. In our previous work in CMOS technology [5], the DTLTs provided wideband 1:4 impedance transformation by broadside coupling and connecting the transmission lines parallel on the low impedance side and serially on the high impedance side. This work adopts the DTLT technique by using edge coupling in GaN process.

2. Circuit Design

The selections of the optimal biased conditions and transistor size are performed by swept the maximum frequency of oscillation f_{max} against the biased current density. As shown the simulations in Fig. 1, it suggests that the highest f_{max} can be obtained around the current density of 0.15 mA/μm for various transistor sizes. The chosen transistor sizes of the power and drive stages are 4 × 110 μm and 2 × 80 μm, respectively.

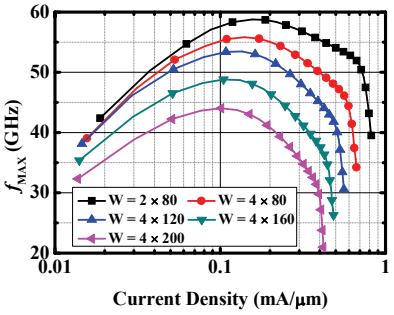


Fig. 1. Simulated fmax for WINTM 0.25-μm GaN.

Fig. 2 shows the schematic circuit of the proposed Ku-band wideband two-stage GaN power amplifier with two Guanella-type DTLTs as the input and output matching networks (OMNs). The T-shape broadband matching network is used to enhance broadband performance [6]. In addition, the parallel RC (R_1, R_2, C_1, and C_2) stabilizing circuits are added in front of the transistors Q_1 and Q_2 to ensure unconditional stability at all frequencies. The Guanella-type DTLTs were utilized as the input and output networks for 4:1 and 1:4 impedance transformations. Since GaN process only provides two metal layers, the DTLTs are realized by edge-coupling structure. To consider the current-handling capability that flow the metal traces, the edge-coupled output DTLT uses the stacked metal 2 to metal 1 to bear high current capability. As shown in Fig. 2, the metal trace of the output DTLT uses the 35-µm width and 5-µm space. The metal trace of the input DTLT uses 20-µm width and 5-µm space. The simulated optimum load impedance (Z_{opt}) of the power stage is 10.9 + j38.7 Ω at 15 GHz. The DTLT, L_{out} and C_{out} were utilized to transform Z_{opt} to 50 Ω. Fig. 3 shows the simulated impedance loci over the frequencies of the output matching network. As can be seen, the OMN brings 50 Ω load very close to the optimized load impedance (Z_{opt}) from 12 to 18 GHz. Thus, the wideband power match is successfully implemented by OMN DTLT.

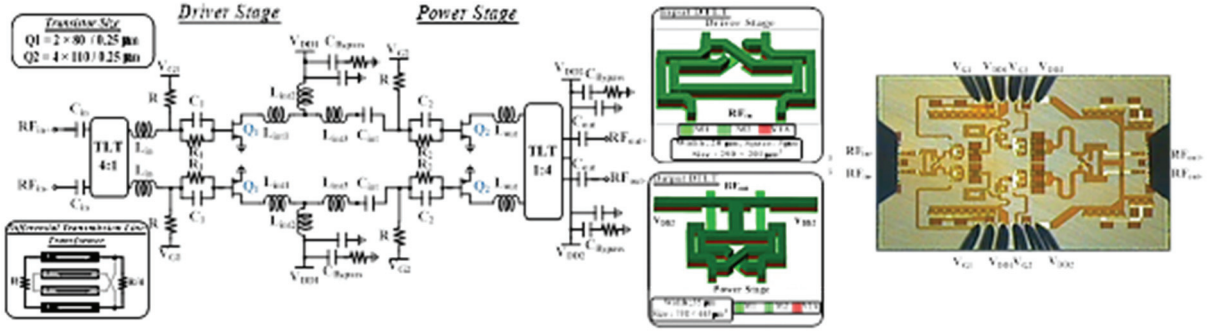


Fig. 2. Schematic circuit diagram and chip photo of the proposed Ku-band GaN power amplifier using Guanella-type DTLTs. The dimensions of the fabricated chip are 2.16 × 1.45 mm^2.

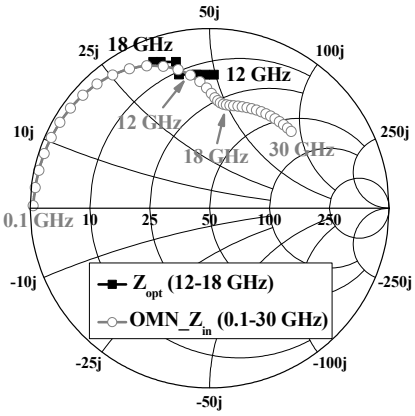


Fig. 3. Simulated impedance loci over the frequencies of the output matching network.

3. Measurement Results

Fig. 4 shows the photo of the fabricated GaN PA which was measured by on-wafer test. The de-embedded input and output baluns were used to convert the differential signal into single-ended signal. Fig. 5 shows the S-parameters at biased currents of I_{DD1} = 58.2 mA and I_{DD2} = 78.2 mA under the supply voltage of V_{DD1} = V_{DD2} = 28 V and V_{G1} = -2.43 V, V_{G2} = -2.71 V. The PA achieves a small signal gain of 14.7 dB and the 3-dB bandwidths are from 13-18.2 GHz which corresponds to a fractional bandwidth (FBW) of 33.33 %. As can be seen, the simulated and measured S-parameters are in good agreements. Fig. 6 shows the simulated and measured CW power performance at 15 GHz. The proposed PA exhibits the measured P_{sat} of 32.3 dBm, the OP1dB of 27.6 dBm, the peak PAE of 14.8 % and the PAE at P_{1dB} of 10.4 %. Fig. 7 displays the power performance versus the frequency of interest. A flat saturated power (30 ± 1 dBm) can be obtained from 13.5 to 17 GHz which is attributed by the successful use of DTLT in wideband OMN. Fig. 8 shows the PAE versus the frequency. The 1-dB bandwidths of saturated power and OP1dB are from 13.5 to 16 GHz and 13.5 to 16 GHz, respectively. From 13.5 to 16.5 GHz, the peak PAE are better than 10 %. Fig. 9 shows the measurements under 16 QAM/36 Mbps modulated signals. Fig. 9(a) shows the constellation diagram. Fig. 9(b) depicts the ACPR diagram and spectrum mask characteristics. Fig. 9(c) shows the ACPR at upper and lower sides.

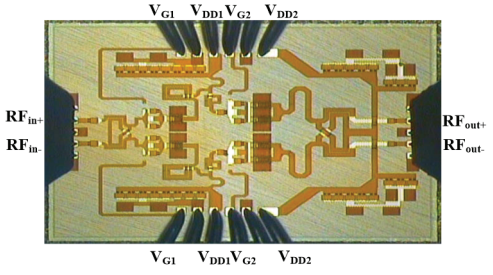


Fig. 4. Chip photo of the proposed PA with the size of 2.16 × 1.45 mm^2.

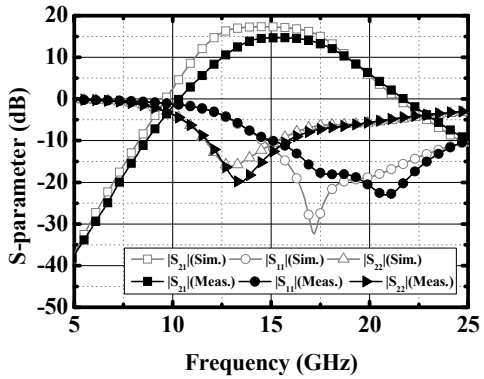


Fig. 5. Simulated and measured S-parameters of the proposed PA.

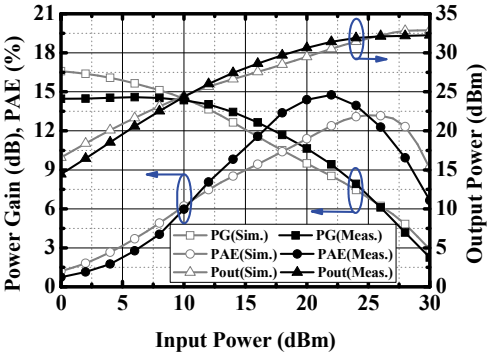


Fig. 6. Measured power performance at 15 GHz.

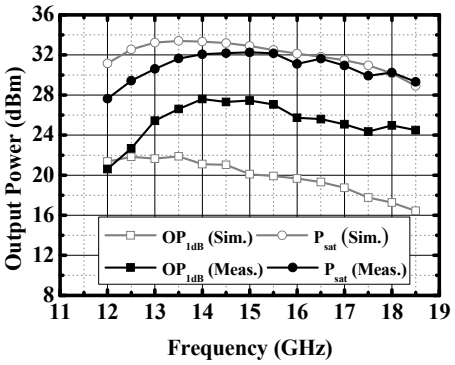


Fig. 7. Measured power performance versus the frequency of interest.

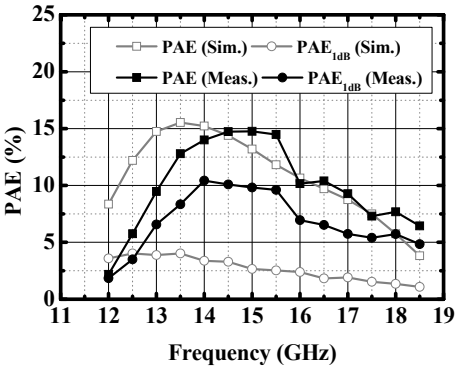
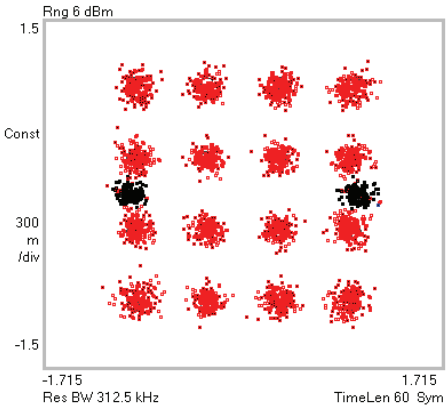
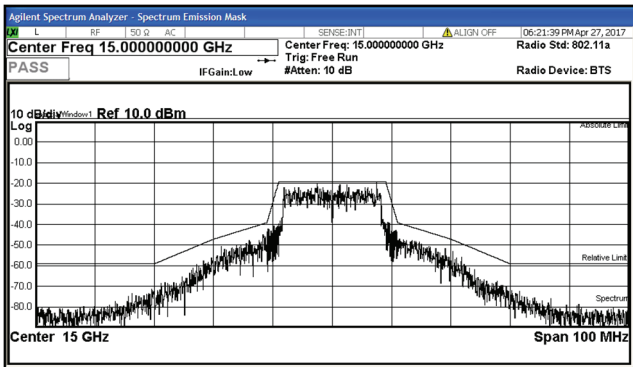


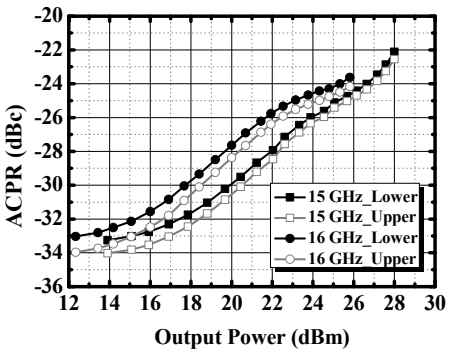
Fig. 8. Measured PAE versus the frequency of interest.



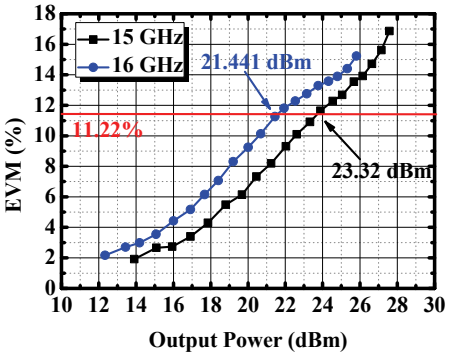
(a)



(b)



(c)



(d)

Fig. 9. The measurements under 16 QAM/36 Mbps modulated signals. (a) Constellation diagram, (b) ACPR, (c) ACPR with both sides, and (d) EVM.

Both ACPR in upper and lower sides are in slight difference at the same frequency. Fig. 9(d) shows the error vector magnitude (EVM) at 15 GHz and 16 GHz, respectively. In the acceptable EVM of 11 %, the proposed PA delivers 23.3 dBm and 21.4 dBm at 15 GHz and 16 GHz, respectively.

Table 1summarizes the performance of the recently published Ku-band 0.25-µm GaN PAs. Compared to the cited works, our GaN PA demonstrates the smallest chip size and the best flatness in gain and output power. Since the power measurements of the designed GaN PA are done by on-wafer testing in continuous wave (CW) mode with no heat sink, our work shows moderate performance in output power, PAE and fractional bandwidth. It is believed that the output power and PAE can be significantly improved under pulse mode testing with proper thermal design.

Table 1. Comparisons of Ku-Band Wideband 0.25-µm GaN PAs.

Ref.	**[1]**	**[2]**	**[3]**	**This Work**
GaN, process	0.25-µm	0.25-µm	0.25-µm	0.25-µm
Topology	Dual-gate, HPA	Switchless Bidirectional amplifier	T/R module	Push-pull +DTLT
Freq., (GHz)	16	10	9.9	15.6
BW_{3dB} (GHz)	14-18	8-12	8.6-11.2	13-18.2
Fractional bandwidth (%)	25	40	26	33
Gain (dB)	10	24-30	22	14.6
P_{sat} (dBm)	34	30-32.5	39	32.3
OP_{1dB} (dBm)	N/A	N/A	N/A	27.6
PAE_{Peak} (%)	N/A	10.5-15.4	25	14.8
Chip Size (mm^2)	2.75×2.25	2.5×1.87	3×3	2.16×1.45

4. Conclusion

A Ku-band wideband PA has been successfully developed in WIN 0.25-µm GaN/SiC process. By adopting the Guanella-type DTLTs, the PA achieves a small signal gain of 14.6 dB and a 3-dB bandwidth from 13-18.2 GHz which equals to 33.33 % fractional bandwidth. The PA exhibits a power gain of 14.6 dB, a P_{sat} of 32.3 dBm, an OP1dB of 27.6 dBm, a peak PAE of 14.8 % and a PAE at P_{1dB} of 10.4 %. 30 ± 1 dBm flat saturated power is obtained from 13.5 to 17 GHz due to the successful use of DTLT as the OMN. To the authors' best knowledge, the proposed PA is the first demonstration with Guanella-type DTLT to realize Ku-band GaN technology.

Acknowledgements

This work is supported by the Ministry of Science and Technology, Taiwan, R.O.C under MOST 106-2221-E-008-007-MY3. National Chip Implementation Center (CIC) of National Applied Research Laboratories, Taiwan, R.O.C., is also acknowledged for chip fabrication.

References

[1]. P. Dennler, F. van Raay, M. Seelmann Eggebert, R. Quay, O. Ambacher, Modeling and realization of GaN-based dual-gate HEMTs and HPA MMICs for Ku-band applications, *Proceedings of the Microwave Symposium Digest*, 2011, pp. 1-4.

[2]. D. Kim, D. H. Lee, S. Sim, L. Jeon, S. Hong, An X-band switchless bidirectional GaN MMIC amplifier for phased array systems, *IEEE Microw. Wireless Compon. Lett*., Vol. 24, Issue 12, December 2014, pp. 878-880.

[3]. A. Biondi, S. D'Angelo, F. Scappaviva, D. Resca, V. A. Monaco, Compact GaN MMIC T/R module front-end for X-band pulsed radar, in *Proceedings of the 11th European Microwave Integrated Circuits Conference (EuMIC'16),* London, 2016, pp. 297-300.

[4]. C. L. Ruthroff, Some broadband transformers, *Proceedings of IRE*, Vol. 47, August 1959, pp. 1337-1342.

[5]. P.-H. Chen, H.-K. Chiou, Y.-C. Wang, A K-band 24.1 % PAE wideband unilateralized CMOS power amplifier using differential transmission-line transformers in 0.18-µm CMOS, *IEEE Microw. Wireless Compon. Lett*., Vol. 26, Issue 11, November 2016, pp. 924-926.

[6]. P.-C. Huang, Z.-M. Tsai, K.-Y. Lin, H. Wang, A 17-35 GHz broadband, high efficiency PHEMT power amplifier using synthesized transformer matching technique, *IEEE Trans. Microw. Theory Tech.*, Vol. 60, Issue 1, January 2012, pp. 112-119.

(004)

High Gain, High Bandwidth Fully Differential Operational Amplifier Design Using Self-Cascode MOSFET with Adaptive Bias and Common Mode Feedback

Anu Gupta [1] and Kalpraj Vaidya [2]
[1] Department of Electrical & Electronics Engineering, BITS PILANI, Rajasthan
[2] M. E. (Microelectronics), BITS PILANI, Rajasthan
E-mail: anug@pilani.bits-pilani.ac.in

Summary: In this paper, an adaptive fully differential Operational Amplifier using Self Cascode Transistor giving a maximum differential gain 75.31 dB with slew rate of 14.58V/μS has been presented. In comparison to conventional design, proposed design with adaptive bias has slew rate increased by 7× for a capacitive load of 3pF. An adaptive bias circuit with current reference circuit is also designed using Self Cascode configuration to get reference current varying by only 20 nA when temperature varies from 25°C to 100 °C. A Common Mode Feedback circuit designed using Self Cascode shows only 0.01 % variation in V_{ocm} as V_{icm} varies by 1V. The proposed Operational Amplifier has been developed in a standard TSMC 0.18 μm CMOS technology with 3.3 V power supply and the simulations are done using Cadence software.

Keywords: Self cascode, High DC gain, Adaptive bias, CMFB, OpAmp, Current reference.

1. Introduction

The decrement of power supply for low power design makes it difficult to implement useful analog circuits, so novel circuit architectures have to be introduced. The values of the current sources inside the amplifiers are the main sources responsible of quiescent power dissipation. In this paper we propose a novel rail-to-rail fully differential self cascode (SC) operational amplifier (OPAMP), showing enhanced gain characteristics, where DC gain has been enhanced by a technique which increases the output impedance of the OTA input stage through a regenerative feedback [1] [2]. Fig. 1 shows the variation of Rout with length of M1 in SC, where "Ls" and Ld are transistor lengths for M1 and M2 respectively in SC already published in [2] but reproduced here.

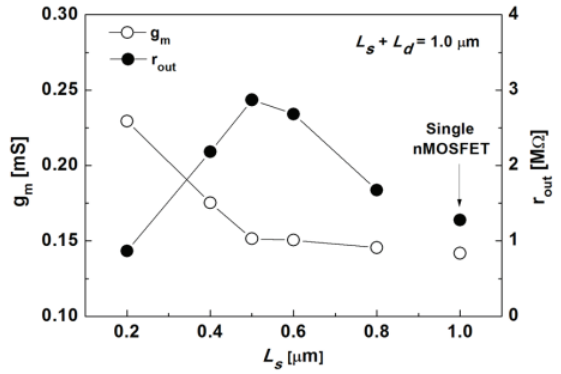


Fig. 1. Variation in $g_{m\,eff}$, and R_{out} of SC with variation in Ls and Ld [2].

Using this, highly optimized SC can be obtained by just varying the length of M1 resulting in maximum gain of OP AMP. SC is also used in the design of current mirrors in this paper.

1.1. Analysis of Self Cascode Transistor

Fig. 2 shows an NMOS SC configuration with gates shorted together and width of upper transistor is **m** times the lower transistor where **m** >> 1. Length can be adjusted between the two so as to get the optimized trans-conductance gm_{eff} and output résistance R_{out}.

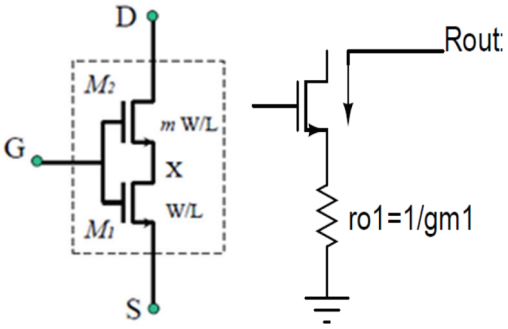


Fig. 2. (a) Self Cascode Transistor,
(b) Circuit for equivalent impedance of nMOS SC.

For this design, Ln = 400 n (for M1) and Ln = 600 n (for M2) transistor. Fig. 4 shows that Gm of SC increases with decrease in length but its R_{out} increases. Hence, an optimum value for gm_{eff} and r_o needs to be found out which will provide highest gain as compared to non SC transistor. Similar but complementary setup is made and used for pMOS transistors.

For a VDS varying from 0 to 3.3 V, 'gm_{eff}' graphs are plotted in Fig. 3. As observed, gm_{eff} and R_{out} are functions of length of M1 transistor. Fig. 2b shows circuit for computing equivalent impedance R_{out} of SC. Equivalent trans-conductance 'gm_{eff}' and R_{out} of SC are as computed below in equation (1), and (2).

$$R_{out} = \left(g_{m2}r_{o2}r_{o1} - r_{o2} - r_{o1}\right) \approx \left(g_{m2}r_{o1} - 1\right)r_{o2} = \left(mg_{m1}r_{o1} - 1\right)r_{o2} = \left(m-1\right)r_{o2}, \quad (1)$$

$$g_{meff} = \frac{g_{m2}}{m} = g_{m1}. \quad (2)$$

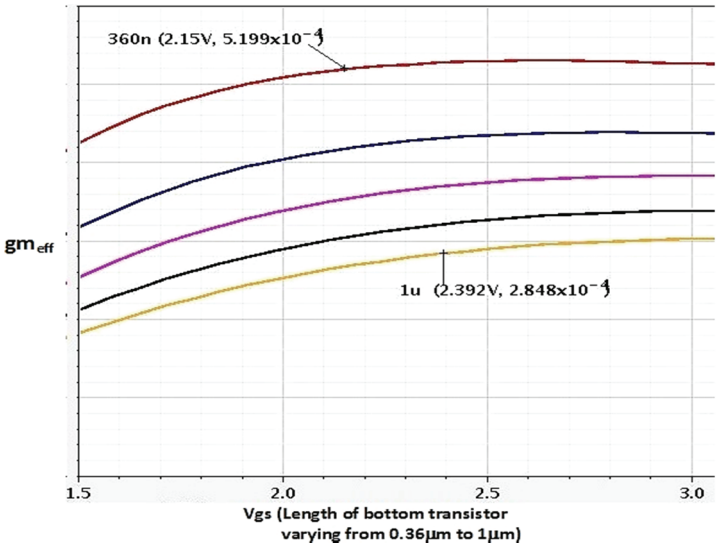


Fig. 3. Variation of gm_{eff} versus V_{gs}.

2. OPAMP Schematic Design

Fig. 4 shows the schematic design of proposed OPAMP. Here, a positive feedback has been provided at the PMOS stage to get a gain increment of about 35 dB as compared to classical two stage cascode OPAMP at 1MHz. Figs. 5-7 shows frequency response for Adm, and Acm respectively of proposed OPAMP with R-C frequency compensation. Table 1 shows the tabulated values of characterizing parameters of proposed and conventional OPAMP.

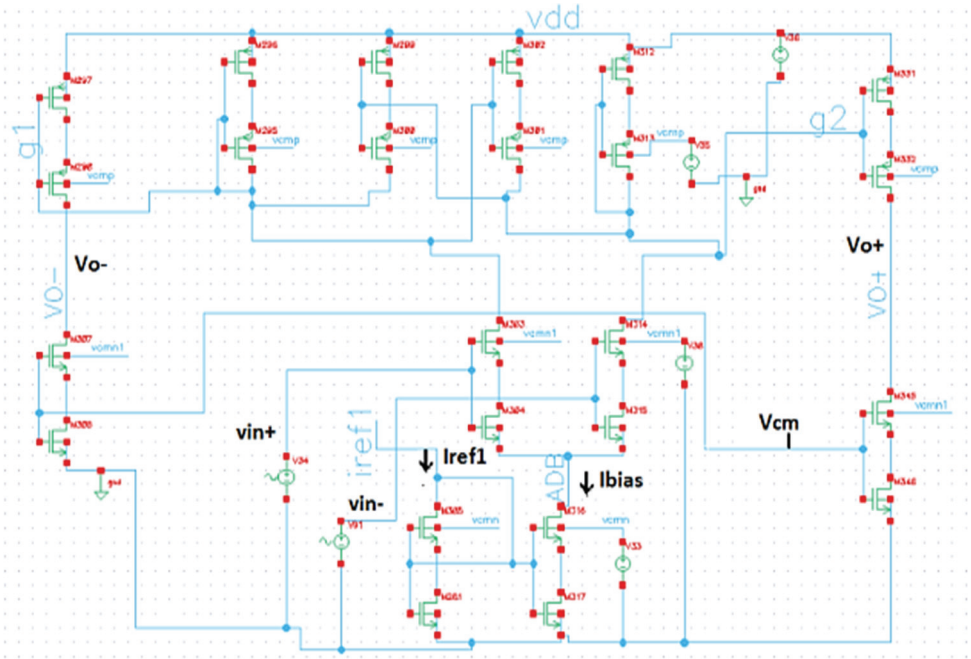


Fig. 4. Schematic design of proposed OPAMP [4].

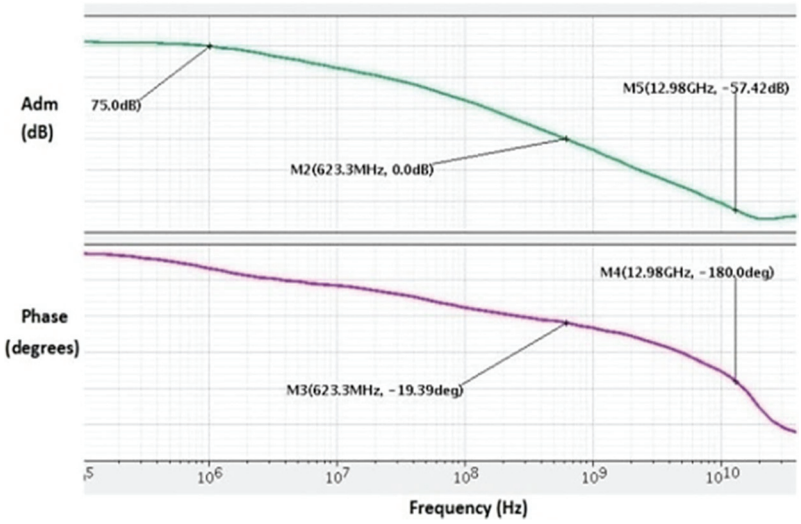


Fig. 5. Differential mode gain (Adm) of proposed design versus frequency.

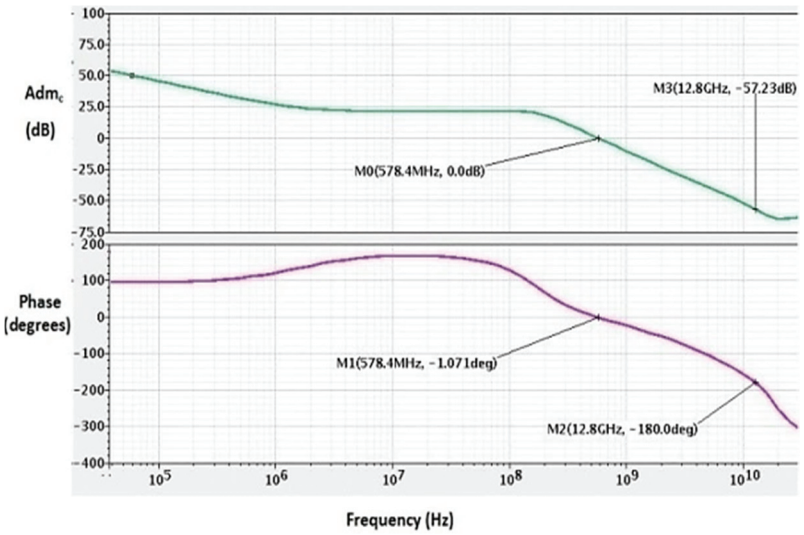


Fig. 6. Adm of proposed OPAMP with R-C miller compensation at second stage Vs. frequency.

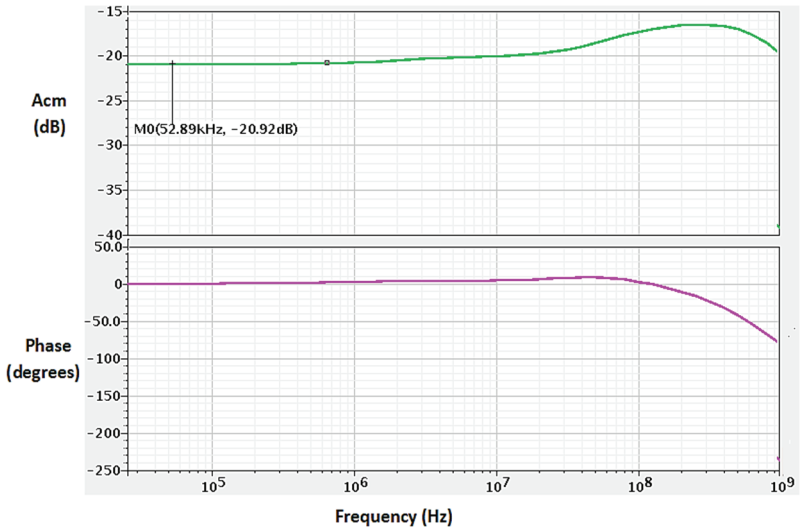


Fig. 7. Common mode gain (Acm) of proposed design versus frequency.

Table 1. Simulated values of characterizing parameters of proposed OPAMP for V_{dd}=3.3V.

Parameter	Proposed OPAMP Design	Conventional 2-stage OPAMP
DC Differential Mode Gain, Adm, (dB)	75.31	40
DC Common mode Gain, Acm, (dB)	-20.92	---
CMRR (dB)	99.23	---
Bandwidth (UGB) (MHz)	623.12	0.75
Phase Margin (deg)	82	---
PSRR (dB)	53.86	---
ICMR (mV)	700	---
OCMR (mV)	800	1000
Slew Rate (58V/µS)	14.58	2.3

3. Novel Current Reference Circuit Design

Typically CMOS reference current, Fig. 8 is designed using a CMOS Widlar source [5] mirror and a passive resistor. The precision of the reference current depends on the complete value of the resistor. A slight variation in the resistor value can degrade the performance over temperature and process corners as current I is proportional to inverse of mobility and square of resistance. Since µp is a temperature dependent variable that reduces with temperature, the reference current 'I' will increase with temperature. Also, the mobility changes with carrier concentration, which makes the reference current sensitive to process variations too. Thus in our OPAMP, a current reference is designed with only MOS transistors using SC as shown in Fig. 9 generating a 10 µA in each arms. Here, instead of using resistor, a SC is replaced in linear region. PMOS Transistor pairs e.g. (M11, M12) in Fig. 9 is biased in deep triode region so that even if temperature increases, (M11, M12) remains in linear region. Thus a better stability with respect to temperature can be obtained by varying the W/L of Transistor pair (M11, M12).

Fig. 10 shows the variation of reference current I_{ref} is by only 0.002 uA with temperature varying from 25 to 80 degree C.

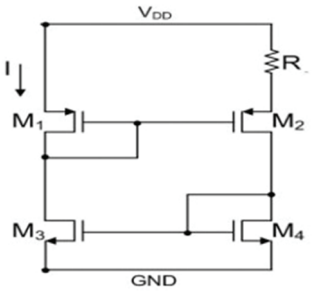


Fig. 8. Conventional Wildar reference current Generation [5].

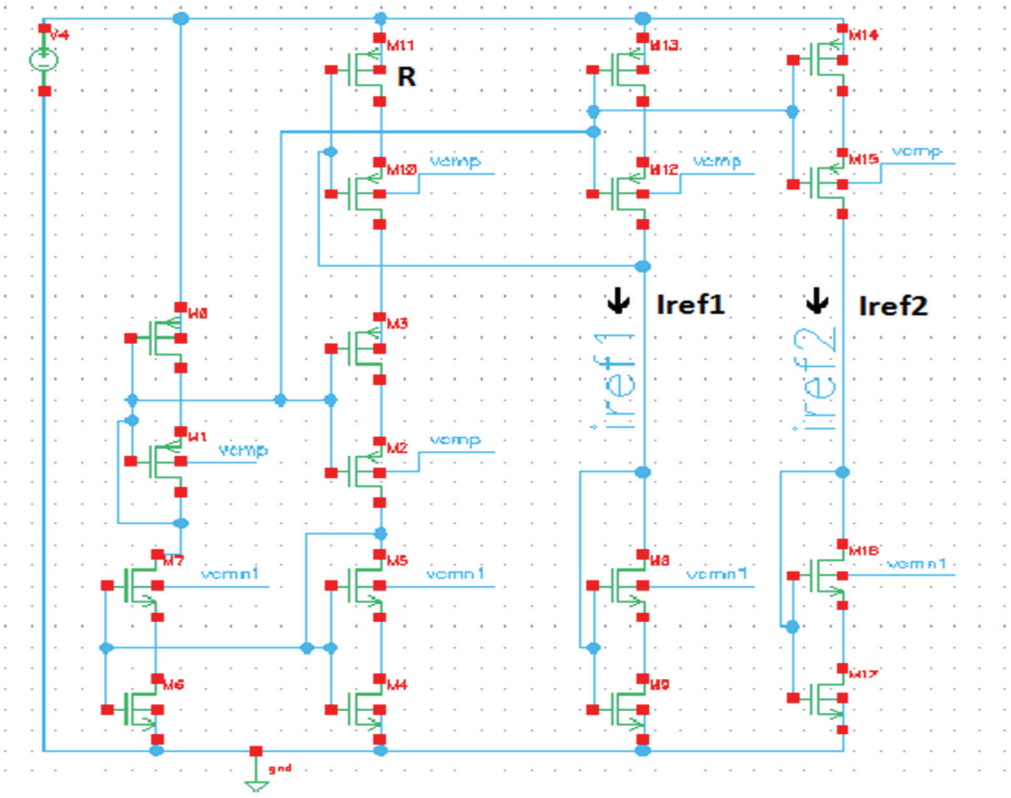


Fig. 9. Proposed current reference design with only SC's.

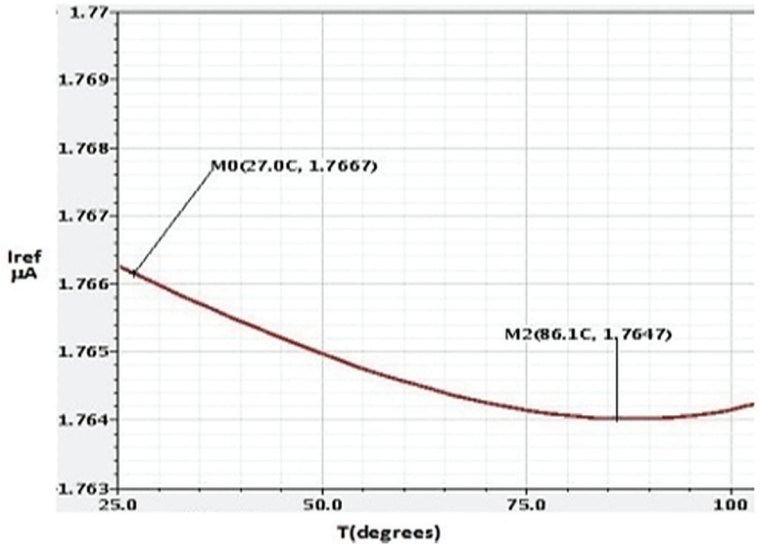


Fig. 10. Variation of reference current Iref w.r.t temperature.

4. Adaptive Bias Circuit

An adaptive bias circuit is designed for slew rate improvement. The circuit is shown in Fig. 11. Basic current subtractor is realized in differential arms to provide extra current as seen from Eq. (3)

$$I_{total} = I_{bias} + A * \mathrm{mod}(I_2 - I_1), \quad (3)$$

where I_1 and I_2 are the current in branches close to main I_{bias} current mirror branch in differential tail branch.

$$I_{total} = I_{bias}(1 + A + A^2 + ...). \quad (4)$$

To ensure transistors to remain in saturation it is necessary to have value of parameter A < 1 but not too less than 0.5 as it will reduce slew rate. I_{total} forms a geometric progression because of the positive feedback for A < 1 as in Eq. (4). For A = 0.9, current I shows 10 times improvement in slew rate as observed in Figs. 12 and 13.

5. Common Mode Feedback Circuit

Common mode feedback circuit is designed to maintain stable DC value at output, which will stabilize from process variations. CMFB senses voltage V_{out} and adjust the current of Ibias to maintain constant V_{ocm}. Instead of using resistive sensing, we have used all SC in implementation of CMFB as shown in Fig. 14.

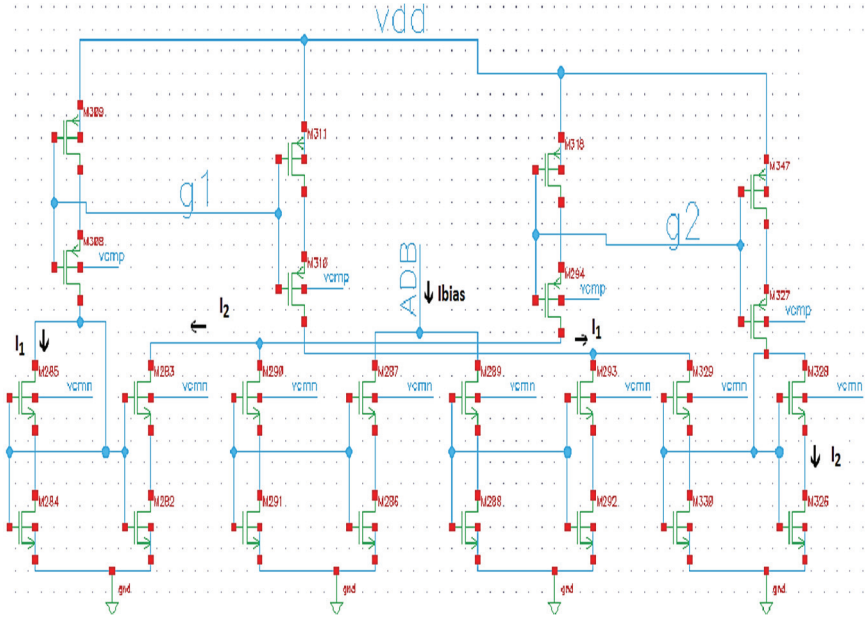


Fig. 11. Adaptive bias circuit [4].

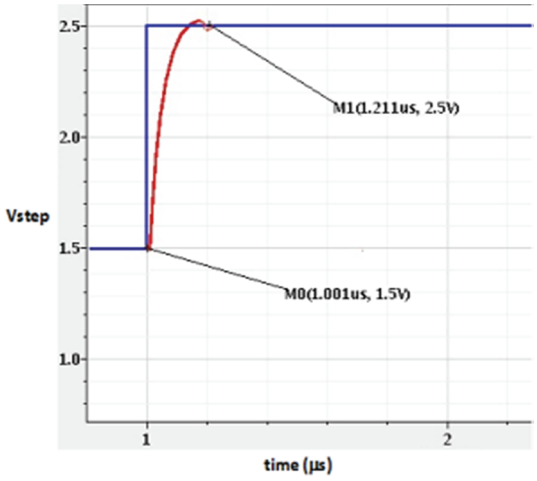


Fig. 12. Step voltage response of proposed without adaptive bias, Slew Rate =2.3 V/µS.

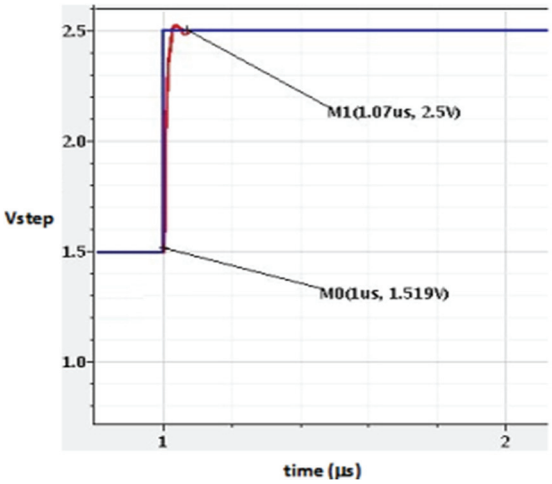


Fig. 13. Step voltage response with adaptive bias, Slew Rate =14.58V/µS.

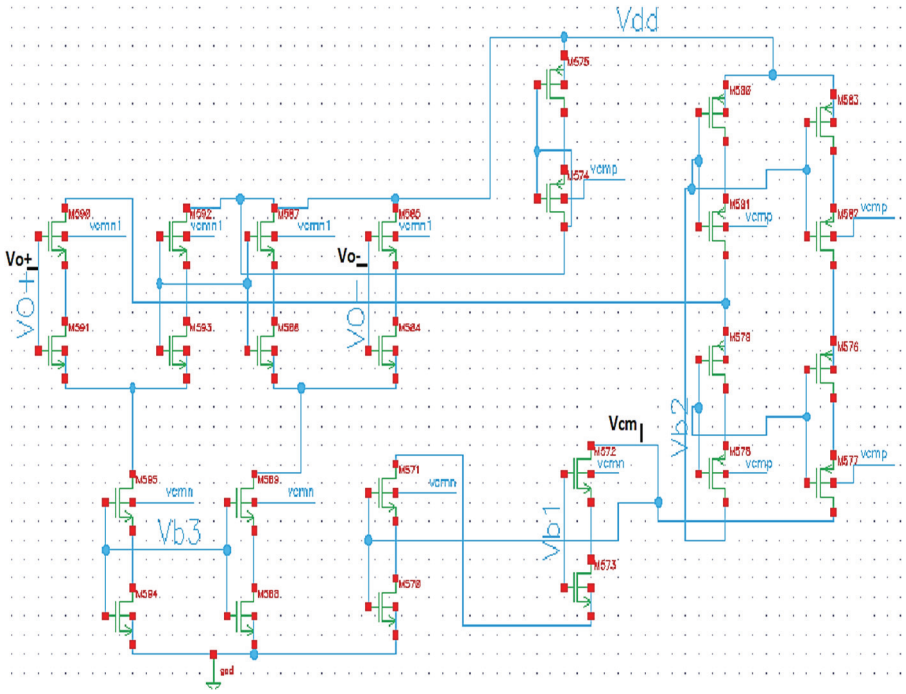


Fig. 14. Common Mode Feedback Circuit (CMFB) circuit.

6. Conclusions

This paper presents a high performance 2 stage OPAMP design using SC MOS structure. Both the trans-conductance gm_{eff} and output resistance 'Rout' are optimized by channel length ratio of the SC MOSFETs Table 1 summarizes the parameters of proposed design.

As seen in Fig. 15, CMFB circuit levels the output to a constant value, within 0.01 % for Vicm varies from 1.5 to 2.5 V_{in} differential mode operation. The DC gain improvement has been achieved by using partial positive feedback technique. This technique improves gain and bandwidth of the circuit. The measured DC gain of the proposed OPAMP is 35 dB higher and slew rate is 7 times higher than that of the conventional 2 stage cascode OPAMP. The proposed OPAMP has a power efficient high DC gain adaptive bias circuit which utilizes current subtractor based on CCM for providing extra tail current sources in addition to fixed bias current sources.

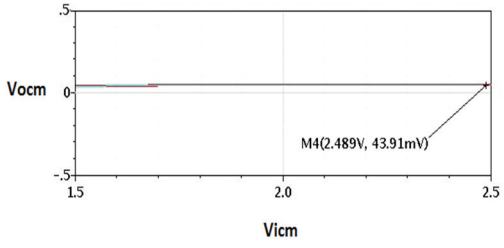


Fig. 15. Variation of Vout-common mode (Vocm) w.r.t input common mode voltage Vicm varying from 1.5 to 2.5 V.

Acknowledgements

This research work is supported by Department of Science and Technology, Govt. of India under Grant SR/FST/ ETI-346/20 13.

References

[1]. B. Hershberg, S. Weaver, U. K. Moon, Design of a Split-CLS pipelined ADC with full signal swing using an accurate but fractional signal swing opamp, *IEEE J. Solid-State Circuits*, Vol. 45, Issue 12,, 2010. pp. 2623-2633.

[2]. H.-S. Kim, K.-J. Baek, D.-H. Lee, Y.-S. Kim, OPAMP using self cascoded structure, *Transactions On Electrical And Electronic Materials*, Vol. 15, Issue 3, 2014, pp. 149-154.

[3]. G. Ferri, V. Stornelli, A. D. Marcellis, A. Celeste, A rail-to-rail DC-enhanced adaptive biased fully differential OTA, in *Proceedings of the 18th European Conference on Circuit Theory and Design (ECCTD'07),* 2007, pp. 527-530.

[4]. B. Razavi, Design of Analog CMOS Integrated Circuits, by, *McGraw-Hill*, 2002,

[5]. Fully Differential CMOS OPAMP Having Adaptive Bias and Common Mode Feedback Circuits, Patent Number 5729178, *United States Patent*.

(005)

The Algorithm and Software Implementation of the Thermal Transient Testing Technology Applied in High-Power Electronics

Erping Deng [1,2], Yaru Shen [1], Zhibin Zhao [1], Jinyuan Li [2] and Yongzhang Huang [1]
[1] North China Electric Power University, State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, Beijing, China
[2] State Grid Global Energy Interconnection Research Institute, Changping District, Beijing, China
Tel.: + 8613260057843
E-mail: dengerpinghit@163.com

Summary: Thermal transient testing technology is currently the most effective method for obtaining thermal characteristic parameters of high-power semiconductor devices. This paper briefly outlines the basic theory of the thermal transient testing technology, and focuses on two key algorithms in the implementation of this technology: deconvolution and transformation of thermal network model algorithms. Meanwhile, a software system of the thermal transient testing applied to power semiconductor devices is established. Mathematica is used to solve the problem of data accuracy in network model transformation. By comparing the commonly used deconvolution algorithm, it is concluded that the thermal characteristic parameters of the device calculated by Bayesian deconvolution based on Richardson-Lucy algorithm are the most precise. Finally, the measurement data of power semiconductor devices tested by mature commercial thermal transient testing equipment is set as an example to verify the accuracy and effectiveness of the proposed system.

Keywords: High-power electronics, Structure function, Thermal transient testing technology, Deconvolution, Thermal network model transformation.

1. Introduction

High-Power semiconductor devices due to high voltage, high current, and excellent switching performance, have gradually been applied to high voltage and high power density applications, especially power electronics. Thermal characteristic have always been a quite important concern in the application of power semiconductor devices. 55 % of the failure of electronic devices is caused by heat-related problems [1]. Therefore, it is quite important to accurately measure the thermal parameters of power electronics.

For high-power IGBT devices, junction temperature and thermal resistance are two critical thermal characteristics. Many electrical parameters of the device are related to the junction temperature, which is also affected by the thermal resistance of the device. Accurately measuring the junction temperature and thermal resistance of high-power IGBT devices not only helps to optimize the heat dissipation structure of the device package, but also guides users to give full play to the device performance and prolong its service life. This has become a common concern for the manufacturers and users. Traditional steady-state thermal resistance test method can only measure the overall thermal resistance of the device, so that the further thermal analysis of the device is restricted. The thermal transient testing technology can comprehensively analyze thermal properties of each layer structure of the device from chip to heat sink on the path of heat conduction, construct equivalent thermal model of devices, and provide reliable data base for the research on thermal characteristic of the device [2].

Hence, in order to give full information of the thermal characteristic parameters of high-power electronics, a complete set of software analysis and test system is proposed in this paper. The system can accurately measure the thermal characteristic parameters, and provide reliable data foundation for life expectancy, extreme operation and over-temperature protection [3]. The result has important reference value and practical significance.

2. Methodology

Fig. 1(a) is a simple package model composed of different materials. The model is placed on an ideal heat sink and other surfaces are thermal adiabatic. When a constant power P_H is applied to the model, the model can be equivalent to the n-order RC network shown in Fig. 1(b). Among them, the thermal transient response function $a(t)$ of the model under the power P_H is

$$a(t) = P_H \cdot \sum_{i=1}^{n} R_{thi}(1-\exp(-\frac{t}{\tau_i})), \qquad (1)$$

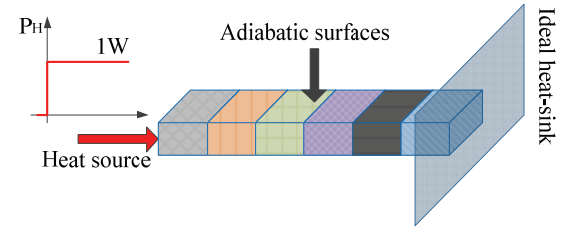
where P_H is the unit power, R_{thi} denotes the thermal resistance of the heat transfer model equivalent to an RC network, t is the time, τ_i represents the time constant and can be calculated by thermal resistance R_{thi} and thermal capacity C_{thi}.

When the applied power step denotes as a unit power, the time t in formula (1) is logarithmic and the formula (1) is derived to obtain the convolution formula shown in formula (2).

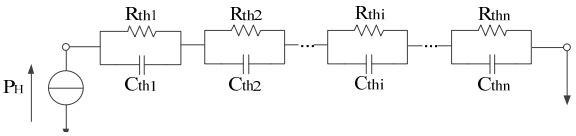
$$\frac{d}{dz}a(z) = R(z) \otimes w(z) + n(z), \tag{2}$$

where $\otimes$ is the convolution operator, the $w(z)$ represents the constructor which can be calculated by the following formula

$$w(z) = \exp(z - \exp(z)). \tag{3}$$



(a) simple one-dimensional heat transfer model



(b) the equivalent RC network

Fig. 1. Heat transfer model and its equivalent RC network.

The thermal transient response function $a(z)$ in equation (1) can be obtained by measuring the change of temperature-sensitive parameters of the device in the cooling process and combining the relationship between the temperature-sensitive parameters and the junction temperature and thermal impedance. In addition, the constructor is known. Hence, the time constant spectrum is

$$R(z) = \frac{d}{dz}a(z) \otimes^{-1} w(z), \tag{4}$$

where $\otimes^{-1}$ is the deconvolution operator.

It should be noted that the actual measured thermal transient response signal is usually mixed with a certain noise signal $n(z)$. These noise signals can affect the results of thermal transient tests that must be taken into account when analyzing.

$$\frac{d}{dz}a(z) = R(z) \otimes w(z) + n(z), \tag{5}$$

The thermal transient testing technology is based on the formula (1). Thermal transient response signal $a(z)$, time constant spectrum $R(z)$, constructor $w(z)$ and noise $n(z)$ in the formula (1) are all expressed as function of logarithmic time z. Take the derivative and deconvolution operation of $a(z)$ to get $R(z)$. Then, split $R(z)$ into a number of segments having Δz width and compute the thermal resistance and heat capacity parameters of the Foster model. Considering the heat capacity of Foster model with no clear physical meaning, hence thermal network model transformation algorithm is used to transform the Foster model to Cauer model, which can reflect the actual heat capacity transfer process. Finally, the structure function of the device can be obtained by accumulating the thermal resistance and heat capacity parameters of the Cauer model in stages, or taking the derivative after accumulating [4].

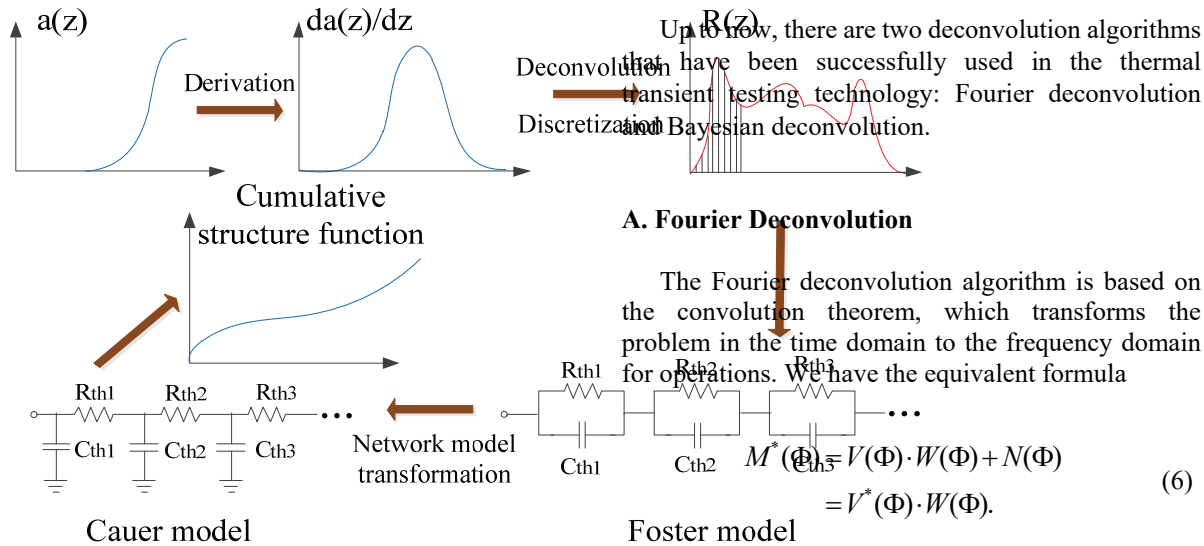


Fig. 2. The process of the thermal transient test technology.

2.1. Deconvolution Algorithm

Up to now, there are two deconvolution algorithms that have been successfully used in the thermal transient testing technology: Fourier deconvolution and Bayesian deconvolution.

A. Fourier Deconvolution

The Fourier deconvolution algorithm is based on the convolution theorem, which transforms the problem in the time domain to the frequency domain for operations. We have the equivalent formula

$$\begin{aligned} M^*(\Phi) &= V(\Phi) \cdot W(\Phi) + N(\Phi) \\ &= V^*(\Phi) \cdot W(\Phi). \end{aligned} \tag{6}$$

Thus theoretically we can obtain the required function by a simple division as shown in formula (7).

$$R(z) = IFFT \parallel \frac{M^*(\Phi)}{W(\Phi)} \parallel . \quad (7)$$

Because the noise corresponds to the high frequency component in the signal spectrum. Although the noise signal has smaller amplitude relative to the measured signal, the high-frequency components of the constructor are some very small items with a smaller magnitude. After the division operation, the noise signal will be amplified, resulting in many differences between the deconvolution reconstruction signal and the original signal, sometimes even resulting in unacceptable results. Therefore, it is necessary to properly handle the noise problem during the application process.

B. Bayesian Deconvolution

Different from the Fourier deconvolution, Bayesian deconvolution is based on Bayes' theorem and total conditional probability formula. It can avoid the noise problem in Fourier deconvolution algorithm. The procedure described by [5] has been proven very suitable for the time-constant spectrum identification. These applies the following iterative formulas

$$R^{i+1}(z) = R^i(z) \cdot (w(z) \oplus \frac{da(z)/dz}{w(z) \otimes R^i(z)}), \quad (8)$$

$$R^{i+1}(z) = R^i(z) \frac{w(z) \oplus (da(z)/dz)}{w(z) \oplus (w(z) \otimes R^i(z))}, \quad (9)$$

The deconvolution algorithm using the iterative formula shown in equation (8) is called Richardson-Lucy algorithms, and shown in equation (9) is called Positive iterative deconvolution. Whether formula (8) or formula (9), the amplitude of the reconstructed signal will be amplified during each iteration. In order to make the reconstructed signal as close as possible to the original input signal, the correction I needs to be introduced to improve the formula.

$$R^{i+1}(z) = R^i(z)(w(z) \oplus \frac{da(z)/dz}{w(z) \otimes R^i(z)}) * I, \quad (10)$$

$$R^{i+1}(z) = R^i(z) \frac{w(z) \oplus (da(z)/dz)}{w(z) \oplus (w(z) \otimes R^i(z))} * I, \quad (11)$$

2.2. Network Model Transformation Algorithm

Because the Foster network model describes the node-to-node thermal capacity without explicit physical meaning, the Foster network model needs to be converted into a Cauer network model that describes the thermal capacity between the nodes and reference nodes. The existing network model transformation algorithm has been relatively mature, and the detailed conversion process is given in [4]. However, due to the limitation of software accuracy, truncation error and operation error occur when the network model conversion operation is performed. The obtained structure function is inconsistent with reality. Therefore, appropriate calculation software should be selected during processing to avoid this situation.

The method that have been published and used to solve the data accuracy problem of the network model conversion process in the thermal transient testing technology is the GMP (GNU MP Bignum Library) open source math library mentioned in the JESD 51-14 standard. However, GMP library functions are written in C language. When calling in interpretive language programming software, you need to write a special interface function, or directly use it in the C language-based software. No matter which way you need to have a programming base. The simulation verified that using Mathematica, a multi-precision calculation software, not only can achieve the same accuracy as GMP, but also is simpler and easier to operate than GMP. This greatly reduces the difficulty of algorithm implementation.

Based on the above theory, this paper establishes a software system of thermal transient testing technology as shown in Fig. 3, which is used to measure the thermal characteristic parameters of power electronics.

3. Case Study

Taking the thermal transient response signal of power electronics measured by commercial thermal transient tester as an example, and the time constant spectrum calculated by the equipment as a reference value. This article compares two kinds of common deconvolution algorithms. Meanwhile, the thermal transient testing software system established in this paper is used for simulation analysis to verify the validity and accuracy of the system. In order to make the results comparable, the simulation parameters are set with the testing equipment parameters.

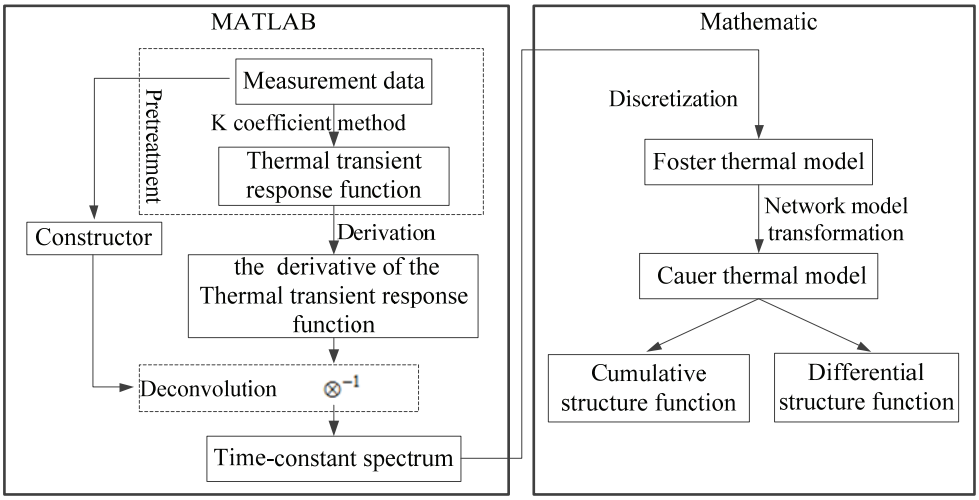


Fig. 3. The Thermal transient testing software system.

3.1. The Contrastive Analysis of Deconvolution Algorithms

In order to compare the accuracy of thermal transient test results when different deconvolution algorithms are applied, this paper uses different deconvolution algorithms to process the same measurement data. The time constant spectrum deviation Δ is defined as the criterion for measuring the accuracy of the algorithm. The simulation results are shown in Table 1 and Fig. 4.

$$\Delta = \frac{\sum [X(z) - \overline{R}(z)]^2}{n}, \qquad (10)$$

Table 1. The deviation of time constant spectral calculated by different deconvolution methods.

Devia -tion	Fourier deconvolu-tion	Bayesian deconvolution	
		Richardson-Lucy algorithm	Positive iterative deconvolu-tion
Δ	0.00131	0.000199	0.000963

Table 1 shows that the result of Richardson-Lucy algorithm is closer to the reference value. The deviation of Richardson-Lucy algorithm is 0.000199, which is far less than the Fourier deconvolution, and less than the positive iterative deconvolution. Fig. 4 also shows that compared with the Fourier deconvolution algorithm and the Bayesian deconvolution based on the Positive iterative deconvolution, the structure function using the Bayesian deconvolution based on the Richardson-Lucy algorithm is most consistent with the reference value.

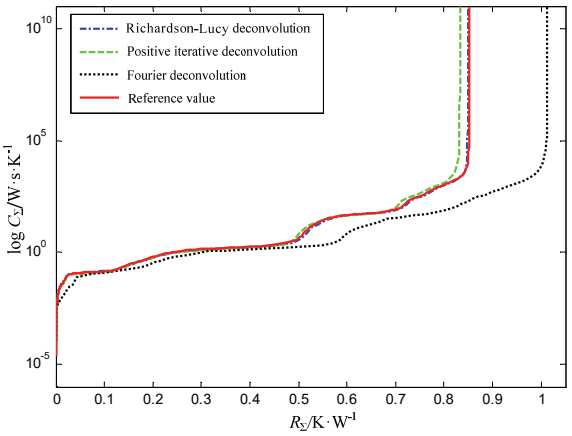


Fig. 4. The structure function of different deconvolution algorithms.

3.2. The Simulation Verification of Software System

Taking the measurement data of a high-power semiconductor device as an example, the thermal transient testing software system established in this paper is used for simulation calculation. After the calculation, structure function curves are shown in Figs. 5 and 6.

Choosing the structure function curve obtained from the thermal transient testing equipment as a reference, it can be seen that the simulation results through the system mentioned above are in good agreement with the reference values. The error between them is very small. Therefore, the software system established in this paper can obtain the thermal parameters of the device accurately and effectively. Furthermore, the internal structure of the device can be identified by combining two structure functions. Each layer structure is marked with different colors respectively.

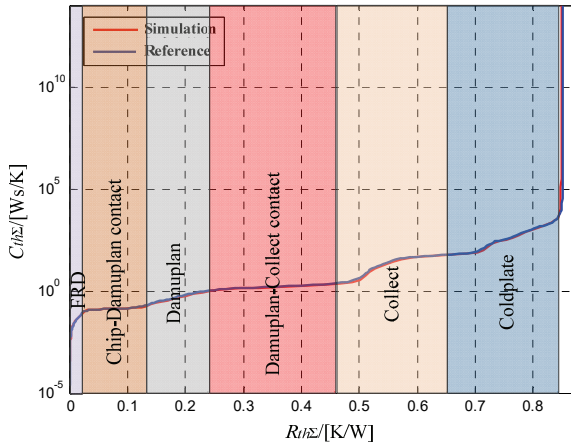


Fig. 5. Cumulative structure function.

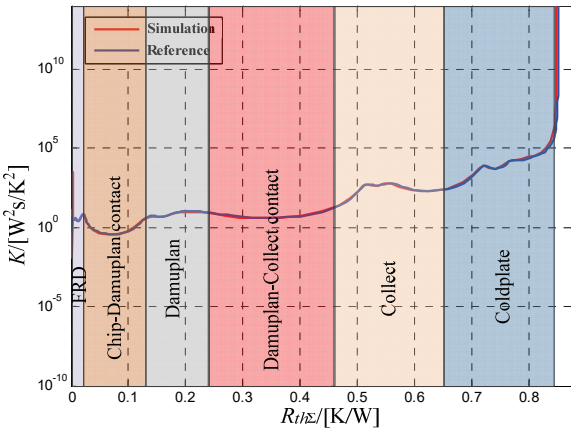


Fig. 6. Differential structure function.

4. Conclusions

A complete set of software system of the thermal transient testing applied to high-power semiconductor devices is established in this paper based on the research status of thermal transient testing technology at home and abroad. Aiming at the problem of deconvolution algorithm, this paper compares the commonly used deconvolution algorithm to get the conclusion that the Bayesian deconvolution algorithm based on Richardson-Lucy algorithm obtains the most accurate structure function. In response to another key issue: data accuracy in the process of network model conversion, it is proposed to reduce the difficulty of implementing the algorithm by using Mathematica to achieve the same effect as GMP. Finally, taking the actual measured data measured by a mature commercial thermal transient test equipment for power semiconductor devices as an example, the validity and accuracy of the system established in this paper are verified.

Acknowledgements

This work is supported by the Project of Manufacturing Technology and Complete Sets of Technology for Very Large Scale Integrated Circuits (2015ZX02301), the Science and Technology Project of State Grid (SGRI-GB-71-16-003) and the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Source, North China Electrical Power University (Grant No. LAPS17003).

References

[1]. Avionics/Elecsonic Integrity Program Requirements, MIL-A-87244A, *USAF*.

[2]. B. Smith, T. Brunschwiler, B. Michel, Comparison of transient and static test methods for chip-to-sink thermal interface characterization, *Microelectronics Journal*, Vol. 40, Issue 9, 2009, pp. 1379-1386.

[3]. V. Székely, Identification of RC networks by deconvolution: chances and limits, *IEEE Transactions on Circuits & Systems I Fundamental Theory & Applications*, Vol. 45, Issue 3, 1998, pp.:244-258.

[4]. Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Trough a Single Path, JESD 51-14, *Solid State Technology Association*.

[5]. M. Pruksch, F. Fleischmann, Positive iterative deconvolution in comparison to Richardson-Lucy like algorithms, *Astronomical Data Analysis Software and Systems VII, A.S.P. Conference Series*, Vol. 145, 1998, p. 496.

(006)

Investigation on Multilayer Conductor Interconnects of Integrated Circuits Using Finite Element Method

L. Belhimer, A. Benfdila and A. Lakhlef
Microelectronic Research Group, Faculty of Electrical Enginnering and Computer Sciences,
University Mouloud Mammeri, Tizi-ouzou, Algeria
Tel.: + 213662525717
E-mail: benfdila@ummto.dz, abenfdil@ictp.it

Summary: The present paper deals with the analysis approach of multiconductor microstrip systems an integrated circuits using the finite element method (FEM). Interconnects are multiple strip and multilevel in ICs. Today interconnects are great attention in high speed digital design and microwave integrated circuit application. With increased density of packing, line to line coupling of electromagnetic also becomes prominent. Computation of the matrices of capacitances, inductances per unit length of multiconductor is important since these elements are essential parameters in designing of package.

Keywords: Interconnects, Finite element method, Capacitance, Multiconductor, Transmission lines.

1. Introduction

Today the electronic circuits see their threshold of electromagnetic susceptibility decrease This increased vulnerability comes from their reduction in size in supply voltage and an increase in their frequency of operation the frequencies of the order of gigahertz are particularly harmful for these systems because by their wavelength they are likely to generate resonance phenomena on the tracks of the integrated circuits thus increasing the risks that it is disturbed.

Computation of the interconnect parameters such as matrices of capacitances and inductances per unit length is important since these parameters are essential in designing of package, lossless transmission line system and microwave circuits. Therefore, the improvement of accurate and efficient computational method to analyze the modeling of multiconductor structure becomes an important area of interest.

Transmission interconnect lines have been investigated for many years. In [1] Hassan Ymeri presented a new semi- analytical procedure for single and coupled interconnects on lossy silicon substrate. In [2] starting from several reasonable approximations, closed-from expression for the mutual impedance per unit length of coupled IC interconnects with

Silicon substrate have be proposed. [3], analysis of multiconductor quasi-TEM transmission lines and multimode waveguide is done. We can mention, finite difference methods (FDM) [4], Analytical method [5], the Green's function approach [6], the Galerkin method [7].

In this paper, we design four-conductor transmission lines interconnect with two dielectric layers, and four-conductor transmission line with two levels systems using FEM to calculate the capacitance matrix then compare the results with some methods in previous publications.

2. Main Results

The capacitance coefficients for a system of parallel microstrip lines are defined as follows, it is convenient to write [8-9]:

$$Q_i = \sum_{j=1}^{n} C_{sij} V_j, \qquad (1)$$

where V_j is the voltage of j^{th} conductor with reference to the ground plane, Q_i is the charge per unit length, C_{sij} is the short circuit capacitance between i^{th} and j^{th} conductor. The short circuit capacitances can be obtained either from measurement or from numerical computation [10-11]. We obtain

$$C_{ii} = \sum_{j=1}^{n} C_{sij}, \qquad (2)$$

$$C_{ii} = -C_{sij}, \; i \neq j, \qquad (3)$$

where C_{ii} is the capacitance per unit length between the i^{th} conductor and the ground plane. The coupling capacitances are illustrated in Fig. 1.

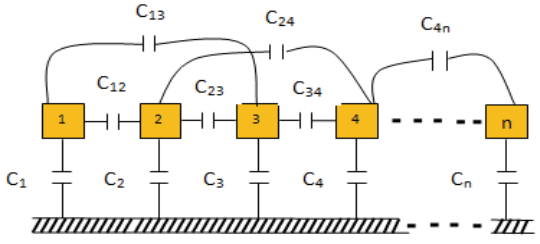


Fig. 1. The per unit length capacitances of general n conductor.

The matrix [c] capacitance for n conductor is given by

$$C=\begin{bmatrix} C_{11} & -C_{12} & .... & -C_{1n} \\ -C_{21} & C_{22} & .... & -C_{2n} \\ : & : & & : \\ -C_{n1} & -C_{n2} & .... & C_{m} \end{bmatrix}. \quad (4)$$

The inductance and capacitance of multiconductor transmission lines are related as

$$[L]=\mu_0\varepsilon_0[C_0]^{-1}, \quad (5)$$

where [L] is the Inductance matrix, $[C]^{-1}$ is the inverse matrix of the capacitance of multiconductor transmission line when all dielectric constants are set equal to 1, μ_0 is the permeability of space or vacuum, ε_0 is the permittivity of free space or vacuum.

The characteristic impedance and capacitance per unit length are related as follows:

$$Z=\sqrt{\frac{[L]}{[C]}}. \quad (6)$$

The electrical parameters are:

Capacitance per unit length matrix ([C] in pF/m), inductance per unit length ([L] in nH/m), impedance ([Z] in Ω).

To illustrate and validate the new proposed formulation, in the first section we consider a planar interconnects line including four strips, Fig. 2 shows the geometry of the model.

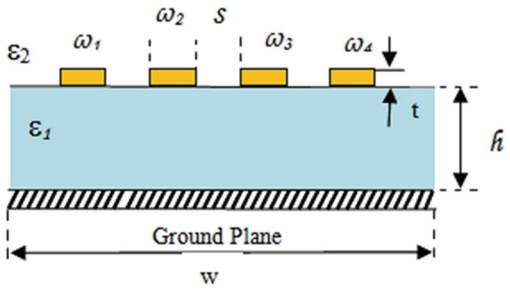


Fig. 2. Symmetric microstrip coupled interconnect.

This microstrip coupled interconnects have the following geometrical parameters: $\omega_1=\omega_2=\omega_3=\omega_4=$ 20 μm, S = 20 μm, h = 40 μm, t = 5 μm, $\varepsilon_1=11.7$, $\varepsilon_2=3.9$.

The capacitance per unit length of the multistrip transmission lines are related as follows:

$$C=\begin{bmatrix} 0.968 & -0.328 & -0.08 & -0.01 \\ -0.328 & 1.126 & -0.325 & -0.08 \\ -0.08 & -0.325 & 1.126 & -0.328 \\ -0.01 & -0.08 & -0.328 & 0.968 \end{bmatrix}.$$

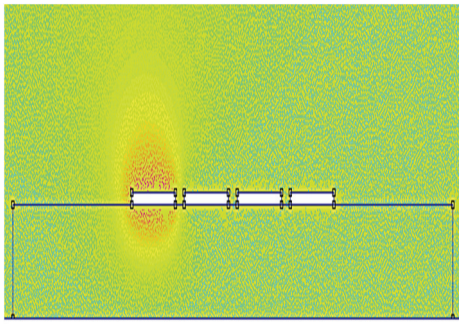


Fig. 3. Mesh of four strip conductor system.

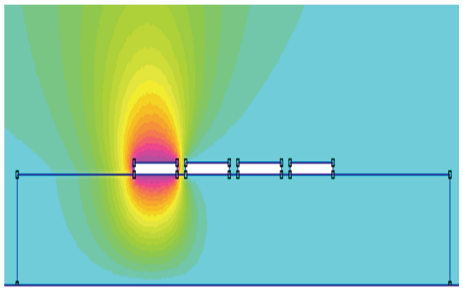


Fig. 4. Surface potential distribution of four strip conductors system.

Table 1. Capacitance matrix of the model in Fig. 2.

Capacitance (10^{-10} F/m)	Galerkin method	FEM	Our work
C_{11}	0.475	1.071	0.968
C_{12}	-0.582	-0.455	-0.328
C_{13}	-0.114	-0.112	-0.08
C_{14}	-0.062	-0.058	-0.01
C_{22}	0.289	1.127	1.112

The inductance per unit length matrix is:

$$L=\begin{bmatrix} 0.1063 & 0.0381 & 0.0220 & 0.0117 \\ 0.0381 & 0.1025 & 0.0387 & 0.0219 \\ 0.0220 & 0.0387 & 0.1025 & 0.0381 \\ 0.0117 & 0.0219 & 0.0381 & 0.1062 \end{bmatrix}.$$

The impedance per unit length matrix is:

$$Z=\begin{bmatrix} 0.3846 & 0.3182 & 0.2699 & 0.2160 \\ 0.3166 & 0.3957 & 0.3287 & 0.2706 \\ 0.2683 & 0.3286 & 0.3963 & 0.3198 \\ 0.2144 & 0.2702 & 0.3196 & 0.3884 \end{bmatrix}.$$

In the second section we consider a planar interconnects line including four strips with two levels systems, Fig. 5 shows the geometry of the model.

This microstrip coupled interconnects have the following geometrical parameters: $\omega_1=\omega_2=\omega_3=\omega_4=$ 20 μm, S = 60 μm, h = 40 μm. t = 5 μm, d =30 μm, $\varepsilon_1=11.7$, $\varepsilon_2=3.9$.

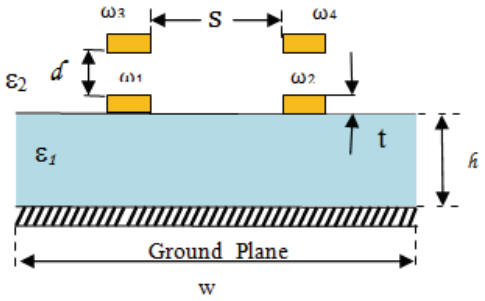


Fig. 5. Symmetric microstrip coupled interconnect with two levels systems.

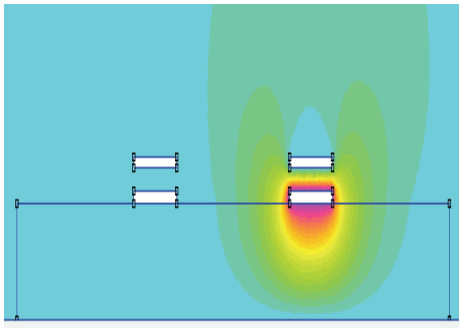


Fig. 6. Surface potential distribution of four strip conductors with two levels systems.

The capacitance per unit length of the multistrip transmission lines are related as follows:

$$C=\begin{bmatrix} 6.921 & -1.251 & -1.312 & -2.104 \\ -1.251 & 8.602 & -4.962 & -3.978 \\ -1.312 & -4.962 & 12.86 & -1.409 \\ -2.104 & -3.978 & -1.409 & 14.012 \end{bmatrix}.$$

Table 2. Capacitance matrix of the model in Fig. 5.

Capacitance (10^{-12} F/m)	MoM	FEM	Our work
C_{11}	7.158	7.210	6.921
C_{12}	-1.284	-1.323	-1.251
C_{13}	-1.296	-1.340	-1.312
C_{14}	-2.224	-2.308	-2.104
C_{22}	8.732	9.022	8.602
C_{33}	13.39	13.86	12.86
C_{44}	14.11	14.55	14.01

The inductance per unit length matrix is:

$$L=\begin{bmatrix} 0.2125 & 0.1016 & 0.0683 & 0.0676 \\ 0.1016 & 0.2619 & 0.1226 & 0.1019 \\ 0.0683 & 0.1226 & 0.1473 & 0.0599 \\ 0.0676 & 0.1019 & 0.0599 & 0.1245 \end{bmatrix}.$$

The impedance per unit length matrix is:

$$Z=\begin{bmatrix} 0.7629 & 0.7553 & 0.6077 & 0.5786 \\ 0.7553 & 0.9686 & 0.7539 & 0.6942 \\ 0.6077 & 0.7539 & 0.6359 & 0.5479 \\ 0.5786 & 0.6942 & 0.5479 & 0.5533 \end{bmatrix}.$$

In the third section we consider a planar interconnects line including nine strips with four levels systems, Fig. 7 shows the geometry of the model.

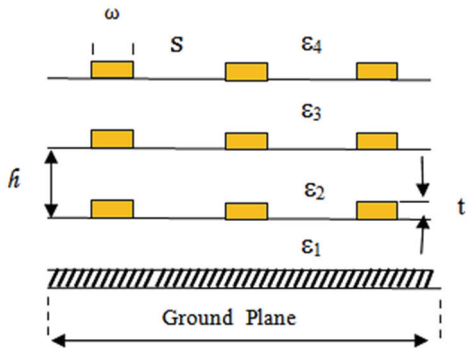


Fig. 7. Symmetric microstrip coupled interconnect with four levels systems.

This microstrip coupled interconnects have the following geometrical parameters: ω = 20 μm, S = 60 μm, h = 40 μm, t = 5 μm, $\varepsilon_1 = 11.7$, $\varepsilon_2 = 8.9$, $\varepsilon_3 = 3.9$, $\varepsilon_4 = 1$.

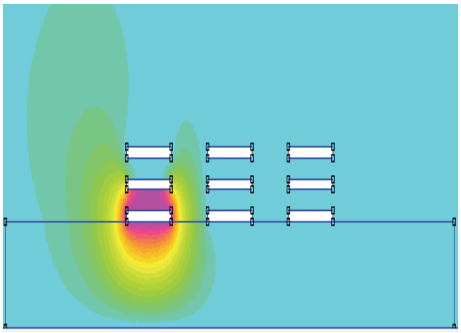


Fig. 8. Surface potential distribution of nine strip conductors with four levels systems.

Table 3. Capacitance matrix of the model in Fig. 7.

Capacitance (10^{-12} F/m)	Our work
C_{11}	4.768
C_{22}	4.389
C_{33}	4.012
C_{44}	3.673
C_{55}	3.216
C_{66}	3.051
C_{77}	2.865
C_{88}	2.654
C_{99}	2.325

Table 4. Inductance matrix of the model in Fig. 7.

Capacitance (10^{-12} F/m)	Our work
L_{11}	0.5302
L_{22}	0.4881
L_{33}	0.4462
L_{44}	0.4085
L_{55}	0.3576
L_{66}	0.3393
L_{77}	0.3186
L_{88}	0.2951
L_{99}	0.2586

In the fourth section we consider a planar interconnects line including four strips with two levels systems, Fig. 5 shows the geometry of the model.

The calculation of the matrix [C] for the given cut is made by making certain parameters vary.

The parameters studied are: t is the thickness of the track varying from 5 to 10 µm, d is the height of the oxides between two tracks, ranging from 40 to 100 µm six cases were simulated, the table below shows the values of the parameters.

Table 5.

Case 1	Case 2	Case 3
W = 20 µm S = 60 µm t = 5 µm d = 40 µm	W = 20 µm S = 60 µm t = 10 µm d = 40 µm	W = 20 µm S = 60 µm t = 5 µm d = 80 µm
Case 4	**Case 5**	**Case 6**
W = 20 µm S = 60 µm t = 10 µm d = 80 µm	W = 20 µm S = 60 µm t = 5 µm d = 100 µm	W = 20 µm S = 60 µm t = 1 µm d = 100 µm

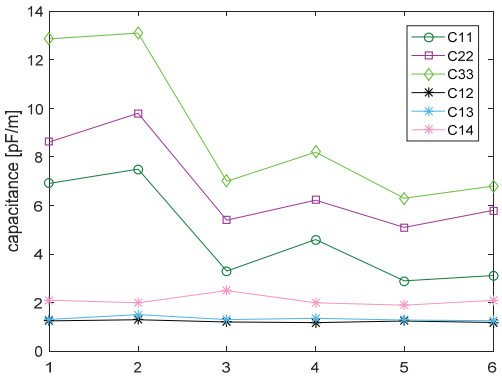


Fig. 9. Capacitance per unit length.

All abilities decrease with distance to the ground plane.

This evolution can be explained by the fact that we combine the increase of the distance between the track, in order to locate an optimum layer thickness corresponds to the thickness for which the parasitic capacitance-to-capacitance ratio mass is the lowest.

3. Conclusions

In this paper we have identified the potential distributor for four interconnect transmission lines and we computed the capacitance matrix. The results obtained in this research to comply with literature and motivating for the future study.

References

[1]. H. Ymeri, B. Nauwelaers, K. Maex, D. De Roest, S. Vandenberghe, M. Stucchi, Admittance matrix calculations of on-chip interconnects on lossy silicon substrate using multilayer green's function, in *Proceedings of Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Digest of Papers*, Sept. 2001, pp. 192-200.

[2]. H. Ymeri, B. Nauwelaers, K. Maex, D. De Roest, S. Vandenber, New analytic expression for mutual inductance and resistance of coupled interconnects on lossy silicon substrate, in *Proceedings of Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Digest of Papers*, September 2001, pp. 7803-7129.

[3]. S. M. Musa, M. N. O. Sadiku, K. T. Harris, Modeling of multiconductor microstrip systems on microwave integrated circuits, in *Proceedings of the COMSOL Conference in Boston*, 2013.

[4]. L. Shujing, Z. Hanqing, An efficient algorithm for the parameter extraction of multiconductor transmission lines in multilayer dielectric media, in *Proceeding of the IEEE Antennas and Propagation Society International Symposium,* July 2005, Vol. 3A, pp. 228-231.

[5]. M. K. Amirhosseini, A. Cheldavi, Time domain analysis of circulant symmetric coupled transmission lines, *IEEE Proceedings of Microwaves,* Vol. 150, Issue 5, Oct. 2003, pp. 325-331.

[6]. W. Shu, S. Xu, Capacitance extraction for multiconductor transmission lines in multilayered dielectric media using the numerical green's function, *Microwave and Optical Letters,* Vol. 40, Issue 6, 2006, pp. 529-531.

[7]. H. Ymeri, B. Nauwelaers, K. Maex, D. De Roest, A new approach for the calculation of line capacitances of two-layer IC interconnects, *Microwave Theory and Optical Technology Letters*, Vol. 27, Issue 5, 2000, pp. 297-302.

[8]. M. S. Lin, Meseared capacitance coefficients of multiconductor microstrip lines with small dimensions, *IEEE Transactions on Microwave Theory and Techniques,* Vol. 13, Issue 4, 1990, pp. 1050-1054.

[9]. M.-S. Lin, Measured capacitance coefficients of multiconductor microstrip lines with small dimension, *IEEE Transactions on Component. Hybrids, and Manufacturing Technology,* Vol. 13, Issue 4, 1990, pp. 1050-1054.

[10]. Z. Q. Ning. P. M. Dewilde, F. L. Neerhoff, Capacitance coefficients for VLSI multilevel metallization lines, *IEEE Trans. Electro. Devices,* Vol. 34, 1987, pp. 644-649.

[11]. C. D. Taylor, G. N. Elkhori, T. E. Wade, On the parasitic capacitances of multilevel parallel metallization lines, *IEEE Trans. Electro. Devices*, Vol. 32, 1987, pp. 2408-2414.

(008)

Simultaneous Read/Write Nanoelectronic SRAM with Shared Write Bit-Line Scheme

B. O. Câmara [1], J. G. Guimarães [2] and J. C. da Costa [1]
[1] Universidade de Brasília, Department of Electrical Engineering, P.O.Box 4386, Brasília, Brasil
[2] Universidade Federal de Santa Catarina, Engineering Department, Rua João Pessoa 2750, Blumenau, Brasil
E-mail: bia.camara@gmail.com

Summary: This work proposes and validates a new, fully working single-electron transistor (SET) based SRAM with individual read and write addressing for simultaneous operation. The SET-based SRAM presents smaller area and lower power consumption, making it ideal for devices with small area and low power consumption demands such as Systems-on-Chip (SoCs).

Keywords: SRAM, SET, Nanoelectronics.

1. Introduction

The capability of storing and retrieving large amounts of information is essential for most modern digital systems. The structured storing of bits, usually as a two-dimensional array, is defined as a memory [1]. One of the types of memories used in modern systems is the Random-Access Memory (RAM). The RAM is a volatile read/write memory in which the access time for read and write operations is independent of the data location in the memory array. The Static RAM (SRAM) is a type of RAM in which the written data remains stored as long as there is power applied to the system.

Area and dissipated power are limiting factors in improving the performance of mobile and Systems-on-Chip (SoCs) devices [2]. 70 % of the area of a SoC chip is occupied by the SRAM memory [3]. Using a nanoelectronic device instead of CMOS transistors within the SRAM could be the solution to these limitations.

Particularly the single-electron transistor (SET) present attractive features like reduced dimensions, extremely low power consumption and low noise behavior. Single-electronic devices are able to control the movement of individual electrons through the tunneling phenomenon, i.e., the nonzero probability that the electron will be transmitted through a potential energy barrier [4].

This work proposes a new and fully working nanoelectronic SRAM based on the SET transistor and with individual read and write addressing.

2. Single-Electron Transistor

The SET consists of two tunnel junctions connected together, forming an island between them [5]. Its operation is based on the flow control of single electrons by tunneling. That leads to very low power consumption. The gate voltage manipulates the Fermi level, i.e., the highest energy level occupied on the island, thus controlling the electrons conduction through the transistor [6].

The operation of SETs up to 350 K has already been reported [7]. In this work, a SPICE model for the SET, which operates at room temperature, proposed by and available at Lientsching *et al.* [8] was employed.

3. SRAM Architecture

A generic SRAM architecture (Fig. 1) is composed of storing cells, read and write control and address logic. The cells store 1 bit in a latch or flip-flop device and are usually arranged in an $m \times n$ matrix, where m corresponds to the number of words that can be stored in the memory, and n represents the number of bits each word contains. They also contain the read/write logic and a select control that enables the operation of each cell. The address logic allows each word of the memory matrix to be selected individually.

The developed SRAM can store 8 words of 8 bits and presents separate controls for read and write addressing, allowing an individual and simultaneous execution of these operations (Fig. 2). All the components of this digital architecture were designed with a nanoelectronic gate (nanoNAND) as base element (Fig. 3). This nanoNAND gate consists of four SET transistors [9]. All simulations were made using the LTSpice software [10]. Its building blocks are briefly presented in the next subsection.

3.1. SRAM Cell and Array

The SRAM cell consists of a flip-flop D, which can store 1 bit. The cells are arranged in an array of 8 bits, constituting a word. Each array consists of the 8 bits entries, a clock and an asynchronous clear, read and write signals to indicate the operation and independent select signals for each operation, which are used by the addressing logic (Fig. 4).

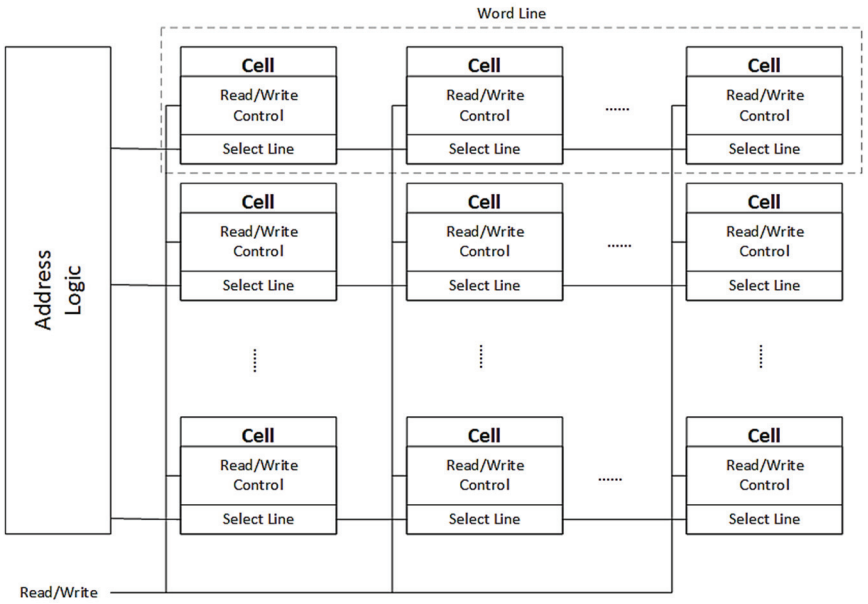


Fig. 1. Generic SRAM architecture.

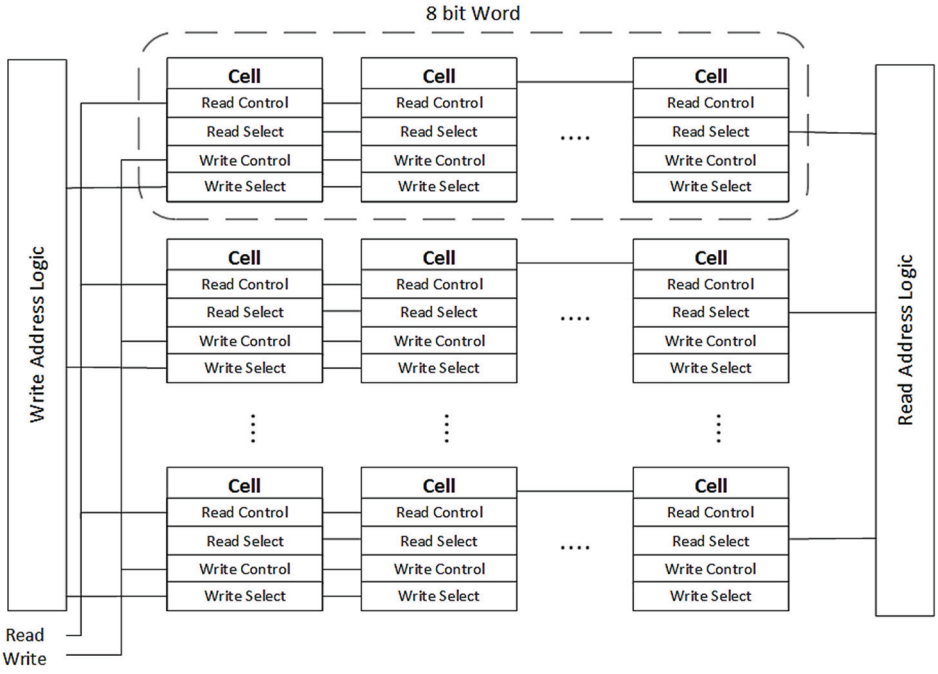


Fig. 2. SRAM architecture.

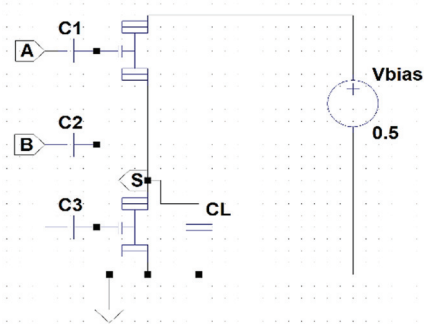


Fig. 3. NanoNAND schematic.

In order for the read/write operation to occur in the m^{th} word, both the corresponding operation signal and operation address should be selected in the m^{th} array. Because it is possible to realize a simultaneous read and write operation in the same array, an unstable situation could be reached in the output. To avoid this problem both operations are also regulated by the system's clock. The write operation is executed only during the rising of the clock signal, while the read operation is executed when the clock signal is low.

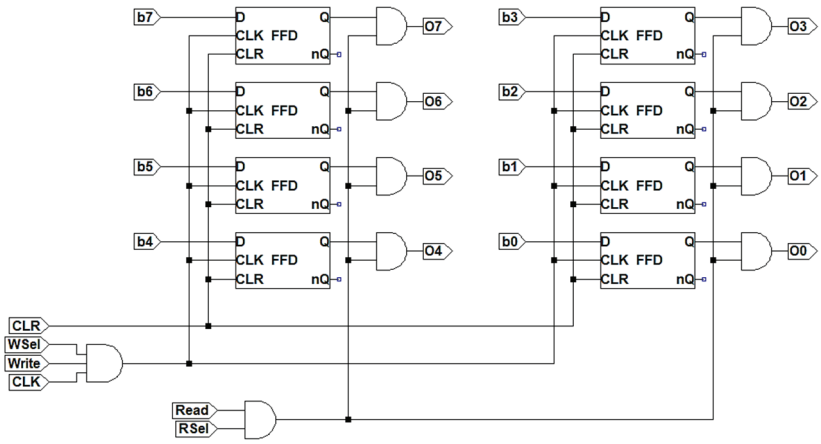


Fig. 4. SRAM array.

3.2. Read and Write Addresses

Because the proposed SRAM contains 8 memory arrays (words), read and write addressing are done through separated 3 to 8 decoders. An array address is then a 3-bit number that should be input in the corresponding operation decoder.

4. Simulation

The simulations were done through the software LTSpice. In this phase a test was presented to evaluate the correct functioning of the SRAM. The test consisted of writing two different 8-bit words on address 3 and 7 (Table 1), respectively, and retrieving them later.

Table 1. Words for SRAM testing.

Add.	b7	b6	b5	b4	b3	b2	b1	b0
3	1	0	0	1	0	1	1	1
7	1	1	0	1	1	0	0	1

The simultaneous read/write feature was also assessed during the test. Table 2 presents a timetable for when the write and read actions occurred and what addresses they accessed.

Table 2. Read/Write actions timetable.

Time (ms)	Write Action	Write Address	Read Action	Read Address
0-0.5	1	3	0	-
0.5-1	0	-	1	3
1-1.5	1	7	1	7
1.5-2	0	-	1	7

5. Results

The results of the test presented during simulation shows that the nanoelectronic SRAM works correctly. The write, read, addressing and simultaneous read/write functions perform as expected, as shown on Fig. 5 (a, b).

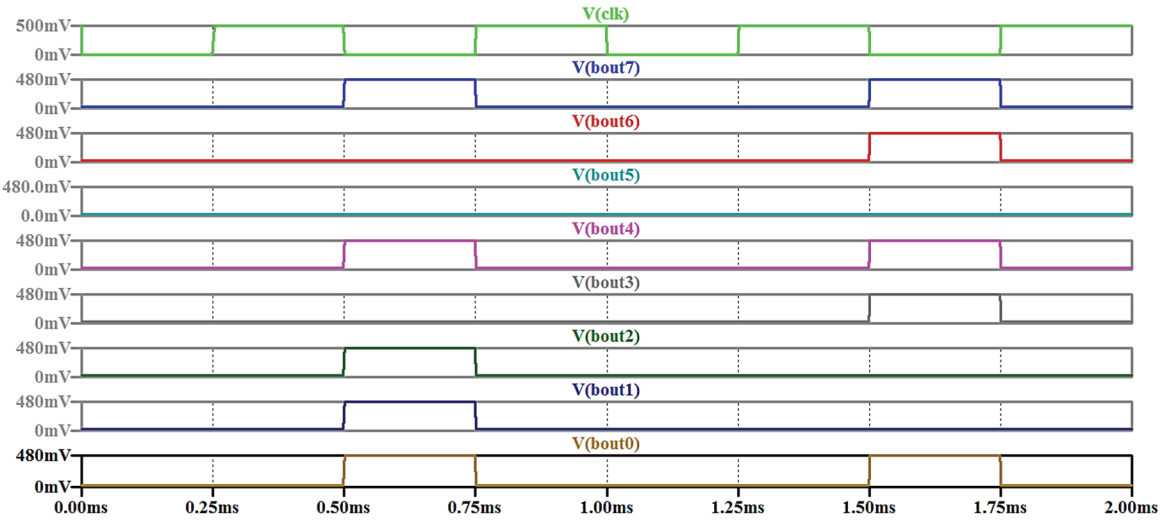


Fig. 5 (a). SRAM simulation.

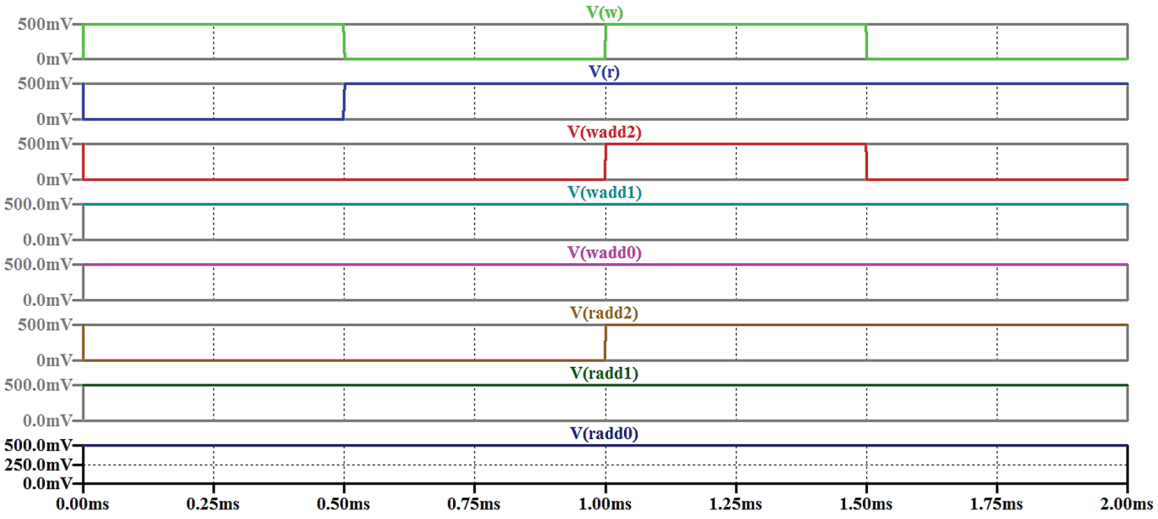


Fig. 5 (b). SRAM simulation.

The complete nanoelectronic SRAM has a total of 1890 nanoNANDs. The area of 1 nanoNAND is 172 nm² and 3.5 pW [9] and its dissipated power can be calculated by using equations 1 to 3. The total dissipated power is given by the sum of the static and dynamic powers. Table 3 presents the values for area and dissipated power for 1 nannoNAND, 1 array (word), 1 decoder, and the complete SRAM.

$$P_{dissipated} = P_{static} + P_{dynamic}, \quad (1)$$

$$P_{static} = V_{dd} \times I_{max}, \quad (2)$$

$$P_{dynamic} = f \times {V_{dd}}^2 \times C_L. \quad (3)$$

The complete SRAM has an area of 0.325 µm² and dissipates 6.6 nW, which highlights the advantages of a nanoelectronic SRAM.

Table 3. SRAM area and dissipated power.

	#SET NAND	Area	Power
nanoNAND	1	172 nm²	3.5 pW
Array	206	35432 nm²	721 pW
Decoder	37	6364 nm²	129.5 pW
SRAM	1890	0.325 µm²	6.6 nW

6. Conclusions

This work presented and validated the proper working of a completely nanoelectronic SRAM. This new approach solves the area and power consumption limitations that current applications face. Also, the new architecture provides the possibility of a separate read and write addressing, allowing for more versatile applications.

Acknowledgements

The authors would like to thank CAPES, PQ/CNPq and INCT-NAMITEC for support.

References

[1]. J. F. Wakerly, Digital Design: Principles and Practices, *Prentice Hall*, 2000.

[2]. N. Gupta, A. Makosiej, A. Vladimirescu, A. Amara, C. Anghel, Tunnel FET based ultra-low-leakage compact 2T1C SRAM, in *Proceedings of the 2017 18th International Symposium on Quality Electronic Design (ISQED'17)*, 2017, pp. 71-75.

[3]. S. Raju, K. Jeevan Reddy, Design and implementation of 8×8 DRAM memory array using 45 nm technology, *Int. J. Adv. Technol. Eng. Sci*., Vol. 3, Issue 1, 2015, pp. 443-451.

[4]. G. W. Hanson, Fundamentals of Nanoelectronics, *Pearson/Prentice Hall*, 2008.

[5] D. V. Averin, K. K. Likharev, Coulomb blockade of single-electron tunneling, and coherent oscillations in small tunnel junctions, *J. Low Temp. Phys*., Vol. 62, Issues 3-4, Feb. 1986, pp. 345-373.

[6]. H. Grabert, M. H. Devoret, Single Charge Tunneling: Coulomb Blockade Phenomena In Nanostructures, 1st Ed., *Springer*, 1992.

[7]. R. Lavieville, S. Barraud, A. Corna, X. Jehl, M. Sanquer, M. Vinet, 350 K operating silicon nanowire single electron/hole transistors scaled down to 3.4 nm diameter and 10 nm gate length, in *Proceedings of the Joint International Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS'15)*, 2015, pp. 9-12.

[8]. G. Lientschnig, I. Weymann, P. Hadley, Simulating hybrid circuits of single-electron transistors and field-effect transistors, *Jpn. J. Appl. Phys*., Vol. 42, Oct. 2003, pp. 6467-6472.

[9]. L. Silva, J. G. Guimarães, Performance analysis of single-electron NAND gates, *ECS Transactions*, Vol. 23, 2009, pp. 311-318.

[10]. Linear, Linear Technology – Design Simulation and Device Models, http://www.linear.com/designtools/software/#LTspice.

(009)

Modeling GaAs MESFET's Using Finite Elements Method

M. Djouder [1], A.Benfdila [1] and A. Lakhlef [2]
Microelectronics and Nanotechnology Research Group GRMNT, FGEI,
University M. Mammeri, Tizi-Ouzou, Algeria
E-mail: benfdila@ummto.dz

Summary: This paper deals with the simulation of the MESFET transistor (Metal semiconductor Field-Effect Transistor), reducing size geometrical parameters 1-µm GaAs MESFET with a 0.3-µm gate length, the transconductance value is 80-mS for VDs = 0.2 V and the conductance is 260-mS/V for VGs = -0.2 V and The evolution of the Drain-Source current IDs = f(VDs, Vgs) in GaAs microwave MESFET's devices versus frequency domain are presented, The transport properties of the device are dominated by electrons (majority carriers). we introduce the finite elements method, we will consider the substrate doped p-type Na = 1.e10[1/cm3] and channel doped Nd = 1e16[1/ cm3], the interest of this simulation is to record the I-V Characteristics, the output transconductance Gd, output conductance Gm and channel resistance simulated in the frequency domain from 100 GHz, the transconductance and drain current on the gate voltage this resultants are in good agreement for RF power transistors.

Keywords: MESFET's, Output transconductance, Output conductance frequency, Finite elements.

1. Introduction

MESFET GaAs metal semiconductor field effect transistors (MESFETs) with submicron channel lengths can operate comfortably at a frequency greater than 100 GHz [1], used in microwave applications, and a height speed digital circuits point of view their superior height frequency [2-5]. High frequency devices, cellular phones, satellite receivers, radar. The simplest way to enhance the performance of the device is to reduce the gate length [3], a high gm 375 mS/mm (Vth = -0.09 V) has been achieved from 0.3 long gate GaAs MESFET with a very small short channel [4]. In this paper we are interest to simulate this device record the I-V Characteristics, The active channel region of the device is an N-GaAs layer that can be obtained by ion-implanting Si into semi-insulating substrate [6]. The small channel depth requires that the carrier concentration in the channel be as high as possible to maintain a high current.

For MESFET's with a 1-um gate length, domain formation is expected to take place if the pinchoff voltage exceeds 1.5 V [7], In our simulation, the n-type doping concentration is Nd 1e16/cm3, the affinity level of GaAs is 4.07 eV, the band gap of GaAs is 1.42 eV, to obtains the I-V Characteristics and the different Output-Conductance Gm and the Output Transconductance Gd. at first time we varying the VGs voltage and VDs voltage taking into account two important parameters such as the length of the gate Lg and the doping of the channel Nd concentration respectively to see the impact of these parameters on the electrical characteristics of this MESFET GaAs device and, the second party we simulated and we studied how to operate at variable frequencies going up to 100 GHz then we fixed at freq-T = 40 GHz.

1.1. Schematic Structure Basic and Parameters for MESFET Transistor

The basic device structure taking in this simulation shown in Fig. 1. The substrate considered to be semi insulating p-doped.

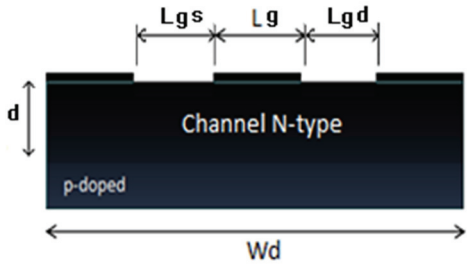


Fig. 1. MESFET Physical Structure.

The electrical parameters for device of the 1 [µm] MESFET presented in Table 1.

Table 1. Parameters structure for MESFET.

Parameters	MESFET 1-[µm]	Unites
Lg	0.3	[µm]
Nd	1.10^{16}	[1/cm^3]
Na	1.10^{10}	[1/cm^3]
d	0.25	[µm]
Lgd	0.15	[µm]
Lgs	0.15	[µm]
Vbi	0.87	[v]
Vsat	1.2×10^7	[cm/s]

2 Resultats for Simulation

2.1. Device DC Characteristics

The Simulations are achieved on MESFETs using different types of curves in order to emphasize on the device performances.

The I-V Characteristics IDs = f (VDs,VGs) for a device obtained by simulation are presented in Figs. 2-7.

Typical curves are given through Figs. 1 to 5 to illustrate the behavior of the device in conjunction to electrical parameters. These curves obtained using the Finite element method allow the possible introduction of graphene material for possible succession to GaAs, which is the goal of our study.

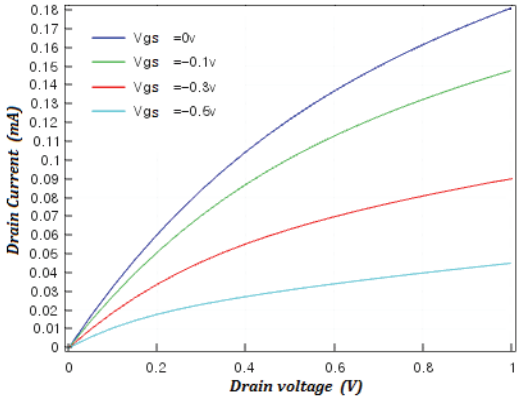


Fig. 2. The I-V Characteristics IDs–VDs **for** MESFET, gate voltage bias VGs varying 0 to -0.5 V by step 0.1 V.

In the Fig. 2 we presented the characteristics obtained by the simulation of the device. These characteristics illustrate the relation between the drain current Ids and the drain voltages V_{ds}.

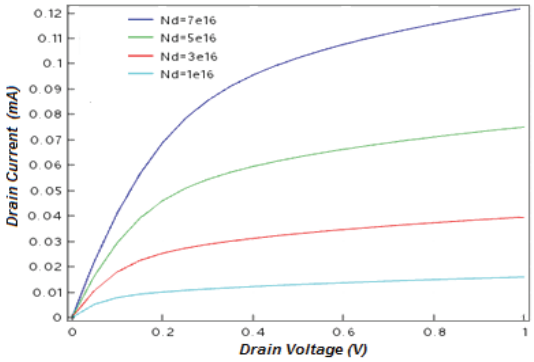


Fig. 3. The I-V Characteristics IDs–VDs for MESFET, gate voltage bias VGs -0.1 V by step 0.1 V changing the canal doping Nd Concentration.

The Fig. 3 As shown in the IDS-VDS characteristics for different gate voltage, we see that the drain current becomes almost zero at about Nd = 1e16 [1/cm^3] and important value a drain current at Nd = 7e16 [1/cm^3] for the device.

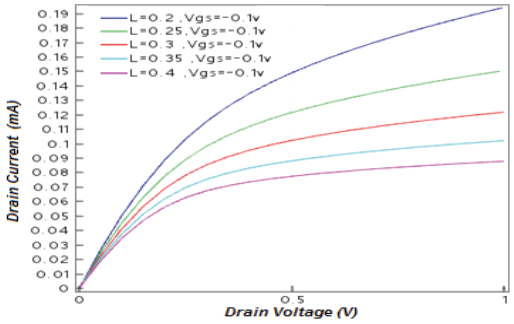


Fig. 4. The I-V Characteristics IDs–VDs for MESFET, gate voltage bias VGs -0.1 V by step 0.1 V with different values Gate length Lg.

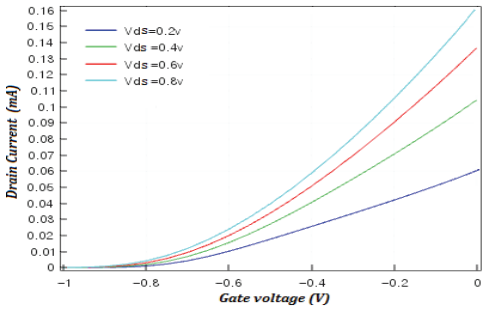


Fig. 5. Output I-V Characteristics IDs–VGs for MESFET, drain voltage bias VDs varying between 0.2 to 0.8 V.

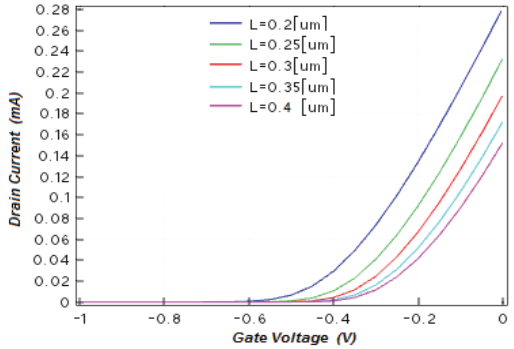


Fig. 6. Output I-V Characteristics IDs–VGs for MESFET, drain voltage bias VDs is fixed to 0.6 V, canal doping Concentration N = 2e16 [1/cm3], we varying gate length Lg.

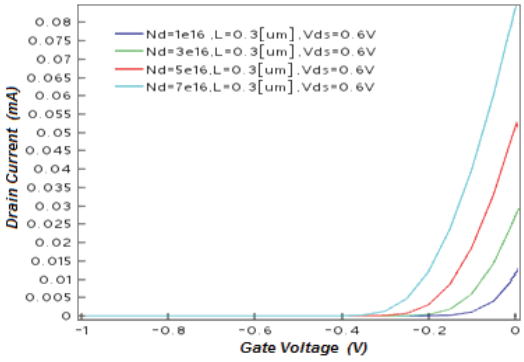


Fig. 7. Output I-V Characteristics IDs–VGs for MESFET, drain voltage bias VDs is fixed to 0.6 V, Gate length and changing the canal doping Nd Concentration.

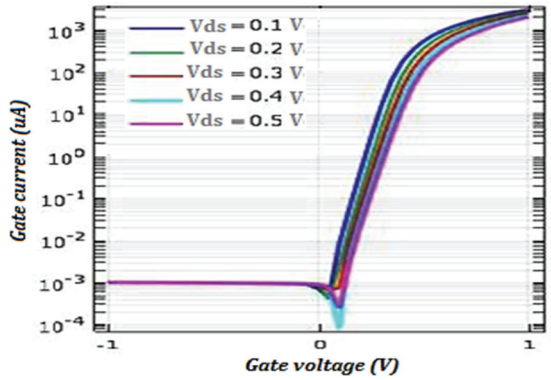


Fig. 8. Schottky Gate I-V Characteristics IGs-VGs on a semi-log plot VDs varying between 0.1 to 0.5 V by step 0.1 V.

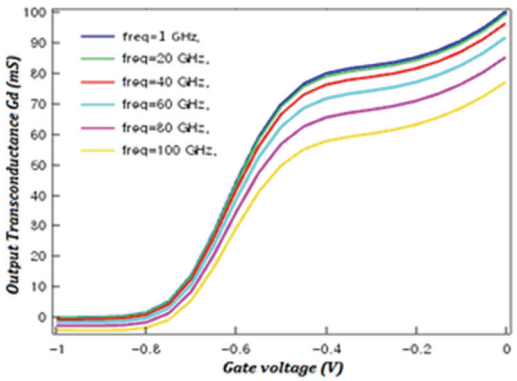


Fig. 10. Variation in transconductance as a function of gate-source voltage at different frequencies-perturbation domain VDs fixed in 0.2 V.

2.2. Output Transconductance, Output Conductance and Resistance

The transconductance of the MESFET is defined by a variation ratio of the drain-source current (IDs) by drain-source voltage (VGS), as well as the conductance obtained by the variation of the IDs by gate-source voltage (VGs).

Fig. 9 represents the drain conductance a function of the drain voltage VDs for different values of frequency. We notice that the drain conductance is decreases on the one hand as the drain voltage increases its maximum value in linear regime, and is minimal in regime of saturation.

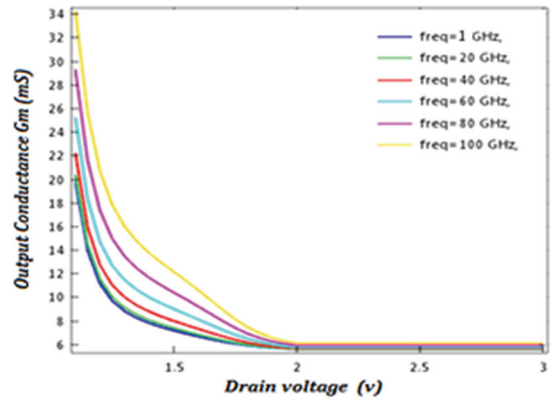


Fig. 9. The Variation Output conductance as a function of drain-source voltage varying 0.1 V to 3 V by step 0.05 V VGs fixed -0.2 V at different frequencies-perturbation domain.

Fig. 10 presented the transconductance as a function of the Gate voltage VGs for a different of frequency. In this figure, we noticed that the transconductance increases on the one hand as the absolute value of the frequency decreases.

Fig. 11 represent the drain output conductance a function of the drain voltage for different values of Gate voltage VGs. We noticed that the drain conductance is decreases on the one hand as the drain voltage increases its maximum value in linear regime, and is minimal in regime of saturation.

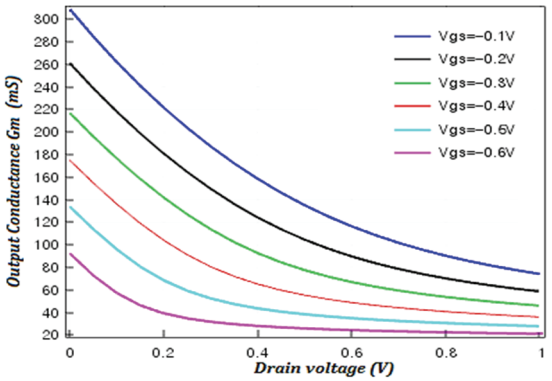


Fig. 11. Output conductance as a function of drain-source voltage varying VGs between -1 to 0 V, frequencies fixed freq-T fixed 40 GHz.

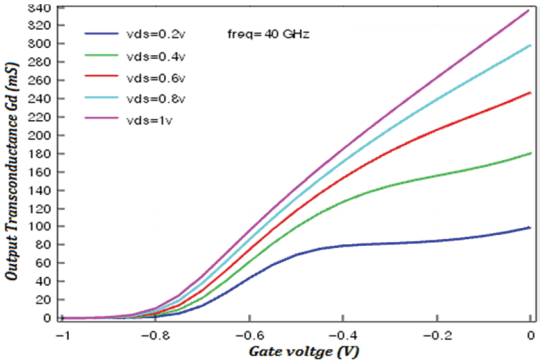


Fig. 12. Variation in Transconductance as a function gate-source voltage, VDs varying between 0.2 to 1 V by Steps 0.2, freq-T fixed 40 GHz.

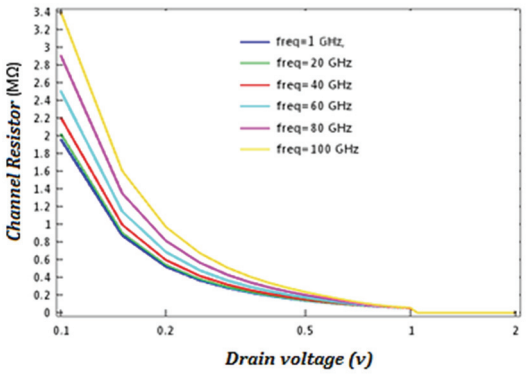


Fig. 13. Variation in Resistance as a function of Drain-source voltage at different frequencies, VGs fixed -0.2 V.

4. Conclusion

During this work, we simulate the MESFET GaAs transistor. At first we studied how to operate at variable frequencies going up to 100 GHz, then we fixed at freq-T = 40 GHz, we revealed the characteristics gm and Gd. In order to obtain the performance characteristics I-V of a device with a length of 1 µm, simulating the DC characteristics of short-gate GaAs MESFETs. Transconductance and conductance curves obtained by simulations are found similar to those of short-channel MESFETs.

We have shown the applicability of the finite element method in order to find an approach to introduce Graphene MESFETs as we reported in our earlier work.

References

[1]. M. M. Ahmed, H. Ahmed, P. H. Ladbrook, An improved method to estimate intrinsic small signal parameters of a GaAs MESFET from measured DC characteristics, *IEEE Trans. on Electron Devices*, Vol. 50, Issue 11, 2003, pp. 2196-2201.

[2]. H. A. Hung, *et al.*, V-band GaAs MMIC low-noise and power amplifiers, *IEEE Trans. Microwave Theory Tech.,* Vol. 36, 1988, pp. 1966-1975.

[3]. M. M. Ahmed,, Schottky barrier depletion modification – A source of output conductance in submicron GaAs MESFETs, *IEEE Transactions on Electron Devices,* Vol. 48, Issue 5, 2001, pp. 830-834.

[4]. K. Ueno, T. Furutsuka, H. Toyoshima, M. Kanamori, A. Higashisaka, A high transconductance GaAs MESFET with reduced short channel effect characteristics, in *Proceedings of the International Electron Devices Meeting,* 1985, pp. 82-85.

[5]. P. R. H. Riemenschneider, K. L. Wang, A finite-element program for modeling transient phenomena in GaAs MESFET's, *IEEE Transactions on Electron Devices,* Vol. 30, Issue 9, 1983, pp. 1142-1150.

[6]. S. Tripathi, S. Jit, Analytical modelling of the current (I)–voltage (V) characteristics of sub-micron gate-length ion-implanted GaAs MESFETs under dark and illuminated conditions, *IET Circuits Devices Syst.,* Vol. 7, Issue 1,2013, pp. 42-50.

[7]. T. A Fjeldly, Analytical modeling of the stationary domain in GaAs MESFET's, *IEEE Transactions on Electron Devices,* Vol. 33, 1986, pp. 874-880.

(010)

Increasing the Dielectric Constant of HfO_2 in MIS Structures, by Thermal Annealing Right after Deposition of the Dielectric Layer

I. S. Hernández, S. I. Garduño, and M. Estrada
Section of Solid State Electronics, Electric Engineering Department, Center of Research and Advanced Studies of the National Polytechnic Institute, 2208 IPN Av., 07360 CDMX, Mexico
E-mail: ihernandezl@cinvestav.mx

Summary: A significant increase in the dielectric constant of hafnium oxide (HfO_2) layers deposited by room temperature radio frequency magnetron sputtering is observed after thermal annealing the samples in O_2 at 200 ºC, right after the deposition of the layer. Metal-Insulator-Semiconductor (MIS) structures, using (HfO_2) as dielectric and amorphous Hafnium-Indium-Zinc oxide as semiconductor, were characterize using capacitance-voltage (CV) and current voltage (IV) characteristics. It was observed that the dielectric constant increased from around 29 in the un-annealed to around 45 in the annealed, while maintaining the breakdown voltage and leakage current density in satisfactory values. Results obtained were used to fabricate AOSTFTs working in the operating voltage range below 5 V with mobility values above 4 cm^2/Vs.

Keywords: Amorphous Oxide Semiconductors, Hf-In-ZnO (HIZO), High-*k* gate dielectrics, Thermal annealing treatment.

1. Introduction

Amorphous oxide semiconductor thin film transistors (AOSTFTs) have attracted interest due their high mobility values and optical transparency that allow their application as switching and/or driving elements in flat-panel displays. They are fabricated using low temperature (<200 °C) and conventional deposition techniques [1, 2]. To increase the carrier mobility and improve the electrical stability of TFTs based on zinc oxide (ZnO) as active layer, binary components as indium oxide (In_2O_3), gallium oxide (Ga_2O_3) and hafnium oxide (HfO_2), have been incorporated to the ZnO structure [1, 2]. On the other hand, using insulating layers with dielectric constants higher than silicon oxide allows to reduce the operation voltage range of AOSTFTs [1, 2].

The AOSTFTs performance strongly depends on the materials used in the device structure and on the deposition techniques [2, 3]. To improve the electrical features, thermal annealing processes are also used [4].

Recently in [5], we presented the characterization of MIS structures and TFTs using HfO_2 and Hf-In-ZnO (HIZO) layers, both deposited by room temperature radio-frequency (RTRF) magnetron sputtering. However, to improve the electrical features of devices based on the HfO_2/HIZO interface, including an annealing process in the technological fabrication sequence is very important, as shown in [4].

In this work, we present the influence of annealing treatment and significant increase of the HfO_2 dielectric constant (*ki*) in metal-insulator-semiconductor (MIS) structures, using HfO_2 as dielectric and HIZO as semiconductor that can be obtained after annealing the samples right after the deposition of the dielectric layer.

2. Experimental Details

MIS capacitors were fabricated on corning glass substrate. Subsequently, molybdenum (Mo), 100 nm thick, was deposited by RTRF magnetron sputtering. As the dielectric layer, 150 ± 5 nm layer of HfO_2 was deposited by RTRF magnetron sputtering, at 20 mTorr in argon (Ar) and 5.7 W/cm^2 of power density. As semiconductor layer, 35±2 nm of HIZO were deposited by RTRF magnetron sputtering at 8 mTorr in Ar and 3.9 W/cm^2 of power density. Using a HfO_2:In_2O_3:ZnO target with the ratio of 0.3:1:1 at mol % and 99.98 % of purity. The results showed in this work correspond to unannealed sample and used as reference (Sample A). Sample with thermal annealing was done at 150 ± 2 ºC, in nitrogen (N_2) for 1 hr, after HIZO layer deposition (Sample B). Sample with annealing was carried out in O_2 at 200 ± 2 ºC for 20 min, immediately after HfO_2 deposition (Sample C). Finally, 200 nm of Mo were deposited by RTRF magnetron sputtering. All layers were patterned using standard lithography, see Fig. 1.

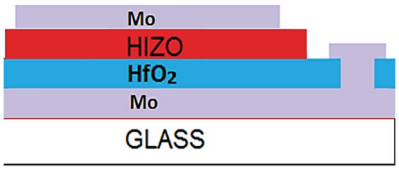


Fig. 1. MIS capacitors structure.

Layer thickness was measured by ellipsometry. Capacitance-voltage (CV) and current-voltage (IV) curves were obtained using the Agilent E4980A LCR meter and Keythley measurement system, respectively.

3. Results and Discussion

Fig. 2 shows CV curves corresponding to samples A, B, and C. The characteristic of samples A and B are almost identical, which indicates that thermal annealing at the above-mentioned conditions does not produce much variation on the capacitance. On the other hand, for sample C, the value of the capacitance in accumulation increased which gives an increase to values of *ki* (see Table 1). This significant increase in the *ki* may be attributed to a short-range ordering of the amorphous atomic structure during HfO_2 layer annealing [6].

The breakdown voltage for all samples was above 6 V. The leakage current at 3 V for sample C was 4×10^{-7} A/cm^2, while for sample A was 1×10^{-7} A/cm^2. This slight increase is expected due to the increase in the *ki* [7]. CV curve transition from depletion to accumulation is in the interval between -3 and 3 volts, indicating that devices with this MIS structure can operate in a voltage range below 5 V.

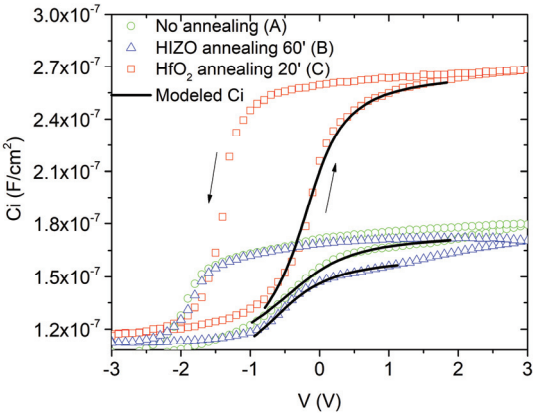


Fig. 2. CV curves of samples A, B and C at 1 kHz.

Table 1. Extracted and modeled parameters.

Sample	*ki* (1 kHz)	V_{FB} (V)	N_B (cm^{-3})	N_{SS} (cm^{-2})	V_H (V)
A	29	0.2	5.75×10^{1}	4.90×10^{1}	1.5
B	28.8	0.0	2.66×10^{1}	1.86×10^{1}	1.6
C	45	0.1	3.49×10^{1}	6.55×10^{1}	1.3

Parameters extracted from the CV curves are shown in Table 1 and modeled see Fig. 2. Fig. 2 also shows a hysteresis loop of less than 1.6 V at 1 kHz, for the CV curves swept in both directions. Despite the higher *ki*, sample C shows the smallest voltage loop, which can be due to the behavior of the dielectric dipoles for a better short-range ordering of the HfO_2.

The frequency dispersion of the capacitance in accumulation (Cr), measured at 3 V, is shown in Fig. 3. Samples A and B in the measured frequency range, this demonstrates that thermal annealing at above-mentioned conditions does not produce a variation on *ki*. On the other hand, sample C has a sharp dispersion over the highest frequencies as a probable consequence of the *ki* increase.

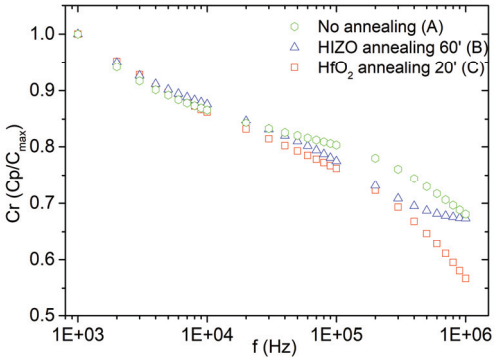


Fig. 3. Frequency dispersion of samples A, B, and C.

Finally, Fig. 4 shows the output characteristic of AOSTFT fabricated using the MIS structure corresponding to sample C with W = 200 µm and L = 40 µm, confirming the reduction of the voltage operation range to less than 3 V, V_T was 0.5 V and mobility higher around 4 cm^2/Vs.

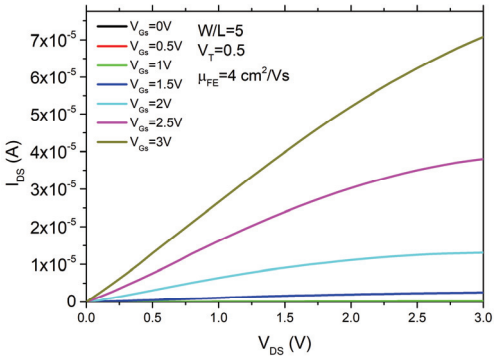


Fig. 4. Output characteristic of AOSTFT.

4. Conclusions

The HfO_2/HIZO MIS capacitors, fabricated with annealing in O_2 at 200 °C during 20 min, right after HfO_2 deposition layer showed a significant increase in *ki* from 29 to 45, while maintaining the rest of the structure parameters. The increase in *ki* is important to reduce the operating voltage of the devices fabricated with this high-k dielectric, which is shown in AOSTFTs fabricated with the analyzed MIS structure.

Acknowledgements

This work was supported by CONACyT project 237213. S.I. Garduño specially acknowledges to CONACyT project "Cátedras CONACyT para Jóvenes Investigadores". We also acknowledgement Ing. Luis Abad for the devices fabrication.

References

[1]. E. Fortunato, P. Barquinha, R. Martins, Oxide semiconductor thin-film transistors: A review of recent

advances, *Advanced Materials*, Vol. 24, Issue 22, 2012, pp. 2945-2986.

[2]. H. Kumomi, T. Kamiya, H. Hosono, Advances in oxide thin-film transistors in recent decade and their future, *ECS Transactions*, Vol. 67, Issue 1, 2015, pp. 3-8.

[3]. C.-J. Kim, S. Kim, J.-H. Lee, J.-S. Park, S. Kim, J. Park, E. Lee, J. Lee, Y. Park, J. H. Kim, S. T. Shin, U-I. Chung, Amorphous hafnium-indium-zinc oxide semiconductor thin film transistors, *Applied Physics Letters*, Vol. 95, Issue 25, 2009, pp. 1-3.

[4]. L. X. Qian, P. T. Lai, Improved performance of InGaZnO thin-film transistor with HfLaO gate dielectric annealed in oxygen, *IEEE Transactions on Device and Materials Reliability*, Vol. 14, Issue 1, 2014, pp. 177-181.

[5]. I. Hernandez, C.A. Pons-Flores, I. Garduño, J. Tinoco, I. Mejia, M. Estrada, Characterization of MIS structures and thin film transistors using RF-sputerred HfO_2/HIZO layers, *Microelectronics Reliability*, Vol. 75, Issue 1, 2017, pp. 9-13.

[6]. F. M. Li, B. C. Bayer, S. Hofmann, J. D. Dutson, S. J. Wakeham, M. J. Thwaites, W. I. Milne, A. J. Flewitt, High-k (k = 30) amorphous hafnium oxide films from high rate room temperature deposition, *Applied Physics Letters*, Vol. 98, 2011, 252903.

[7]. J. W. McPherson, J. Kim, A. Shanware, H. Mongul, J. Rodriguez, Trends in the ultimate breakdown strengh of high dielectric-constant materials, *IEEE Transactions on Electron Device*, Vol. 50, 2003, pp. 1771-1778.

(011)

Study and Simulation of Degradation of MOS Transistor Using Silvaco Athena and Matlab

N. Guenifi, R. Mahamdi and T. Chenaf
Department of Electronics, University Mostefa Benboulaid of Batna, Algeria
E-mail: guenifi_2000@yahoo.fr

Summary: In this paper, our work focuses on the impact of P_b centers on the reliability of transistor MOS, therefore, we have implementated a theoretical model. The model takes into account the P_b centers is solved using the engineering software tool MATLAB. The results found show that the P_b centers are responsible of the derive of the electrical characteristics of the TMOS, from the density of P_b centers greater than 10^{11} / cm^2. But, for the density of P_b centers less than 10^{11} cm^2 there is a negligible influence on the fiability of the TMOS. In this article we also show, by the study of static characteristics, the influence of geometrical and electrical parameters on the degradation phenomena. Our results are compared with those already simulated using electrical simulator SMARTSPICE level 3 model. A good agreement is observed between both methods. Also, energy distribution of the P_b centers in the semiconductor band and their capture cross section were analyzed through a computer simulation software from Silvaco.

Keywords: P_b centers, Interface states Si/SiO_2, TMOS, Silvaco, MOSFET degradation.

1. Introduction

Interface traps, also known as interface states, exist at the SiO_2/Si interface. They are the result of a structural imperfection. Interface traps, also known as P_b centers, are electrically active defects with an energy distribution throughout the Si band gap. They act as generation/recombination centers and contribute to leakage current, low-frequency noise, and reduced mobility, drain current, and transconductance. Since electrons or holes occupy interface traps, they become charged and contribute to threshold voltage shifts. The surface potential dependence of the occupancy of interface traps is illustrated in Fig. 1. Interface traps at the SiO_2/Si interface are acceptor-like in the upper half and donor-like in the lower half of the band gap.[1, 2] As shown in Fig. 1(a), at flatband, with electrons occupying states below the Fermi energy, the states in the lower half of the band gap are neutral (occupied donors designated by "0"). Those between midgap and the Fermi energy E_F are negatively charged (occupied acceptors designated by "-"), and those above E_F are neutral (unoccupied cceptors). For an inverted p-MOSFET, shown in Fig. 1(b), the fraction of interface traps between mid gap and the Fermi level is now unoccupied donors, leading to positively charged interface traps (designated by "+"). Hence interface traps in p-channel devices in inversion are positively charged, leading to negative threshold voltage shifts. Interface trap have differences capture cross section, for this we can say the donor like and acceptor like are not independent [1, 2].

Given the importance of model simulation and the study of the reliability of components in this work, we have simulated the degradation phenomena by the development and implementation of a model using MATLAB on a personal computer. This model takes into account all the geometrical and electrical parameters also P_b centers of the studied transistor. It also gives the different curves of static characteristics, which can be obtained experimentally for different parameters [3]. To locate our results, we have taken as reference the Level 3 of SMARTSPICE model [4]. Energy distribution of donor and acceptor centers in the semiconductor band and their capture cross section were analyzed using simulator technologic Silvaco [5] (not shown in this abstract).

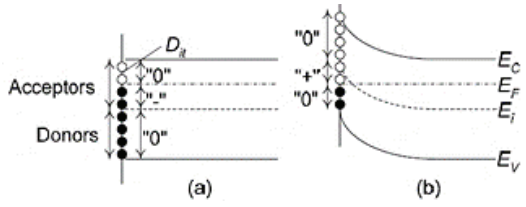


Fig. 1. Band diagrams of the Si substrate a P-channel MOS device showing the occupancy of interface traps p-substrate with (a) negative in interface traps charge at flatband and (b) positive interface trap at inversion. It is either occupied by an electron (solid circle) or occupied by a hole [1].

2. Influence of Density Trap Nss on the Static Characteristics

The model developed in our study is for a P-type substrate, MOS transistors with channel length less than 2 µm taking into account the P_b centers in each region of operation of the transistor. The basic equations of the model were proposed by Dang [4]. In

order to follow the degradation study we have acted on the two voltages that demarcate the three regimes, flatband voltage VFB which separates the accumulation regime from the depletion regimes and the threshold voltage VT which demarcates the depletion regime from the inversion regime, the channel length of the transistor studied is equal to 1 µm, with an oxide thickness equal to 230 Å, flatband voltage is VFB = -0.8 V, the threshold voltage is VTH = 0.8 V. The others parameters used in all simulation are shown in reference [4].

We have seen that the degradation of the transistor is reflected by creating P_b centers. This change leads to a modification of the surface potential ψ_s, This parameter, plays a very important role in the degradation phenomena of TMOS. Through simulated curves, the P_b centers have a detrimental effect on the static characteristics of the components, which facilitates experimentally its identification. Once identified, its elimination becomes easy. This makes it possible to obtain more and more reliable components. Therefore, this simulation gives us the opportunity to improve the performance of the electronic component.

The simulated curves in Fig. 2(a, b) show the influence of the interface states on output or drain characteristics (a) and transfer characteristics (b). We observe:

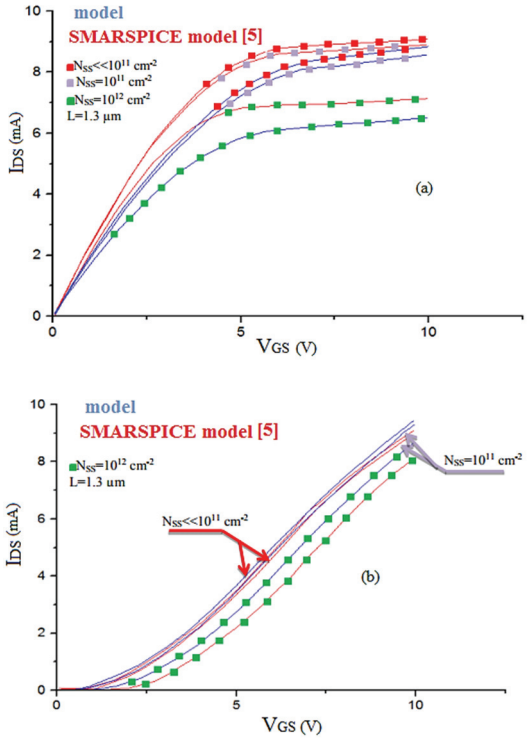


Fig. 2. Influence of P_b center trap in static characteristics (a) output characteristics, (b) transfer characteristics (MATLAB).

– The effect of the P_b centers is negligible for density Nss << 10^{11} atoms/cm^2.
– The increase of density Nss causes an increase in the drain current I_{DS}, this increase affects reliability and component life.
– An inclination of the linear part towards the highest tensions (lower slope), (i.e. the flanks of the curves are modified.

3. Influence of Acceptor Level Density on Component Performance

As we pointed out in the introductory part, electrically active defects are often responsible for degradation of a device, they introduce donor levels and acceptor levels in the band gap of the substrate. In this work we have studied the influence of the density of the acceptor levels in the band gap of the semiconductor. Fig. 3a and b show the drain current versus gate voltage with drain voltage V_{DS} = 0.5 V and V_{GS} = 0 to 3 V. and drain current versus drain voltage MOS transistors V_{GS} = 1.1, 1.2, 1.3 V and we have taken V_{DS} as parameter V_{DS} = 0 to 3 V. Channel length of transistor equal to 0.48 µm and gate oxide thickness equal to 100.163 Angstroms.

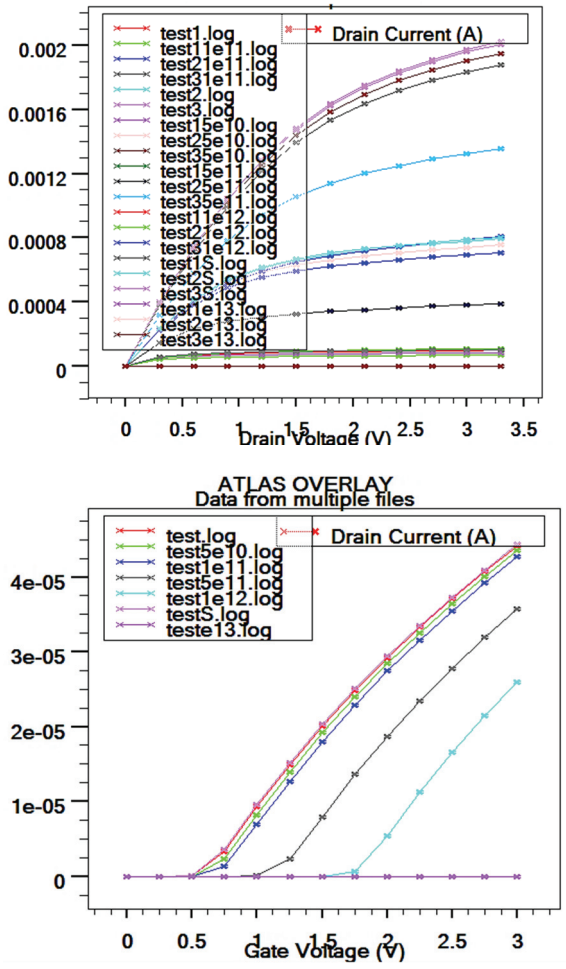


Fig. 3. Influence of P_b center trap in static characteristics (a) output characteristics, (b) transfer characteristics (Silvaco).

We have taken the density of the acceptor levels in the band gap of the semiconductor as: 0.5.10^{10},

$0.5.10^{11}$, $0.5.10^{12}$ and $0.5.10^{13}$ / cm^2, the energy level position is 0.23 eV, the cross sections for the electrons and holes are 1.510^{-15} / cm^2 and $5.5\ 10^{-14}$ / cm^2 respectively, the crystallographic orientation of the substrate is <100>.

As shown in Fig. 3, the increase of the defects density of the acceptor levels causes a shift to the right of the threshold voltage of the TMOS. This shift increases with increasing defect density.

Also the drain current increases with increasing the defects density. The simulation results of the variation of the density of the acceptor levels were noted that for the high densities, only noise is measured. In our case for Dit equal to $10^{13}/cm^2$ was unable to extract the threshold voltage.

The simulated threshold voltage values are shown in Table 1. For values of the density of the acceptor levels lower than 10^{11} atoms/cm^2, the threshold voltage of the transistor remains constant and the effect of defects is negligible on the degradation of electronic components.

Table 1.

Acceptor Density/cm²	0	10^{10}	5.10^{10}	10^{11}	5.10^{11}	10^{12}
Threshold Voltage (V)	.5	.5	.5	.5	1	1.750

– The increase of acceptor level density causes an increase in the drain current I_{DS}, this increase affects reliability and component life drain current characteristics or a small net increase of the current, depending on whether the density of the defect.
– An inclination of the linear part towards the highest tensions (lower slope), (i.e. the flanks of the curves are modified.

4. Conclusion

In this work, we have simulated the degradation phenomena by the development and implementation of a model using MATLAB on a personal computer. This model takes into account all of the geometrical and electrical parameters of the transistor and gives their mathematical expressions. It also gives the can be obtained experimentally for different different curves of the drain characteristics, which parameters. The model is validated with others simulation results obtained from SMARTSPICE. The results obtained in both simulators are similar. Also, we obtained using Simulator Silvaco, the distribution energy in semiconductor band of donor and acceptor traps.

References

[1]. D K. Schroder, J A. Babcock, Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing, *Applied Physics Review*, Vol. 94, 2003, pp. 1-18.

[2]. P. M. Lenahan, Book chapter on P_b and E prime Centers, in a CRC handbook, Taylor Francis publishers on defects in semiconductor devices, 2008.

[3]. N. Guenifi, O. Ghobar, D. Bauza, Further evidences that P_{B0} centers dominate Si/SiO_2 interface traps fully processed MOSFET's, in *Proceedings of the 15th Workshop on Dielectrics in Microelectronics (WODIM'08)*, Berlin, Germany, 23-25 June 2008, pp. 1-2.

[4]. T. Quales, et al., SPICE Version F2 User's Manual, Department of Computer Sciences, *University of California*, Berkley, Oct. 1992.

[5]. Manuel D'utilisation de Silvaco, VWF Interactive Tools, Vol. 2, *Silvaco International*, 1998.

(012)

Investigation of Post-Implantation Annealing for Phosphorus-Implanted 4H-Silicon Carbide

V. Šimonka [1], A. Hössinger [2], S. Selberherr [3] and J. Weinbub [1]
[1] Christian Doppler Laboratory for High Performance TCAD, Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Wien, Austria
[2] Silvaco Europe Ltd., Compass Point, St Ives, Cambridge, PE27 5JL, United Kingdom
[3] Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Wien, Austria
Tel.: +43 1 58801 36031
E-mail: simonka@iue.tuwien.ac.at

Summary: A time-dependent modeling approach for electrical activation of implanted dopant species in semiconductors is currently missing, which limits the predictability of process simulations in technology computer-aided design. In this study we investigate the time-dependent electrical activation of phosphorus-implanted silicon carbide and propose a transient model to characterize the donor concentration as a function of the annealing time, temperature, and total implanted concentration.

Keywords: Silicon carbide, Annealing, Phosphorus, Implantation, Modeling, Transient.

1. Introduction

Silicon carbide (SiC) is an attractive candidate to replace traditional silicon (Si), particularly in power electronics, in order to improve device properties and reduce internal device losses. The advantageous properties of SiC are higher thermal conductivity, higher breakdown field, and higher carrier saturation velocity. However, some fabrication steps of novel SiC devices are not yet fully optimized [1]. In particular, post-implantation steps are currently not well understood and, moreover, a time-dependent, i.e., transient, modeling approach is still completely missing.

In this study we investigate the time-dependent electrical activation of phosphorus (P)-implanted SiC and propose a transient model to characterize the donor concentration (N_D) for arbitrary annealing time (t_A), temperature (T_A), and total concentration (C_{tot}). We then perform a detailed parameter analysis and various process simulations to corroborate our approach.

2. Method

We have collected numerous experimental data in order to identify major dependencies on electrical activation of P-implanted SiC. Free carrier concentrations have been fitted with the charge neutrality equation [2], shown in Fig. 1, to obtain N_D, which have been plotted as a function of t_A for various T_A and C_{tot}, shown in Fig. 2. Based on these results, we have fitted the pre-processed data with the transient activation model, which has been inherited from the model for annealing Si-based device structures [3]:

$$\frac{dN_D}{dt} = -\frac{1}{\tau}\left(N_D - \frac{C_{tot}}{1 + C_{tot}/C_{ss}} \right), \qquad (1)$$

where C_{ss} and τ are the solid solubility and the characteristic time, respectively. In order to confirm the model predictions, we have performed simulations of ion implantation followed by the various post-implantation annealing steps, considering t_A, T_A, and C_{tot}, in order to mimic experimental setups [4].

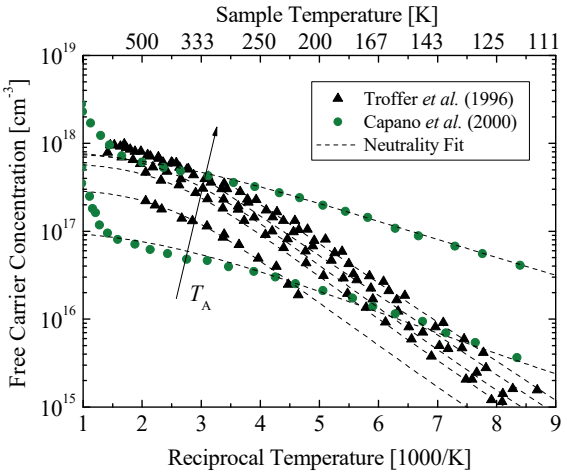


Fig. 1. Charge neutrality fits of free carrier concentrations as a function of temperature.

3. Results and Discussion

The obtained model parameters C_{ss} and τ are plotted as a function of T_A, shown in Fig. 3, and fitted with the Arrhenius equation in order to incorporate the continuous temperature dependence and to enable parameter extrapolations. The Arrhenius parameters for C_{ss} are: pre-exponential factor $Z = 7.17\times10^{23}$ cm^{-3} and activation energy $E = 2.09$ eV and for τ: $Z = 1.23\times10^{-4}$ min and $E = 1.38$ eV.

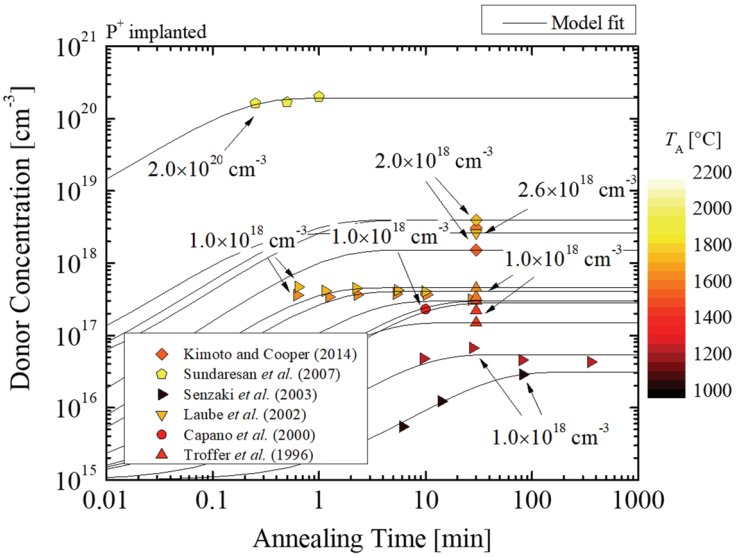


Fig. 2. Experimental data of time-dependent donor concentrations (symbols) and fits using the transient activation model (solid lines).

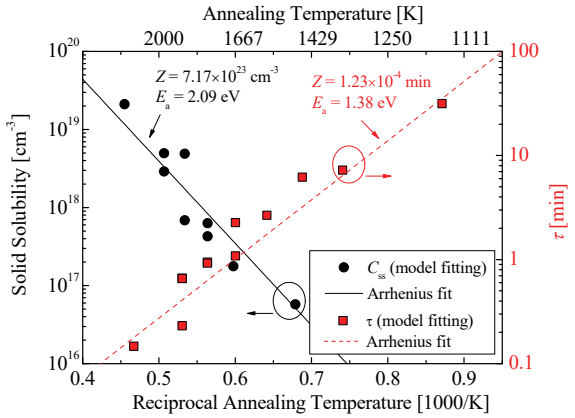


Fig. 3. Arrhenius plots of model parameter C_{ss} (left axis) and τ (right axis) obtained from the model fitting (cf. Fig. 2).

The two temperature-dependent parameters enable the characterization of N_D for P-implanted 4H-SiC over a wide range of processing variables, i.e., T_A and C_{tot}. The parameter analysis is shown in Fig. 4. Below 900 °C the activation of P is very low (i.e., < 10 %) and above 1000 °C the activation of SiC implants depends highly on C_{tot}. Furthermore, the activation process saturates for a particular T_A and C_{tot}, shown with the red shape in Fig. 4.

Finally, we have performed simulations, shown in Fig. 5, in order to validate the model. P-implantations have been conducted with the Monte Carlo ion implantation method from Silvaco's Victory Process simulator (blue solid line), which reproduce experimental doping profiles (blue symbols). The green lines indicate simulation results of the active P concentration after 30 min annealing at 1550 °C and 1700 °C. The green squares indicate the measured mean active concentration from [4]. The model confirms low activation of P-implanted SiC ($N_D < C_{tot}$), which is a consequence of the saturation effect at high doping concentrations ($C_{tot} \approx 1\times10^{20}$ cm^{-3}) for a particular T_A. Fig. 5 proves that the predicted depth profiles are in excellent agreement with the experimental data, i.e., the estimated average error is < 3 %.

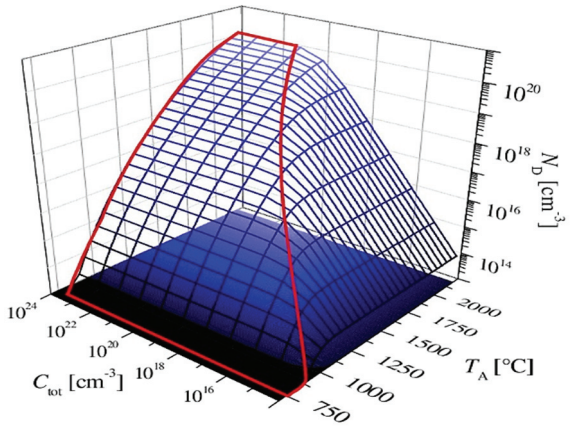


Fig. 4. Parameter analysis, i.e., model predictions of donor concentrations as a function of C_{tot} and T_A.

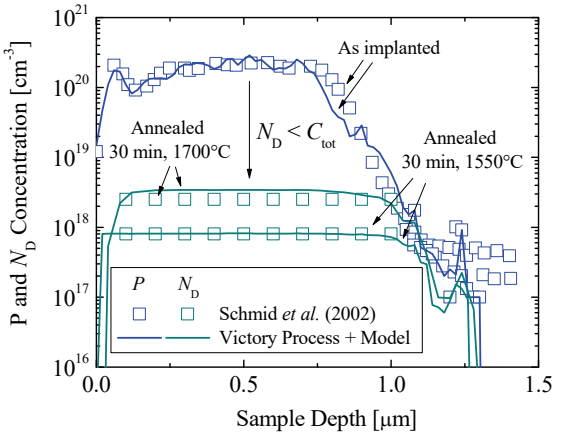


Fig. 5. Depth profiles of P and N_D from experiments (symbols) and simulations (lines).

4. Conclusions

We have proposed a transient activation model for P-implanted 4H-SiC, which has been calibrated according to experimental data from the literature. Our findings underline the importance of the proposed activation model, as 100 % activation cannot be assumed. The actual activation ratio must be accurately predicted – which is now possible – as this critically affects consecutive device performance characteristics.

Acknowledgements

The financial support by the Austrian Federal Ministry of Science, Research and Economy and the National Foundation for Research, Technology and Development is gratefully acknowledged.

References

[1]. V. Šimonka, *et al.*, Empirical model for electrical activation of aluminium- and boron-implanted silicon carbide, *IEEE Transactions on Electron Devices*, Vol. 65, Issue 2, pp. 674-679.
[2]. T. Kimoto, J. A. Cooper, Fundamentals of Silicon Carbide Technology, *John Wiley & Sons*, 2014.
[3]. SILVACO'S Victory Process Simulator, https://www.silvaco.com/products/tcad/
[4]. F. Schmid, *et al.*, Electrical activation of implanted phosphorus ions in [0001]- and [11-20]-oriented 4H-SiC, *Journal of Applied Physics*, Vol. 91, Issue 11, 2002, pp. 9182-9186.

(013)

TCAD Based Investigation of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) Transistor

Vandana Kumari [1], Manoj Saxena [2] and Mridula Gupta [3]
[1] Department of Electronics, Maharaja Agrasen College, University of Delhi, India
[2] Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, India
[3] Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus, New Delhi, India
E-mail: mridula@south.du.ac.in

Summary: In this work, TCAD based investigation of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) Transistor has been presented for reliability assessment and high frequency application. Leakage current has been examined for the assessment of device reliability for different parametric variations. The position of the peak doping concentration along the channel, work-function of source/drain metallic contacts and straggle value of Gaussian profile has been changed to optimize the performance of the device for HF applications. Higher straggle value of Gaussian doping results in superior cut-off frequency. The performance of the Gaussian doped DG-JL transistor has also been compared with the equivalent uniform doped DG-JL transistor. Compared to uniformly doped transistor, Gaussian doped DG-JL transistor provides superior cut-off frequency, better reliability in terms of lower electron temperature inside the device and lesser deterioration with the change in S/D work-function.

Keywords: JunctionLess, Gaussian, Cut-off frequency, leakage current, Schottky contacts.

1. Introduction

From past few years, JunctionLess Transistor (JLT) has emerged as a viable alternative for low voltage circuit applications [1]. For JLT, suitable gate work-function, high channel doping along with thinner channel region is required to change the transistor form fully depletion state to off state at zero gate voltage. Thus, Double Gate and Fin-shaped JLTs are more promising architectures instead of single gate architecture [2-4]. Various interesting features associated with the multigate JunctionLess transistor are: better sub-threshold slope, lower leakage current, high I_{on}/I_{off} ratio and lower threshold voltage roll-off [5-6]. Schottky barrier DG-JL transistor also provides benefits in terms of lower source drain series resistance leading to better on-state current of the device [7-9]. But the advantage comes at the cost of higher leakage current through the device in the off state. To circumvent this effect, non-uniformly doped channel can be used in spite of using uniform doping throughout the channel. It has also been reported previously [9-12] that non-uniformly doped JunctionLess transistor provides higher I_{on}/I_{off} ratio [9-12] by improving the leakage current of the device. In 2018, empirical model for non-uniformly doped Double Gate junctionLess Transistor has been reported by Kumari *et. al* [13] wherein, the superiority of the device has been reported and DC electrical parameters are compared with uniformly doped JLT (having equivalent total doping concentration inside the channel region).

In this work, performance of the Gaussian doped Double Gate junctionLess (GD-DG-JL) Transistor has been investigated for high frequency applications by extracting the cut-off frequency of the device using extensive TCAD simulation [14]. Different device specifications like oxide permittivity, straggle value of Gaussian doping and position of the peak of Gaussian doping has also been varied for optimizing the device performance for high frequency applications. The reliability issues of the GD-DG-JL transistor has also been analyzed by investigating gate leakage current and electron temperature of the device. Compared to uniform doped (having equivalent doping same as Gaussian) DG-JL transistor, GD-DG-JL transistor provides higher cut-off frequency and slightly lower electron temperature near the drain side.

2. TCAD Model Parameters

The cross-sectional view of GD-DG-JL transistor has been shown in Fig. 1. Models used for TCAD based investigation are comprises of Field dependent mobility model (FLDMOB), Fermi Dirac statistics (Fermi), hydrodynamic model and band gap narrowing (bgn) model (generally used for accounting the quantum effect arise due to high doping). For the evaluation of leakage current model, hot electron injection model (i.e. hei) has been taken into consideration [14], however, for electron temperature calculation, hydrodynamic model has been used.

3. Assessment of Gaussian Profile

In this section, TCAD based assessment of non-uniformly doped DG-JL transistor has been presented for high frequency applications. Comparison has also been assessed with equivalent doped conventional DG-JL transistor.

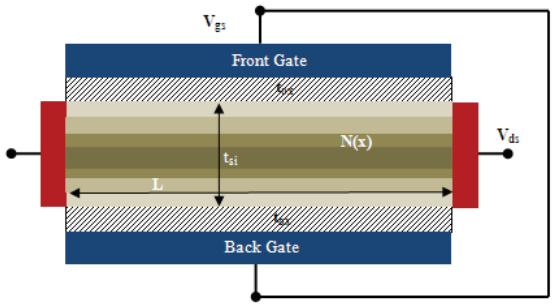


Fig. 1. Schematic view of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) Transistor where, t_{ox} is the oxide thickness, L is the channel length, N(x) represents the Gaussian doping profile and t_{si} is the channel thickness.

Fig. 2, and 3(a) compares, cutoff frequency behaviour with the position of peak doping concentration at different straggle value of the Gaussian doping profile and source/drain workfunction respectively. As depicted from from Fig. 2, higher straggle value results in high cutoff frequency due to higher transconductance of the device. As seen from the results, the behaviour of cut-off is symetrical across the centre of the channel. Also the shift in the peak towards the surface from the centre deteriorates the performance by reducing trans-conductance and hence cut-off frequency of the device.

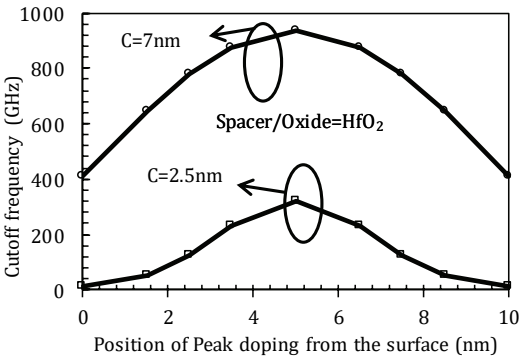


Fig. 2. Cutoff frequency variation with the position of peak doping concentration in Gaussian doped DG-JL-transistor at different straggle value: V_{ds} = 0.5 V, V_{gs} = 0.6 V, S/D workfunction = 4.1 eV, t_{ox} = 1.5 nm, L = 32 nm, t_{si} = 10 nm, $N_p = 1\times10^{19}$ cm^{-3}.

However compare to device havice higher oxide permittivity (as shown in Fig. 2), higher cutoff frequency is resulted from the device having lower oxide permittivity as shown in Fig. 3(a). This reverse behaviour in Fig. 3(a) is due to the higher gate capacitance of the device irrespective of higher trans-conductance in case of high oxide permittivity. With the enhancement in source/drain workfunction from 4.1 eV to 4.3 eV, reduction in cutoff frequency is observed from Fig. 3(a). This reduction is due to the lower current carrying capability of the device because of lower electron concentration (as shown in Fig. 3(b)) at higher drain workfunction. Compared to uniform doped DG-JL transistor (having equivalent total doping inside the channel), GD-DG-JL transistor provides higher cut-off frequency.

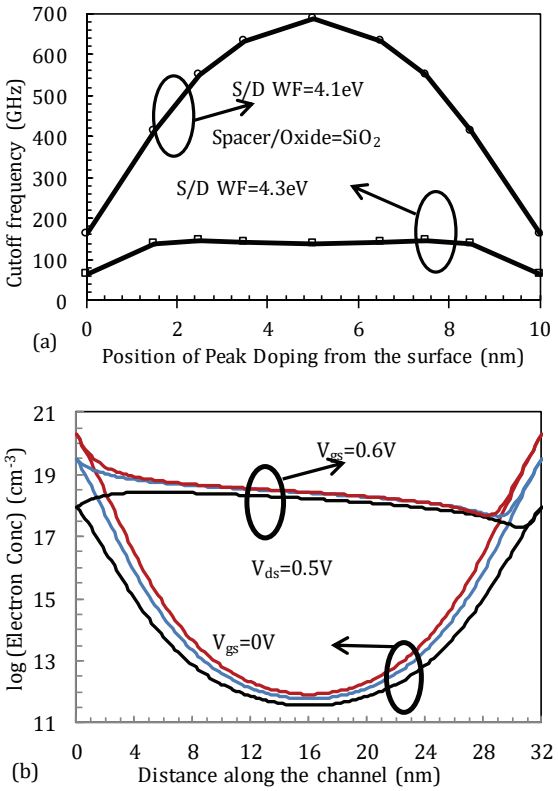


Fig. 3. (a) Cutoff frequency variation with the position of peak doping concentration in Gaussian doped DG-JL-transistor at different source/drain work-function: V_{ds} = 0.5 V, V_{gs} = 0.6 V, c = 2.5 nm, (b) Variation in electron concentration with channel length at different gate voltage; t_{ox} = 1.5 nm, L = 32 nm, c = 2.5 nm, t_{si} = 10 nm, $N_p = 1\times10^{19}$ cm^{-3}, black -4.3 eV, blue -4.2 eV and red -4.1 eV.

In Fig. 4, gate leakage current has been plotted against the peak doping concentration for different oxide permittivity. With the reduction in peak doping concentration, gate leakage current of the device increases, and the change is more significant at higher oxide permittivity. Also, the gate leakage current is significantly high at higher oxide permittivity. Thus, with the amalgamation of higher permittivity oxide material device reliability deteriorates.

Cutoff frequency variation of Gaussian doped DG-JL transistor with peak doping concentration at different straggle value has been plotted in Fig. 5. With the reduction in peak doping concentration of gaussian doping, cutt-off frequency deteriorates tremendously due to the reduction in overall doping inside the channel. Since for junctionless transistor, doping of the channel should be high to fully deplete the channel at

zero bias condition. This reduction in cuttoff frequency is higher at higher straggle value.

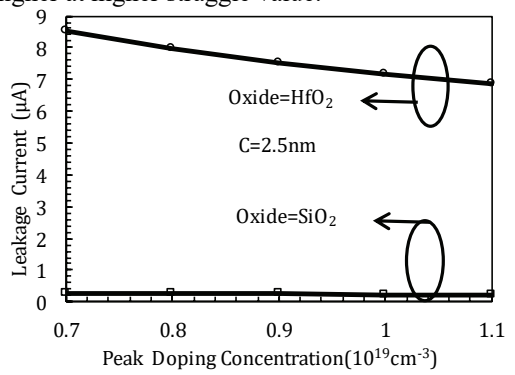


Fig. 4. Gate leakage current variation with peak doping concentration in Gaussian doped DG-JL-transistor at different oxide permittivity: V_{ds} = 0.5 V, V_{gs} = 2 V, c = 2.5 nm, S/D workfunction = 4.1 eV, t_{ox} = 1.5 nm, L = 32 nm, t_{si} = 10 nm.

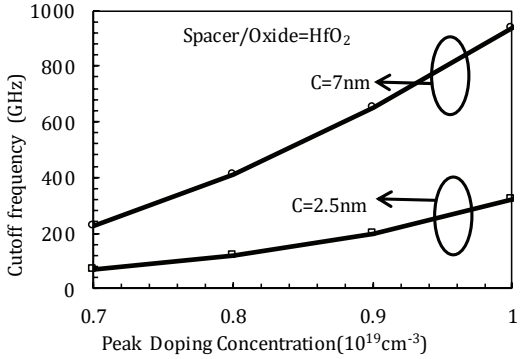


Fig. 5. Cutoff frequency variation with peak doping concentration in Gaussian doped DG-JL-transistor at different straggle value: V_{ds} = 0.5 V, V_{gs} = 0.6 V, S/D work-function = 4.1 eV, t_{ox} = 1.5 nm, L = 32 nm, t_{si} = 10 nm, position of the peak is at center of the channel.

In Fig. 6, variation of gate capacitance with frequency has been investigated with different straggle, peak doping concentration and position of peak doping concentration. The variation in the position of peak doping concentration from center to surface leads to reduction in gate capacitance. However, trans-conductance of the device also deteriorates [13] leading to reduction in cut-off frequency as observed from Fig. 2 and 3(a). The enhancement of Gaussian straggle further increases the gate capacitance, however this enhancement is lower than the enhancement in trans-conductance leading to improvement in cut-off frequency of the device as discussed in Fig. 2. Higher peak doping concentration also deteriorates the gate capacitance of the device but the enhancement in trans-conductance is superior than this deterioration and thereby improving the overall cut-off frequency of the device as seen from Fig. 5.

The influence of S/D workfunction on the leakage current of Gaussian doped DG-JL transistor has been explored in Fig. 7. As seen from the figure, leakage current is higher for high-k gate dielectric compared to SiO_2. With the enhancement in S/D work-function, leakage current increases first up to nearly 4.1 eV and after that it decreases. Similar trend can also be observed with SiO_2 gate dielectric. However, the peak in that case observed at higher work-function i.e. at 4.2 eV. However, compared to Gaussian doped DG-JL transistor, equivalent uniform doped DG-JL transistor shows lower leakage current.

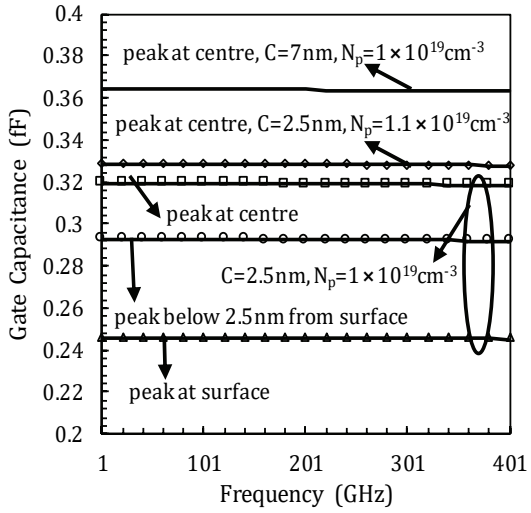


Fig. 6. Gate capacitance comparison of Gaussian doped DG-JL transistor for different straggle, peak doping conc and position of peak doping with frequency: V_{ds} = 0.5 V, V_{gs} = 0.6 V, t_{ox} = 1.5 nm, L = 32 nm, t_{si} = 10 nm.

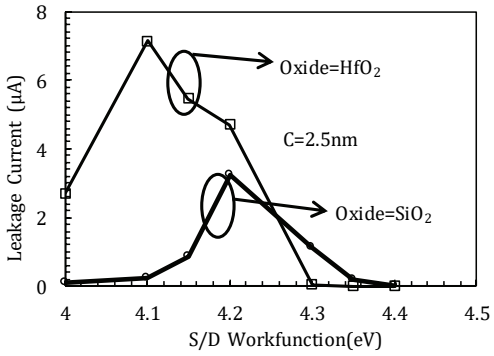


Fig. 7. Gate leakage current variation with S/D work-function for SiO_2 and HfO_2 gate dielectric in Gaussian doped DG-JL-transistor at different oxide permittivity: V_{ds} = 0.5 V, V_{gs} = 2 V, c = 2.5 nm, t_{ox} = 1.5 nm, L = 32 nm, $|t_{si}$ = 10 nm.

4. Comparison of Uniform & Gaussian Profile

In Fig. 8, comparison of uniform and Gaussian doped DG-JL transistor has been plotted for different S/D work-function. Compared to uniformly doped DG-JL transistor Gaussian doped (having equivalent doping same as uniform device) device provides higher cut-off frequency. Enhancement in S/D workfunction leads to reduction in cut-off frequency for both Gaussian as well as uniformly doped DG-JL transistor. However, the change is significantly higher in Gaussian doped DG-JL transistor. Thus, the

influence of S/D workfunction is tremendously higher in Gaussian doped DG-JL transistor.

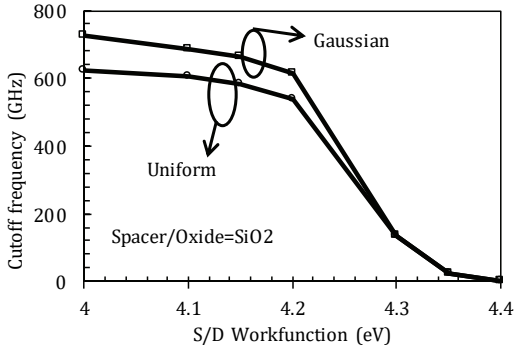


Fig. 8. Cutoff frequency variation with S/D workfunction for uniform and Gaussian doped DG-JL transistor: V_{ds} = 0.5 V, V_{gs} = 0.6 V, t_{ox} = 1.5 nm, L =32 nm, t_{si} =10 nm, position of the peak is at center of the channel. For uniformly doped DG-JL transistor, equivalent doping has been used.

Fig. 9 shows the comparison of electron tempearture of gaussian and uniformly doped DG-JL transistor. As depicted, electron temperature for gaussian and uniformly doped DG-JL tranistor is nearly same (slightly higher in uniformly doped DG-JL transistor). With the enhancement in the straggle value of doping, electron temperature inside the device deteriorates, resulting in poorer SCEs as reported in preveoulsly reported work in terms of higher DIBL. As a result of higher S/D workfunction electron temperature inside the device increases in both uniformly and gaussian doped devices leading to deterioration in device performance as depicted from Fig. 7 in terms of lower cut-off frequency due to lower trans-conductance and drain current of the device. However, the enhancement in electron temperature with S/D workfunction is higher in gaussian doped DG-JL transistor.

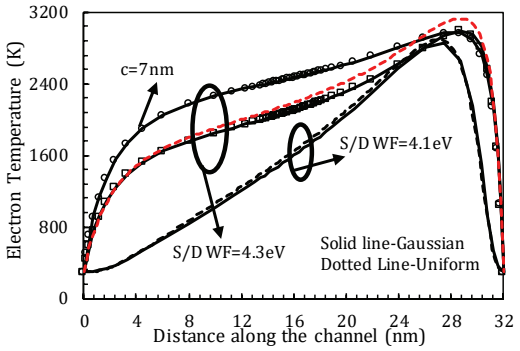


Fig. 9. Electron temperature comparison of Gaussian and uniformly doped DG-JL transistor for different straggle value: V_{ds} = 1 V, V_{gs} = 1 V, t_{ox} = 1.5 nm, L = 32 nm, t_{si} = 10 nm.

Fig. 10(a) and (b) shows the variation of drain current and trans-conductance respectively of uniformly and gaussian doped DG-JL transistor at different source/drain work-function. Uniform doped DG-JL transistor (having equivalent doping same as gaussian doped device) delivers lower on-state current compared to gaussian doped DG-JL transistor. Inspite of having higher drain current, I_{on}/I_{off} ratio of Gaussian doped DG-JL transistor deteriorates compared to uniformly doped DG-JL transistor (due to lower leakage current). However, by optimizing the profile of gaussian doping (equivalent doping remains same as uniform), higher I_{on}/I_{off} can be achieved (discussed in detail in [13]). As a result of higher drain current in gaussian doped DG-JL transistor, higher trans-conductance is seen from from Fig. 10(b) compared to uniformly doped channel. With the enhancement in S/D workfunction, reduction in on-state current and hence trans-conductance is observed from Fig. 10(a) and **(b)** respectively. As a result, I_{on}/I_{off} ratio of the devices also deteriorates.

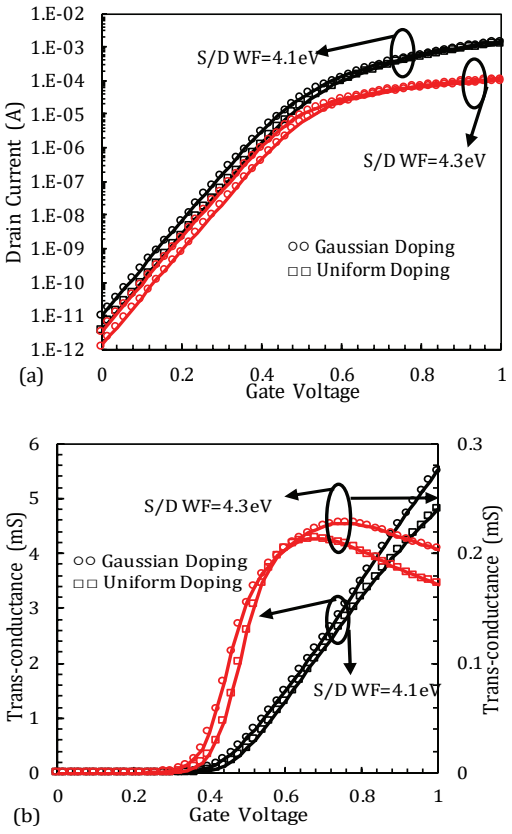


Fig. 10. Variation of (a) drain current and (b) trans-conductance with gate voltage at different S/D workfunction for uniformly and Gaussian doped DG-JL transistor for different straggle value: V_{ds} = 0.5 V, t_{ox} = 1.5 nm, L = 32 nm, t_{si} = 10 nm.

As seen from Fig. 11, gate capacitance remains constant with the variation in frequency. By changing the doping profile from Gaussian to uniform (having equivalent doping same as Gaussian), gate capacitance remains almost constant (marginally lower in Gaussian doped DG-JL transistor). However, the enhancement in S/D drain workfunction leads to reduction in gate capacitance and the change is higher in Gaussian doped DG-JL transistor as clearly observed from the Fig. 11. Also, at higher S/D work-function, gate

capacitance is inferior in case of Gaussian doped device. In spite of having this lower gate capacitance, cut-off frequency of the device deteriorates with higher S/D
work-function as seen in Fig. 3(a) and 8. This reduction is due to the reduction is trans-conductance of the device as seen in Fig. 10(b).

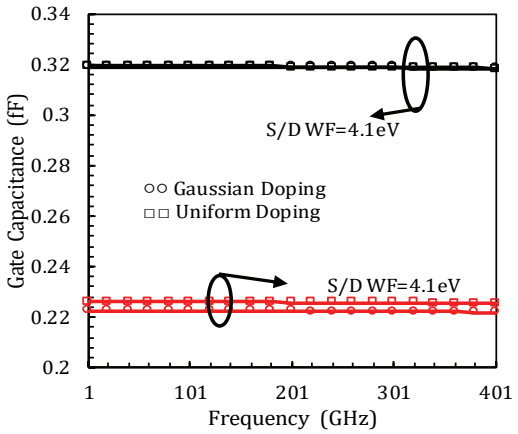


Fig. 11. Variation of gate capacitance with frequency at different S/D workfunction for uniformly and Gaussian doped DG-JL transistor for different straggle value: V_{ds} = 0.5 V, V_{gs} = 0.6 V, t_{ox} = 1.5 nm, L = 32 nm, t_{si} = 10 nm.

5. Conclusions

TCAD based investigation of GD-DG-JL transistor has been reported in this work. Cut-off frequency at different device parameters such as: peak doping concentration, straggle value, gate oxide permittivity, position of peak doping concentration and S/D work-function has been investigating. Results presented in the work shows that the Gaussian doped DG-JL transistor exhibits higher cut-off frequency compared to uniformly doped DG-JL transistor having same total doping concentration. Device reliability in terms of gate leakage current and electron temperature has also examined in this work. Gate capacitance and electron temperature of uniformly and Gaussian doped DG-JL transistor is nearly same (slightly better in Gaussian doped device), but the deterioration with the change in S/D workfunction is higher in uniform doped DG-JL transistor.

References

[1]. S.-J. Choi, D.-I. Moon, S. Kim, J.-H. Ahn, J.-S. Lee, J.-Y. Kim, Y.-K. Choi, Nonvolatile memory by all-around-gate junctionless transistor composed of silicon nanowire on bulk substrate, *IEEE Electron Device Lett*., Vol. 32, Issue 5, May 2011, pp. 602–604.

[2]. C.-W. Lee, A. A fzalian, N. D. Akhavan, R. Yan, I. Ferain, J.-P. Colinge, Junctionless multigate field-effect transistor, *Appl. Phys. Lett*., Vol. 94, Issue 5, 2009, 053511.

[3]. J.-P. Colinge, Jean-Pierre; C-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, R. Murphy, Nanowire transistors without junctions, *Nature Nanotechnology*, Vol. 5, February 2010, pp. 225-229.

[4]. T. K. Chiang, A quasi-two-dimensional threshold voltage model for short-channel junctionless double-gate MOSFETs, *IEEE Trans. on Electron Devices*, Vol. 59, Issue 9, September 2012, pp. 2284-2289.

[5]. J. P. Colinge, Junctionless nanowire transistor (JNT): Properties and design guidelines, *Solid-State Electron*., Vols. 65-66, 2011, pp. 33-37.

[6]. P. Mondal, B. Ghosh, P. Bal, M. W. Akram, A. Salimath, Effects of non-uniform doping on junctionless transistor, *Appl. Phys. A*, Vol. 119, Issue 1, Apr. 2015, pp. 127-132.

[7]. T. K. Chiang, A quasi-two-dimensional threshold voltage model for short-channel junctionless double-gate MOSFETs, *IEEE Trans. on Electron Devices*, Vol. 59, Issue 9,September 2012, pp. 2284-2289.

[8]. T.-K. Chiang, A new quasi-2-D threshold voltage model for short-channel junctionless cylindrical surrounding gate (JLCSG) MOSFETs, *IEEE Trans. on Electron Devices*, Vol. 59, Issue 11, November 2012, pp. 3127-3129.

[9]. H. Ferhati, F. Douak, F. Djeffal, Role of non-uniform channel doping in improving the nanoscale JL DG MOSFET reliability against the self heating effect, *Superlattices and Microstructures*, Vol. 109, September 2017, pp. 869-879.

[10]. P. Bal, B. Ghosh, P. Monda, M. W. A. Akram, A laterally graded junctionless transistor, *Journal of Semiconductor*, Vol. 35, Issue 3, 2014, pp. 034001-034004.

[11]. B. Singh, D. Gola, K. Singh, E. Goel, S. Kumar, S. Jit, Analytical modeling of channel potential and threshold voltage of double-gate junctionless FETs with a vertical Gaussian-like doping profile, *IEEE Trans. on Electron Devices*, Vol. 63, Issue 6, 2016, pp. 2299-2305.

[12]. P. Mondal, B. Ghosh, P. Bal, Planar junctionless transistor with non-uniform channel doping, *Appl. Phys. Lett*., Vol. 102, Issue 13, 2013, 133505.

[13]. V. Kumari, A. Kumar, M. Saxena, M. Gupta, Empirical model for non-uniformly doped symmetric double gate junctionless (NU-DG-JLT) transistor, *IEEE Trans. on Electron Devices*, Vol. 65, Issue 1, 2018, pp. 314-321.

[14]. ATLAS: 3-D Device Simulator, Version 5.14.0.R, *Silvaco International*, 2010.

(014)

Simplified Design of the Digital Control Logic for SAR ADC

M. Borgarino [1], N. Verrascina [2] and J.-B. Begueret [2]
[1] Eng. Department "Enzo Ferrari", University of Modena and Reggio Emilia, Modena, Italy
[2] University of Bordeaux, IMS Laboratory, Bordeaux, France
Tel.: +39 059 2056168, fax: +39 059 2056129
E-mail: mattia.borgarino@unimore.it

Summary: This paper reports on an original approach to design the digital control logic of a SAR ADC where no sequencers or code registers are used. The proposed digital control logic was applied to an 8-bit SAR ADC designed in a 130 nm CMOS technology. The simulations demonstrate that the proposed digital control logic is correctly working leading to a SAR ADC exhibiting performances well aligned with the literature in terms of dissipated power and sampling rate.

Keywords: SAR ADC, Control logic, CMOS, Shift register, Counter.

1. Introduction

Successive Approximation Register Analog-to-Digital Converter (SAR ADC) typically operates following a binary search algorithm implemented in a Digital Control Logic (DCL), which is usually constituted by sequencers and code registers [1-5]. The present paper reports on a simplified design of a DCL for SAR ADC where sequencers or code registers are not used. The work addresses first the binary algorithm implementation and then the general architecture and schematic of the proposed DCL. As a test, the DCL is applied to control an 8-bit SAR ADC designed in a 130 nm CMOS technology.

2. Binary Algorithm Implementation

The DCL proposed in the present work was designed as a finite state machine, whose state transition diagram describes a binary algorithm. It is here worth noticing that in the literature the logic controlling the SAR ADC is not designed or described by adopting a finite state machine approach. Even in [2], where the authors report a working flow, very close to a state transition diagram to describe their proposed switching method, a finite state machine approach was not used to design the control logic. For sake of clearness, Fig. 1 depicts the state transition diagram for a DCL in the case of a 4-bit resolution ADC. The diagram is distributed on four layers. The first layer is the initial state. In the fourth layer are the final states obtained at the end of the digitization process. The DCL goes through the states on the base of the outcome of the comparator around which the SAR ADC is designed (see Fig. 2). In the present work the state is encoded into six bits. The two right-most bits (in grey) count the layer (e.g. they are "00" for the first layer and "10" for the second layer). The remaining four bits (in black) track the sequence of the comparator outputs. In the initial state, these bits are all set to "1". After each comparison, these bits are right shifted and the left-most one is replaced by the comparator outcome. This kind of state encoding, even if it does not minimize the number of bits, allows for a simplified design of the DCL. The state encoding suggests indeed that next state of the binary algorithm can be generated by using a shift register for the bits in black and a counter for the bits in grey.

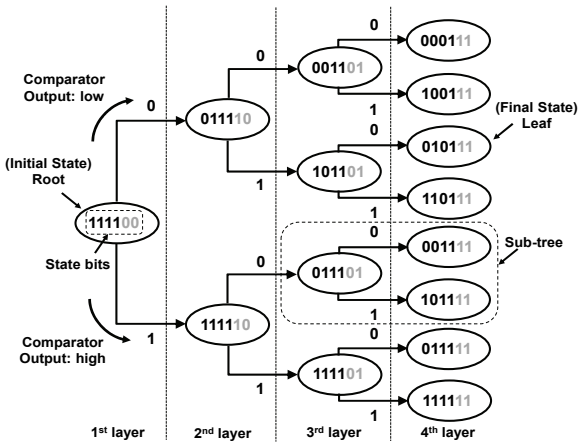


Fig. 1. State transition diagram.

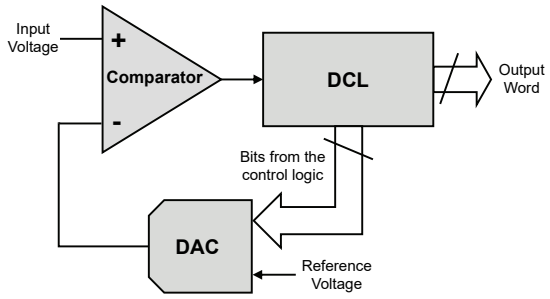


Fig. 2. General building block diagram of a SAR ADC.

3. DCL Architecture and Schematic

Fig. 3 depicts the general architecture of the DCL proposed in the present work. It is constituted by four main building blocks: a shift register, a counter, a logic network, and an output register bar. It is worth here stressing out that no sequencers and code registers are used. The logic network is needful, because the states bit cannot be directly used to control the DAC. The logic network can be therefore designed, in order to implement the desired control strategy for the DAC. The output register bar makes available the output bits when the digitization process is over.

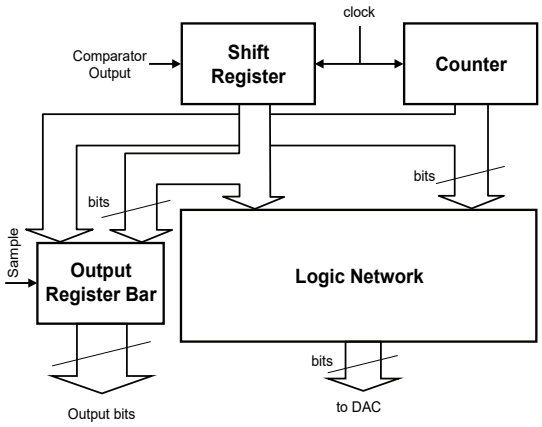


Fig. 3. Building block diagram of the proposed DCL.

The following Fig. 4 shows the schematics of the shift register, the counter and the output register bar of the DCL in the case of an 8-bit resolution SAR ADC, where the states in the transition diagram are encoded with 11 bits (8 black bits and 3 grey bits). Fig. 4 reveals the high simplification in the design of the DCL proposed in the present work: a D-type register is the basic cell for the shift register, the counter, and the output register bar, as well. The CMOS static D-type register was designed with a master-slave architecture.

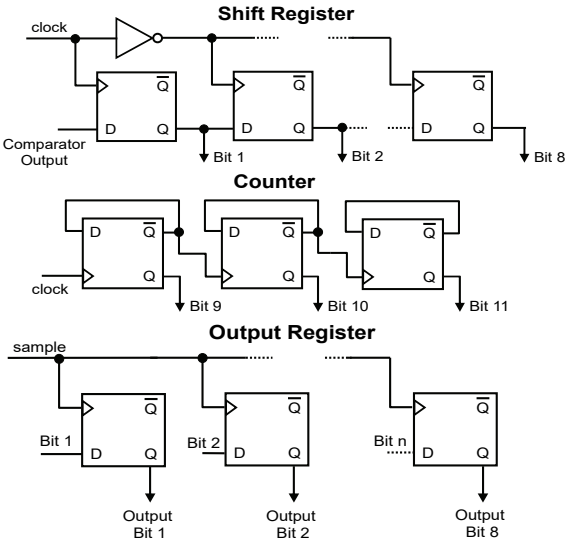


Fig. 4. Schematics of the shift register, the counter and the output register bar.

3. The DAC

The previously described DCL was implemented in a low cost, 130 nm CMOS bulk technology from STMicroelectronics to control an 8-bit SAR ADC, whose architecture is reported in Fig. 5. It is a single-ended SAR ADC, whose core is constituted by a couple of charge shared DACs implemented as multi switched-capacitor circuits as depicted in the following Fig. 6.

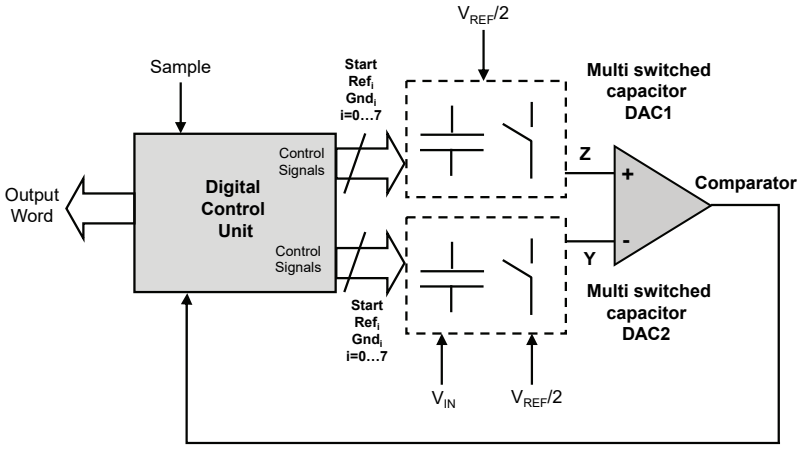


Fig. 5. Architecture of the 8-bit designed SAR ADC.

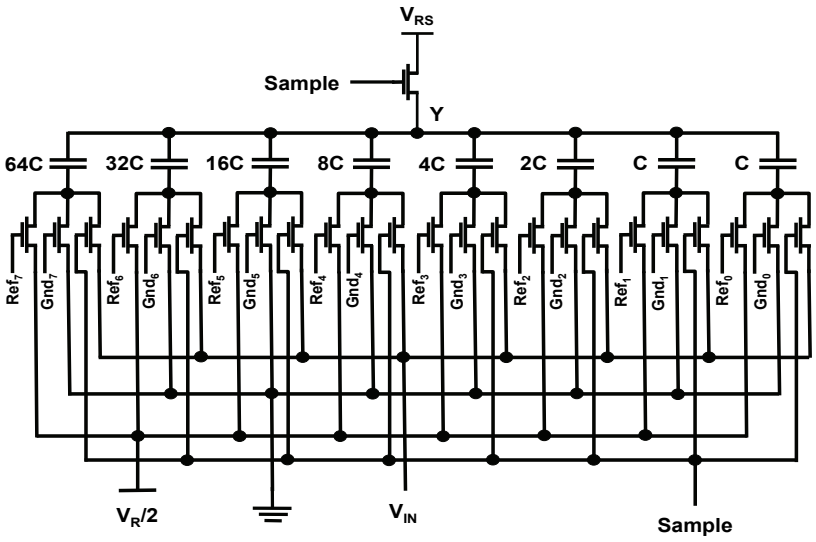


Fig. 6. Schematic of the multi switched-capacitor DAC.

The logic network in Fig. 3 was designed so that the state transition diagram in Fig. 1 matches the switching strategy reported in [2], to minimize the power dissipated by the DAC up to about 88 % with respect to other switching strategies. In this strategy, the DAC1 receives half reference voltage ($V_{REF}/2$) and it is involved in the generation of the MSB only. On the other hand, the DAC2 receives both $V_{REF}/2$ and the sampled analog input voltage (V_{IN}) to be converted and it is involved in the generation of all the remaining bits. DAC1 and DAC2 should be identical, in order to avoid capacitive mismatch at the Y and Z inputs of the comparator.

The comparator in Fig. 2 was designed as a dynamic latch, as depicted in the following Fig. 7. This circuit offers the advantage of a lower dissipated power than an operational amplifier. Since the symmetry is mandatory, a dummy output inverter has been added at the output node not connected to the DCL.

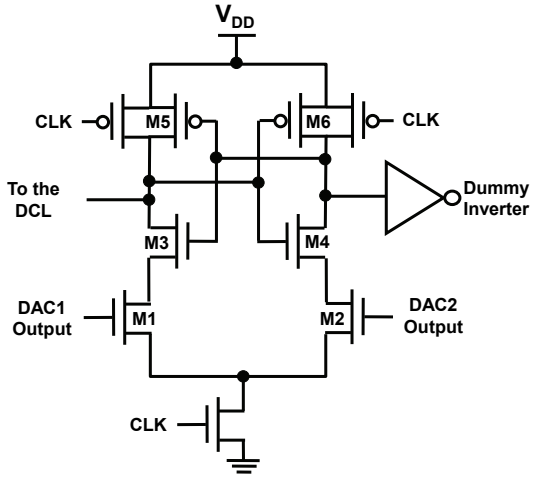


Fig. 7. Schematic of the comparator.

Finally, the logic network in Fig. 3 was synthesized through Karnaugh's maps and designed with static CMOS logic gates biased with a supply voltage of 750 mV.

3. The Test

An 800 mV_{pp}, 70 Hz sinusoidal tone was applied at the input of the resulting SAR ADC (see Fig. 8). Fig. 9 shows the generation of the output bits for several voltages sampled at 1.4 kHz. All the digital output words match the corresponding analog input voltage within the tolerance of $V_{REF}/2^8 = 3.13$ mV, where V_{REF} is the chosen reference voltage of 800 mV. Fig. 9 demonstrates therefore the correct operation of the proposed DCL.

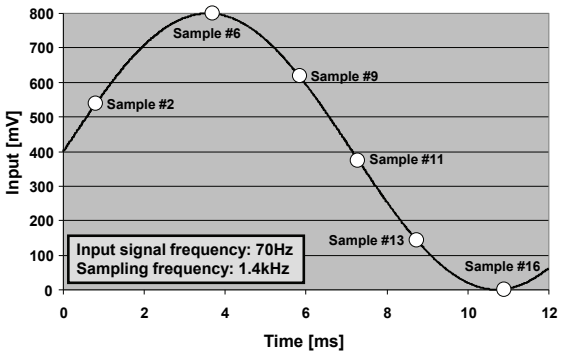


Fig. 8. Input sinusoidal tone with sampled values.

The whole SAR ADC dissipated around 70 nW for a sampling rate of 1 kS/s. Fig. 10 compares the power performance of the SAR ADC with others SAR ADCs reported in the literature with a technology integration scale between 65 nm and 350 nm and resolution between 8 and 12 bits. The performances of the SAR ADC reported in the present work (light squares) stay between the two dashed lines described by the performances claimed in the literature. The SAR ADC

well compares therefore with the literature in terms of dissipated power and sampling rate.

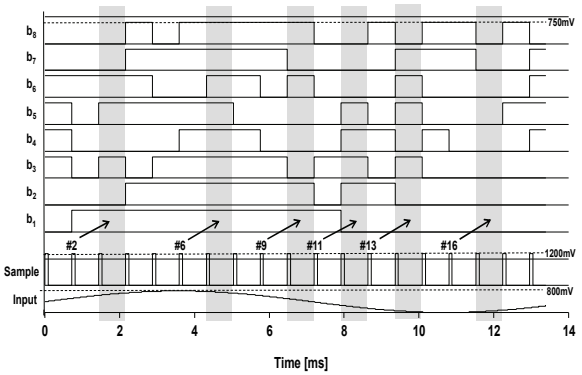


Fig. 9. Digitization outputs.

Fig. 11 shows the Differential Non-Linearity (DNL). The DNL is in the +/-0.05 LSB range for all the codes except for the mid-gap code, where a value of -0.1 LSB is visible. The DNL in Fig. 11 does not take into account the layout of the switched-capacitor DAC, where a common centroid layout and the capacitive parasitics of the interconnections are of great importance [27, 28]. The comparison of the results in Fig. 11 with the literature, where the DNL is usually in the range of tenths of LSB, demonstrates that the DCL proposed in the present work does not affect the linearity and it leaves a large margin for the parasitic capacitances introduced by the layout of the switched-capacitors DAC's.

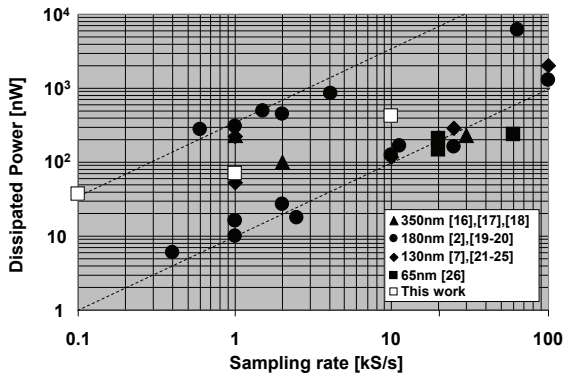


Fig. 10. Power performance comparison.

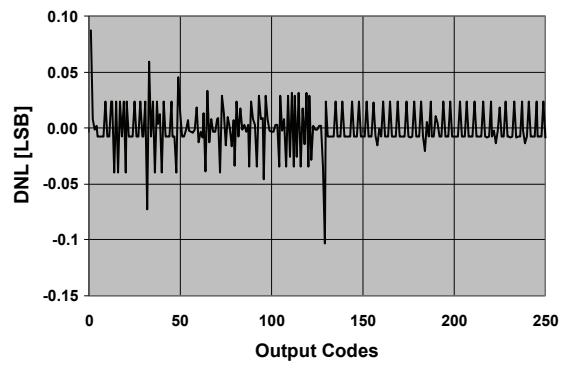


Fig. 11. Differential Non-Linearity.

4. Conclusions

A simplified design of the digital control for a SAR ADC was proposed and proved correctly working in a 130 nm CMOS 8-bit SAR ADC technology. The power dissipated by the DCL was low enough to keep the SAR ADC comparable with the literature in terms of dissipated power and sampling rate. The DCL doesn't affect the non-linearity, leaving margin for the capacitive non-idealities introduced by the layout of the switched-capacitors DAC's.

Acknowledgements

The authors would like to acknowledge STMicroelectronics for providing the 130 nm CMOS technology Design Kit. The technical contribution of Luca Toni is also warmly acknowledged.

References

[1]. T. O. Anderson, Optimum control logic for successive approximation analog-to-digital converters, *The Deep Space Network Progress Report,* TR 32-1526, 1972, pp. 168-176.

[2]. W. Hu, Y-T. Liu, T. Nguyen, D. Y. C. Lie, B. P. Ginsburg, An 8-bit single-ended ultra-low-power SAR ADC with a Novel DAC switching method and a counter-based digital control circuit, *IEEE Trans. on Circuits and Systems*, Vol. 60, Issue 7, 2013, pp. 1726-1739.

[3]. H. T. Russel, An improved successive-approximation register design for use in A/D converters, *IEEE Trans. on Circuits and Systems*, Vol. 25, Issue 7, 1978, pp. 550-554.

[4]. A. Rossi, G. Fucili, Non-rendundant successive approximation register for A/D converters, *Electronics Letters*, Vol. 32, Issue 12, 1996, pp. 1055-1057.

[5]. M. D. Scott, B. E. Boser, K. S. J. Pister, an ultralow-energy ADC for smart dust, *IEEE J. Solid-State Circuits,* Vol. 38, Issue 7, 2003, pp. 1123-1129.

[6]. Y. C. Liang, Z. H. Wu,, B. Li, A new 12-bit fully differential SAR ADC for wireless implantable neural recording system, in *Proceedings of the IEEE Int. Conference on Electron Devices and Solid-State Circuit (EDSSC'09)*, Xian, China, 25-27 December 2009, pp. 399-402.

[7]. D. Zhang, A. Bhide, A. Alvandpour, A 53 nW 9.12 ENOB 1 kS/s SAR ADC in 0.13 um CMOS for Medical Implant Devices, in *Proceedings of the IEEE European Solid-State Circuits Conference (ESSCIRC'11)*, Helsinki, Finland, 12-16 September 2011, pp. 467-470.

[8]. W. Hu, D. Y. C. Lie, Y. T. Liu, An 8-bit single- ended ultra-low_power SAR ADC with a Novel DAC switching method, in *Proceedings of the IEEE Int. Symposium on Circuits and Systems (ISCAS'12)*, Seul, South Korea, 20-23 May 2012, pp. 2349-2352.

[9]. X. Xu, X. Zou, L. Yao, Y. Lian, A 1-V 450-nW fully integrated biomedical sensors interface systems, in *Proceedings of the IEEE Symposium on VLSI Circuits*, *Digest of Technical Paper,* Honolulu, USA, 17-19 June 2008, pp. 78-79.

[10]. X. Zou, X. Xu, L. Yao, Y. Lian, A 1-V 450-nW fully integrated biomedical sensor interface chip, *IEEE J.*

Solid-State Circuits, Vol. 44, Issue 4, 2009, pp. 1067-1077.

[11]. A. T. Do, C. K. Lam, Y. S. Tan, K. S. Yeo, J. H. Cheong, L. Tao, M. T. Tan, M. Je, A 9.87 nW 1 kS/s 8.7 ENOB SAR ADC for implantable epileptic seizure detection microsystems, in *Proceedings of the IEEE Asia and Pacific Conference on Circuits and Systems (APCCAS'12)*, Kaohsiung, Taiwan, 2-5 December 2012, pp. 1-4.

[12]. A. T. Do, C. K. Lam, Y. S. Tan, K. S. Yeo, J. H. Cheong, X. Zou, L. Yao, K. W. Cheng, M. Je, A 160 nW 25 kS/s 9-bit SAR ADC for neural signal recording applications, in *Proceedings of the IEEE Int. New Circuits and Systems Conference (NEWCAS'12)*, Montreal, Canada, 17-20 June 2012, pp. 525-528.

[13]. I. Kianpour, Z. Zou, M. B. Nejad, L. R. Zheng, An 8-bit 166 nW 11.25 kS/s 0.18 um two-step-SAR ADC for RFID applications using Novel DAC architecture, in *Proceedings of the NORCHIP Conference*, Tampere, Finland, 15-16 November 2010, pp. 1-4.

[14]. S. K. Lee, S. J. Park, Y. Suh, H. J. Park, J. Y. Sim, A 1.3 uW 0.6 V 8.7-ENOB successive approximation DAC in a 0.18 um CMOS, *Proceedings of the IEEE Digest Technical Papers Symposium VLSI Circuits*, Kyoto, Japan, 15-18 June 2009, pp. 242-243.

[15]. J. Sauerbrey, D. Schmitt-Landsiedel, R. Thewes, A 0.5-V 1-uW successive approximation ADC, *IEEE Journal of Solid-State Circuits*, Vol. 38, Issue 7, 2003, pp. 1261-1265.

[16]. R. Sekimoto, A. Shikata, H. Ishikuro, A power scalable SAR-ADC in 0.18 um-CMOS with 0.5 V nano-watt operation, in *Proceedings of the IEEE Int. Symposium Access Spaces (ISAS'11)*, Yokohama, Japan, 17-19 June 2011, pp. 89-94.

[17]. Y. Susanti, P. K. Chan, V. K. S. Ong, An ultra low-power successive approximation ADC using an offset-biased auto-zero comparator, in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS'08)*, Macao, China, 2008, pp. 284-287.

[18]. Y. K. Yang, X. Liu, J. Zhou, J. H. Cheong, M. Je, W. L. Goh, A 0.5 V 16 nW 8.08-ENOB SAR ADC for ultra-low power sensor applications, in *Proceedings of the IEEE Int. Microwave Workshop Series RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-Bio'13)*, Singapore, 9-11 December 2013, pp. 1-4.

[19]. H. Zhang, Y. Qin, Z. Hong, A 1.8-V 770-nW biopotential acquisition system for portable applications, in *Proceedings of the IEEE Biomedical Circuits and Systems Conference (BIOCAS'09)*, Bejing, China, 26-28 November 2009, pp. 93-96.

[20]. H. Zhang, Y. Qin, S. Yang, Z. Hong, Design on an ultra-low power SAR ADC for biomedical applications, in *Proceedings of the IEEE Int. Conference Solid-State and Integrated Circuits Technology (ICSICT'10),* Shangai, China, 1-4 November 2010, pp. 460-462.

[21]. S. Al-Ahdab, R. Lofti, W. A. Serdjin, A 1-V 225-nW 1 KS/s current successive approximation ADC for pacemakers, in *Proceedings of the Conference on Ph.D. Research in Microelectronics and Electronics (PRIME'10),* Berlin, Germany, 18-21 July 2010, pp. 1-4.

[22]. K. Abdelhalim, L. MacEachern, S. Mahmoud, A nanowatt successive approximation ADC with offset correction for implantable sensor applications, in *Proceedings of the IEEE Int. Symposium on Circuits and Systems (ISCAS'07)*, New Orleans, USA, 27-30 May 2007, pp. 2351-2354.

[23]. K. Abdelhalim, L. MacEachern, S. Mahmoud, A nanowatt ADC for ultra low power applications, in *Proceedings of the IEEE Int. Symposium on Circuits and Systems (ISCAS'06)*, Kos, Greece, 21-24 May 2006, pp. 1507-1510.

[24]. P. Kamalinejad, S. Mirabbasi, V. C. M. Leung, An ultra-low-power SAR ADC with an area-efficient DAC architecture, in *Proceedings of the IEEE Int. Symposium on Circuits and Systems (ISCAS'11)*, Rio de Janeiro, Brazil, 15-18 May 2011, pp. 13-16.

[25]. A. Rodriguez-Perez, M. Delgado-Restituto, J. Ruiz-Amaya, F. Medeiro, An ultra-low power consumption 1-V, 10-bit successive approximation ADC, in *Proceedings of the IEEE Int. Conference Electronics, Circuits and Systems (ICECS'08)*, St. Julien's, Malta, 2008, pp. 634-637.

[26]. M. Yip, A. P. Chandrakasan, A resolution-reconfigurable 5-to-10 b 0.4-to-1 V power scalable SAR ADC, in *Proceedings of the IEEE Int. Solid-State Circuits Conference (ISSCC'11)*, San Francisco, USA, 20-24 February 2011, pp. 190-192.

[27]. K-H. Ho, H-C. Ou, Y-W. Chang, H-F. Tsao, Coupling-aware length-ratio-matching routing for capacitors arrays in analog integrated circuits, *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 34, Issue 2, 2015, pp. 161-172.

[28] M. Saberi, R. Lotfi, K. Mafinezhad, W. A. Serdijn, Analysis of power consumption and linearity in capacitive digital-toanalog converters used in successive approximation ADCs, *IEEE Trans. on Circuits and Systems*, Vol. 58, Issue 8, 2011, pp. 1736-1748.

(015)

Non-Quasi-Static Large Signal Sub-Circuit Model of AlGaN/GaN HEMT

Nebojsa Jankovic
Faculty of Electronic Engineering Nis, University of Nis, Aleksandra Medvedeva 14, Nis, Serbia
Tel: +381 18 529 338
E-mail: nebojsa.jankovic@elfak.ni.ac.rs

Summary: In this paper, the non-quasi-static (NQS) surface-potential-based large signal model of AlGaN/GaN HEMT yielding continuous static and dynamic characteristics in the whole operation range is described. The model includes some important physical phenomena affecting device DC and transient operation like two-dimensional electron gas (2DEG) quantization, polarization charge, electron velocity saturation, high-field mobility degradation, channel length modulation and the NQS related effect of finite time for the 2DEG charge to build-up. This HEMT model is implemented in SPICE simulator in the form of the equivalent sub-circuit. An excellent fit between the model and the two-dimensional device simulation data from TCAD software is obtained for the DC and switching characteristics of GaN HEMTs with various channel lengths ranging from 1 μm to 10 μm. It is also demonstrated that the quasi-static (QS) modeling approach results in significant errors when predicting the fast switching transient currents of longer-channel GaN HEMTs.

Keywords: Surface-potential, Sub-Circuit, AlGaN/GaN, HEMT model.

1. Introduction

With significant progress in the improvements of quality and performance of GaN HEMTs, the exploitation of full potential of these devices requires the advanced electrical models for circuit simulations. Most GaN HEMT compact models [1, 2] are based on the quasi-static (QS) assumption that ignores the finite time for the 2DEG channel charge to build-up. The QS assumption results in negligible errors when the device is operating at slow rate of change of the terminal voltages that gives enough time for the channel charges to redistribute. However, for higher switching frequencies and/or in longer channel HEMTs, the QS models fails and results in significant errors in AC and transient analysis.

In this paper, the Non-Quasi-Static (NQS) large signal model of AlGaN/GaN HEMT based on the surface-potential (SP) modelling approach [3] is described and implemented in PSPICE.

2. NQS GaN HEMT Model

The NQS HEMT model is implemented in circuit simulator PSPICE in the form of the equivalent sub-circuit as shown in Fig. 1. Unlike the QS models where the gate capacitor node is lumped with both the external source and drain nodes [4], the 2DEG channel of GaN HEMT in NQS model is represented with the N-segment equivalent non-linear RC line as shown in Fig. 1. The core model includes the auxiliary sub-circuit (ASC) computing the boundary surface potentials $\psi_{s,S}$ and $\psi_{s,D}$ at the source and drain ends of the channel, respectively, and the main sub-circuit calculating the drain and source currents Id and Is in SPICE simulations. The main sub-circuit actually emulates the static and dynamic operation of the intrinsic HEMT and can be embedded in the network of extrinsic elements referring to source/drain access regions, gate diode, parasitic capacitances, inductances and contact resistances etc. In present study, only the parasitic capacitances $C_{p,gs,}$ $C_{p,gd}$ and resistances R_s and R_d of the source and the drain access regions, respectively, are included in the NQS HEMT model as shown in Fig. 1. The channel segmental resistance R_i is expressed as [3]:

$$R_i = \frac{w_i \cdot \left(1 - \boldsymbol{\lambda} \cdot V_{DS}^{\mathbf{m}}\right)}{W \cdot q \cdot \mu_n \cdot n_{s,i}}, \qquad (1)$$

where λ and m are fitting parameters of the channel length modulation effect, $n_{s,i}$ is the channel charge density, μ_n is the electron mobility, $w_i = L / N$ is the segmental resistor length, L is the total gate length, W is the channel width and q is the electron charge. The longitudinal and vertical electric filed dependences of μ_n are modelled in (1) with approximate expressions as given in [3]. The longitudinal electric field E_x is easily obtained in the SPSC model of Fig. 1 as:

$$E_x = \frac{\psi_i - \psi_{i-1}}{w_i}. \qquad (2)$$

Finally, the channel charge density $n_{s,i}$ of the i-th segment is approximately expressed with linear function [3]:

$$n_{s,i} \approx \mathbf{a} \cdot \left(V_{gp} - \psi_i\right) + \mathbf{b}, \qquad (3)$$

where $V_{gp} = V_{gs} - V_{off}$ is the effective gate voltage, V_{off} is the channel cut-off voltage, ψ_i is the local channel potential, and ***a*** and ***b*** are the model fitting parameters.

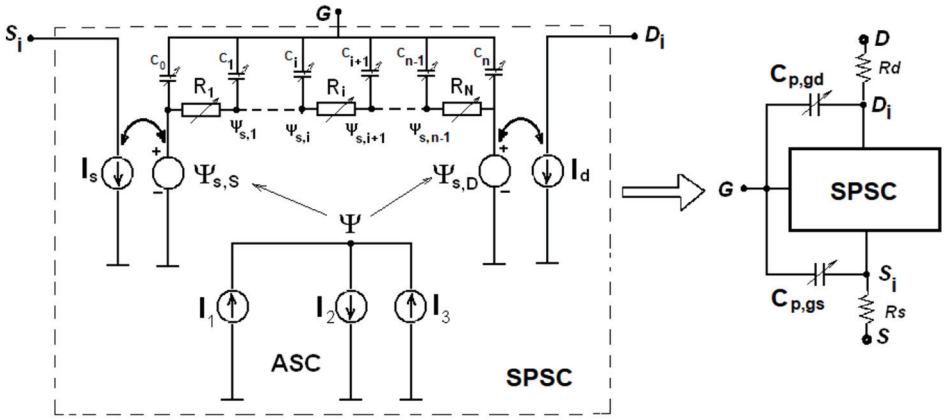
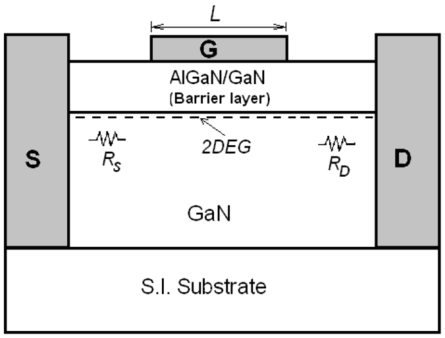


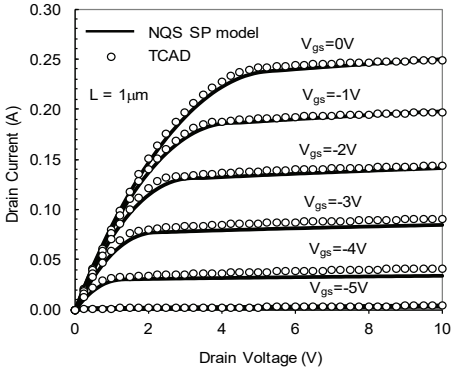
Fig. 1. The NQS equivalent circuit model of AlGaN/GaN HEMT.

3. Results and Discussion

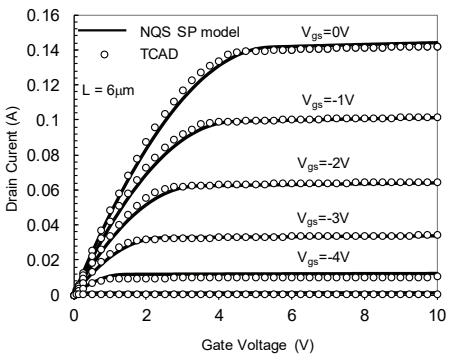
The validity of the Surface-Potential based Sub-Circuit (SPSC) model was proved by comparing with the two-dimensional device simulation data from TCAD software. The schematic cross-section of simulated GaN HEMT is shown in Fig. 2a, Comparisons between simulated and modelled DC output characteristics of the device with various channel lengths L of 1 μm, 6 μm and 10 μm are shown in Figs. 2b, 2c, and 2d, respectively. Note that the thermal effects (device self-heating) are omitted in this study. Using the closed-form analytical expressions for segmental capacitance C_i and resistance R_i, an excellent agreement is obtained between simulated and modeled the gate input capacitance C_{GG} and the gate-drain capacitance C_{GD} extracted for various V_{DS} and V_{GS} from low-frequency AC analysis. These results are shown in Figs. 3(a-c).



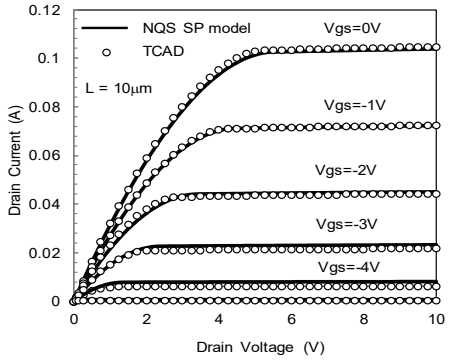
(a)



(b)

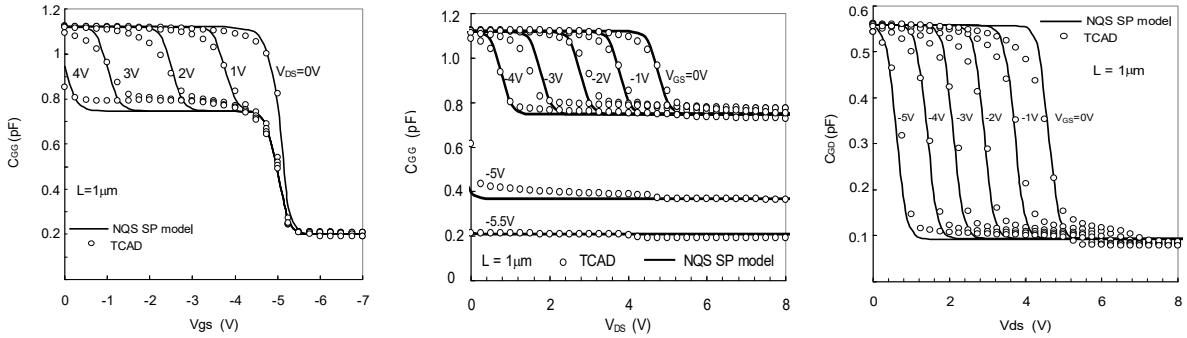


(c)



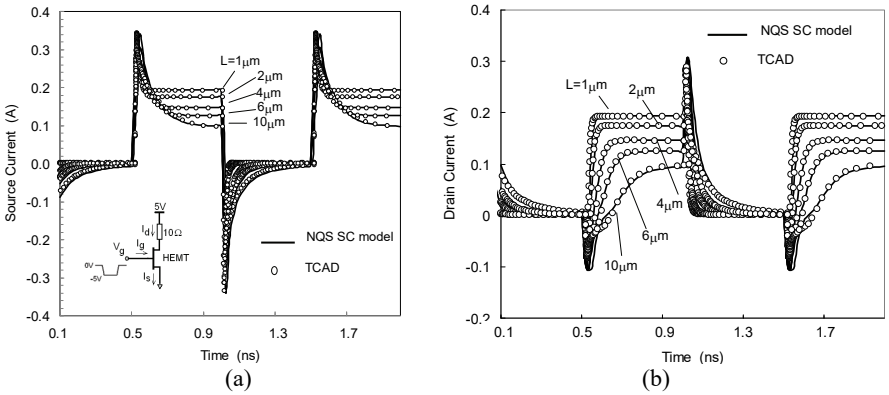
(d)

Fig. 2. Cross-section of GaN HEMT (a) and DC characteristics of the device with L = 1 μm (b), L = 6 μm (c) and L = 10 μm (d).



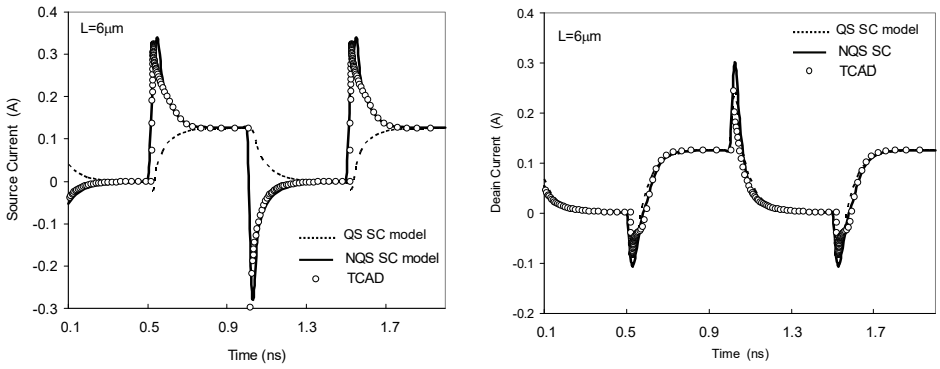
(a) (b) (c)

Fig. 3. Simulated and modeled the gate input capacitance CGG (a), (b) and the gate-drain capacitance CGD (c) for various VDS and VGS.



(a) (b)

Fig. 4. Simulated and modeled: (a) the source and (b) the drain pulse currents assuming 400 μm wide GaN HEMT with L=(1 μm ÷ 10 μm), +5 V power supply, 0 to -5 V periodic gate pulse and 10 **Ω** load resistance (see the inset of (a)).



(a) (b)

Fig. 5. Comparison between the NQS and QS model results with TCAD data. Shown are the source (a) and the drain (b) pulse currents of GaN HEMT with L= 6 μm. The QS model clearly fails to predict the source transient current.

References

[1]. Q. Chen, Latest advances in gallium nitride HEMT modeling, in *Proceedings of the 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ISCIST'14),* 2014, pp. 1-4.

[2]. J. Shanthi, P. Vimala, J. Shanthi, P. Vimala, High electron mobility transistor: A review on analytical models, *International Journal for Innovative Research in Science & Technology*, Vol. 3, 2016, pp. 103-114.

[3]. N. Jankovic, S. Faramehr, P. Igić, A surface-potential based sub-circuit model of I-V characteristics in AlGaN/GaN HEMTs, in *Proceedings of the Small System Simulation Symposium (SSSS 2018),* Niš, Serbia, 12-14 February 2018, pp. 89-95.

[4]. J. Liu, Z. P. Yu, L. L. Sun, An accurate surface-potential based large-signal model for HEMTs, in *Proceedings of the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD'12)*, 2012, pp. 67-70.

(017)

Power and Area Efficient Intelligent Hardware Design for Water Quality Applications

Abheek Gupta [1], Anu Gupta [2] and Rajiv Gupta [3]
[1]BITS PILANI, Rajasthan
[2] Department of Electrical & Electronics Engineering, BITS PILANI, Rajasthan
[3] Department of Civil Engineering, BITS PILANI, Rajasthan
E-mail: anug@pilani.bits-pilani.ac.in

Summary: The paper presents a power efficient and computationally less intensive intelligent hardware using artificial neural network for water quality applications. A compact Hardware Neural Network algorithm has been developed that takes four water quality parameters as the input vector and perform classification of the parameters using a Multilayer Perceptron Network. The computational complexity in the implementation of logistic function has been reduced at a mathematical level by use of approximation methods such as Padé approximation for exponential function and non-linear approximation for sigmoid function. The network improves accuracy of the output by learning by back-propagation of the error. Results show that non-linear approximation method is 34.13 % power efficient and utilises 15.53 % less number of hardware resources in comparison to Padé. ASIC implementation is compact and has 99 % less power consumption as compared to FPGA implementation of the same algorithm.

Keywords: Artificial neural network, Activation function, ASIC, Power efficient, Water quality, FPGA, Computational complexity.

1. Introduction

The aim of the paper is to present a power efficient and computationally less intensive intelligent hardware using artificial neural network for water quality applications. The whole system is designed to be power efficient and will be contained in a handheld device which gives an output in a very easily legible way by classifying the water sample being tested into one of the three classes – potable, agricultural and non-usable.

The classifications and the parameters boundaries are taken as per the standards given by the World Health Organization Drinking Water Quality Standards [1]. A Hardware Neural Network algorithm has been developed that takes four water quality parameters, viz., pH, Oxidation Reduction Potential (ORP), Dissolved Oxygen (DO) and Total Dissolved Solids (TDS) as the input vector and perform classification of the parameters using a Multilayer Perceptron (MLP) Network.

Artificial Neural networks (ANN) have traditionally been implemented using software only or hardware-software co-design approaches for computational simplicity and accuracy [2]. A complete hardware based design, an application specific integrated circuit (ASIC) design approach, involves a trade-off between the accuracy of the calculation vs. the complexity, and power consumption.

A complete hardware based implementation of ANN has been explored by Faiedh, et al. [3] using asynchronous handshaking technique which gives a delayed response. Generally ASIC design approach has proven to be computationally complex but power efficient and area required for design is also reduced drastically as the application specificity of the integrated circuit rules out unnecessary or redundant components from the IC making it suitable for a handheld device. In the present design, both ASIC and field programmable gate array (FPGA) based design methodologies are implemented and performance is compared.

2. ANN Implementation

Various techniques have been used in proposed ANN design to cut down on computational complexity in order to achieve less power consumption. Accuracy is improved by the learning cycle of the network.

2.1. Activation Function Design

The most computationally complex part in hardware implementation of an ANN is the implementation of the activation function as it involves complex non-linear mathematical calculations.

The computational complexity in the implementation of logistic function has been reduced at a mathematical level by use of approximation methods such as Padé approximation for exponential function and non-linear approximation for sigmoid function.

(1) In first method, we use logistic activation function Eq. (1) as the activation function implemented using IEEE 754 floating point representation for Multi-Layer Perceptron architecture.

$$y = \frac{1}{1+e^{-x}}, \quad (1)$$

Padé approximation Eq. (2), as proposed by Zbigniew Hajduk's work [4] has given fairly accurate network outputs despite compromising marginally on mathematical accuracy as compared to other expansions such as Taylor series or McLaurin series. However, the Padé approximation for exponential function is valid only for the input values lying in the interval $0 \leq x \leq 1$.

$$e^x = \frac{1680+840x+180x^2+20x^3+x^4}{1680-840x+180x^2-20x^3+x^4}, \quad (2)$$

This limits the application of the approximation for our project. Fig. 1, shows schematic diagram for Padé approximation using Look up table (LUT) blocks of Xilinx Zynq700 board.

(2) In second method, we implement an approximation of the Sigmoid function as proposed by Zhenzhen Xie [5]. Herein, a Look up table (LUT) based approach is followed, which is particularly suited for FPGA implementation of the sigmoid function. The total domain of the sigmoid function is broken up into shorter intervals and the curve in those intervals is approximated by curve fitting method to simpler polynomials. For our application, since we normalise the input values in the range of [-1, 1], hence, we take up the intervals [-2, -1], (-1, 1) and [1, 2). The polynomials for the said intervals are given by Eq. (3), Eq. (4) and Eq. (5), respectively:

$$y = 0.0467 * x^2 + 0.1239x + 0.2969, \quad (3)$$

$$y = 0.2383x + 0.5, \quad (4)$$

$$y = -0.0467 * x^2 + 0.2896x + 0.4882. \quad (5)$$

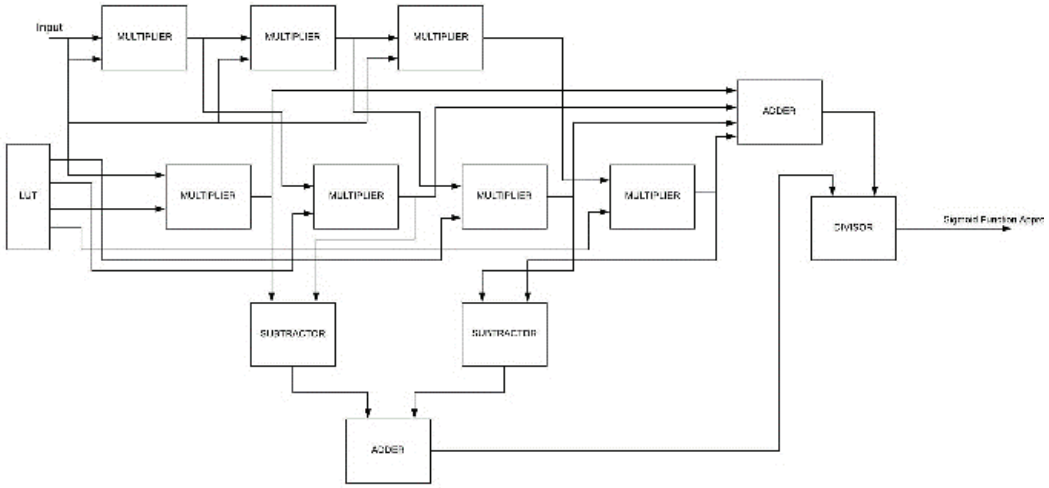


Fig. 1. Schematic Diagram of neuron using Padé Approximation.

3. Power Efficiency and Accuracy of Design

The dynamic power consumption of a single neuron is reduced by replacing sequential units like counters and MAC units by parallel multipliers and adders that perform the calculation in parallel. This also reduces the requirement of storage elements within each neuron.

The network improves accuracy of the output by learning by back-propagation of the error. As the final output of one epoch is generated, an FSM is designed that would generate a signal to start a back-propagation algorithm [6]. This algorithm measures the difference between the desired output and the actual output. The error in the final output is back propagated to all the neurons in the preceding layer while the weights of the current layer are updated. The control of the learning mechanism being synchronized using an FSM gives a time multiplexing to the learning mechanism so as to reduce switching power consumption of the complete network.

4. Results and Comparison

The algorithms have been coded in Verilog and implemented on ZynQ7000 FPGA using Xilinx Vivado. The results of the implementation are shown in Table 1.

Table 1. Comparison of two implementations of Activation Function in FPGA based design.

Implementation	MUX	LUT	DSP	Power (FPGA) (W)	Power (ASIC) (W)
Padé approximation	15	3578	18	5.95	3.75×10^{-4}
Non-linear approximation	14	3144	12	5.3	2.47×10^{-4}

The power consumption of the FPGA implementation were very high. Thus, we synthesized the design using ASIC design methodology. The ASIC

was synthesized using Cadence Encounter RTL Compiler tool with UMC 90 nm standard cell library. The power consumption of a neuron using Padé approximation dropped from 5.95 Watts on FPGA to 3.75×10^{-4} Watts in ASIC synthesis. Similarly for the Non-linear approximation method the power consumption of a single neuron drops from 5.3 Watts on FPGA to 2.47×10^{-4} Watts for ASIC synthesis. Padé approximation method makes use of 25538 Cells covering 241897 nm^2 of the library as compared to 21571 cells covering 196997 nm^2 for nonlinear approximation method.

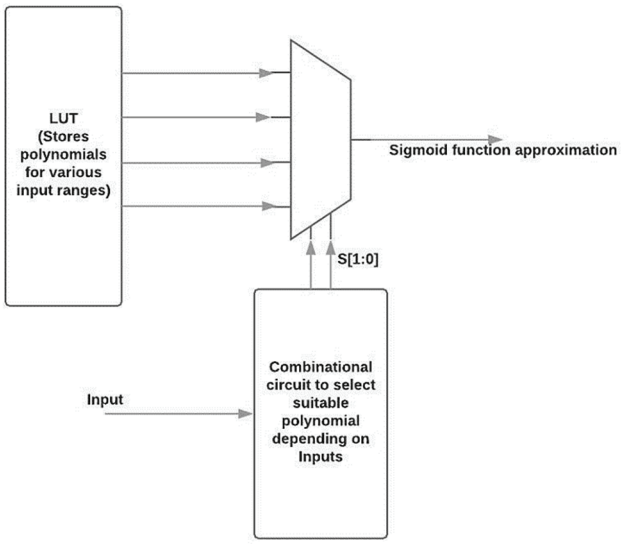


Fig. 2. Schematic diagram of for nonlinear approximation.

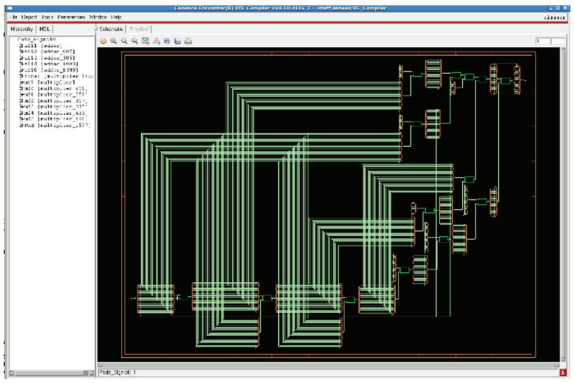


Fig. 3. ASIC implementation of Padé approximation.

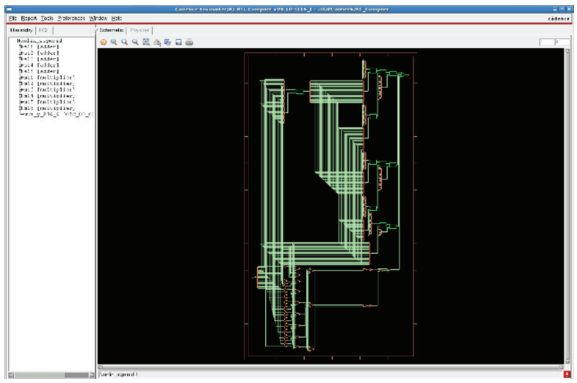


Fig. 4. ASIC Implementation of a Nonlinear Approximation of Sigmoid function.

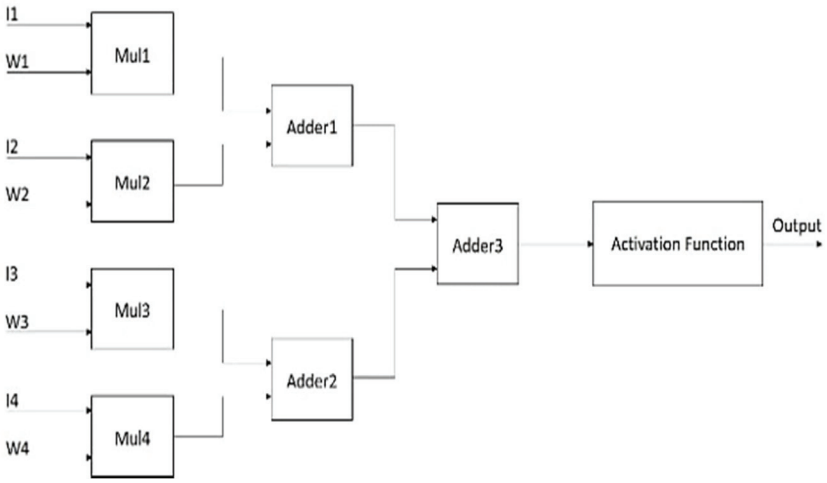


Fig. 5. Basic structure of a Neuron.

5. Conclusions

From the results shown in Table 1, non-linear approximation method is found to be more suited to proposed design for water quality application. It also is much more power efficient and utilizes much less number of hardware resources. However, FPGA implementations are consuming much higher power. Thus we have changed to a compact ASIC implementation of the network designed. The ASIC implementation shows drastic drops in power consumption of the system as compared to FPGA implementation.

Acknowledgements

Financial support for project entitled "Conjunctive use of Rainwater and Groundwater to provide safe drinking water with intervention of Advanced Technology" No. DST/TM/WTI/2K16/204(G), Government of India, Ministry of Science and Technology, Department of Science and Technology, New Delhi, India.

References

[1]. Guidelines for Drinking-Water Quality, 4th Edition, Vol. 3, *World Health Organization*, 2011.

[2]. P. Ferreira, P. Ribeiro, A. Antunes, F. M. Dias, Artificial neural networks processor – A hardware implementation using a FPGA, in *Proceedings of the International Conference on Field Programmable Logic and Applications (FPL'04)*, 2004, pp. 1084-1086.

[3]. L. K. Faiedh, G. Hassene, T. Zied, B. Kholdoun, Digital hardware implementation, in *Proceedings of the 16th International Conference on Microelectronics (ICM'04)*, 2004, pp. 551-554.

[4]. Z. Hajduk, High accuracy FPGA activation function implementation for neural networks, *Neurocomputing*, Vol. 247, 2017, pp. 59-61.

[5]. Z. Xie, A Non-linear Approximation of the sigmoid function based on FPGA, in *Proceedings of the IEEE Fifth International Conference on Advanced Computational Intelligence (ICACI'12),* 2012, pp. 221-223.

[6]. A. Savich, M. Moussa, S. Areibi, A scalable pipelined architecture for real-time computation of MLP-BP neural networks, *Microprocess. Microsyst.*, Vol. 36, Issue 2, 2012, pp. 138-150.

(018)

Investigation on Body Potential in Cylindrical Gate-All- Around MOSFET

M. Kessi, A. Lakhelef and A. Benfedila
Micro and Nanotechnology Research Group (MNRG), Faculty of Electrical Engineering and Computer Sciences, University M. Mammeri, Tizi-Ouzou, UMMTO DZ 15000, Algeria
E-mail: benfdila@ummto.dz, abenfdil@ictp.it

Summary: Cylindrical gate all around (CGAA) MOSFET has been studied and the body potential has been simulated and studied. The center and surface potentials models are studied and a comparison is made between the two potential behaviours for a CGAA MOSFET. Moreover, the channel doping concentration and the band diagrams are obtained using the finite element numerical method by solving Poisson's equation in the cylindrical coordinate system.

Keywords: Gate-All-Around MOSFET, Finite elements, I-V Characteristics, Short channel effects, Nanotransistor, Center potential, Surface potential.

1. Introduction

As MOSFETS continue to get smaller between source and drain has led to an impending power crisis and reduces the capability of gate electrode to control the body potential distribution in the channel. The short-circuit from source and drain is facing serious problems, like Drain Induced Barrier Lowering (DIBL) and the threshold voltage roll off [1]. As a result the off state current increases and the On-Off current ration are degraded. Several designs structures (MuGFETs) have been developed, all of them are targeting the enhancement of the better channel control due to the action of multiple gate electrodes surrounding the channel [2]. Cylindrical Gate-All-Around MOSFETS have been regarded as a promising technology for sub-10-nm CMOS devices, because has provide the best short channel device performance, better gate controllability, suppressed floating-body, improved transport property and CMOS compatibility, compared with other non-classical device structures, because do not have corner effects due to the circular cross-section and cylindrical body [1, 2]. Moreover, the center and surface potential of the CGAA structure has been investigated and the comparison is made with them.

2. Device Structure and Parameters

The schematic diagram of the Cylindrical GAA (CGAA) MOSFET structures used for simulation is shown in Fig. 1. The radial directions are assumed to be along radius and lateral direction along z-axis of the cylinder. The details of device physical parameters used in the structure are shown in Table 1.

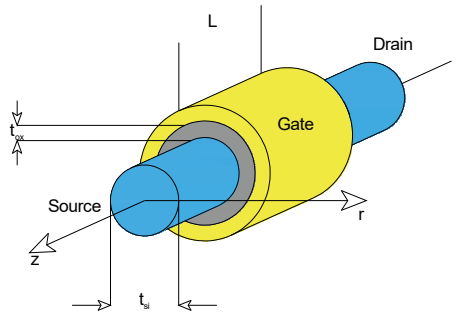


Fig. 1. Schematic structure of Cylindrical Gate-All-Around (CGAA) MOSFETS.

Table 1. Values of various parameters used in simulation.

Symbol	Parameter	Value
N_a	Impurity doping in the channel	10^{16} cm^{-3}
N_d	Impurity doping in source and drain	10^{20} cm^{-3}
R	Channel radius	5 nm
t_{si}	Silicon film thickness	10 nm
L_S, L_D	Length of source and drain	5 nm
t_{ox}	Oxide thickness	2 nm
L	Channel length	30 nm
ε_0	Permittivity of vacuum	8.8×10^{12} F/m
ε_{si}	Permittivity of silicon	$11.85\times\varepsilon_0$
ε_{ox}	Permittivity of oxide	$3.9\times\varepsilon_0$
T	Absolute temperature in Kelvin	300 K
Φ_M	Metal work function	4.6 eV

3. Results and Discussion

In this section, results obtained from numerical simulation of the potential distribution Φ(r, z) in the source-channel-drain region. The center and surface potential has been obtained by solving the following 2-D asymmetric Poisson's equation in cylindrical coordinate system.

The center potential, Φ(0, z), and the surface potential, $\Phi(t_{si}/2, z)$ for the CGAA MOSFET are compared in Fig. 3 and Fig. 4 at different gate to source voltage.

Fig. 2 illustrates the energy band diagram of both the CGAA. The band diagrams are along the radius of the circular cross-section.

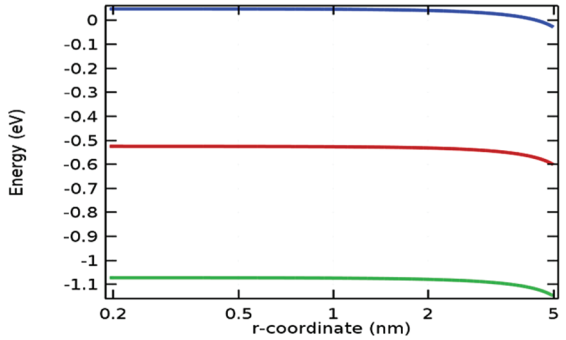


Fig. 2. Band diagram in the both (Si) (r axis) of a CGAA.

Figs. 3 and 4 show the variation of the surface and center potential along the source-channel-drain for different gate to source voltage of CGAA MOSFET. When the gate to source voltage is reduced, the controllability of the gate voltage over the channel becomes stronger in comparison with the influence exerted by the source/drain.

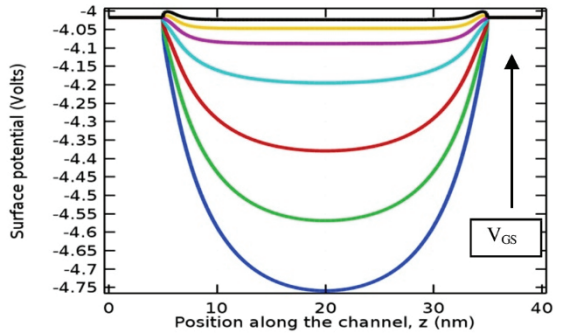


Fig. 3. Surface potential along the channel length at various gate voltages V_{GS} (start: -0.2 V, step: 0.2 V, stop: 1 V) and V_{DS} = 0 V.

Figs. 5 and 6 display the comparison of the surface and center potential along the source-channel-drain at various gate to source voltage of CGAA MOSFET with two value of drain voltage (V_{DS} = 0 V and V_{DS} = 0.9 V). It can be noted that source channel barrier height at channel center is lower than that of the surface. The presence of DIBL effect can be easily observed from Fig. 4 as the center and surface potential minima point shows an upward movement with the increasing of drain voltage. The threshold voltage depends on the drain bias, gate length, body and oxide thickness, gate work function, doping profile, etc. In this paper, only the gate length, drain bias, are taken as parameters.

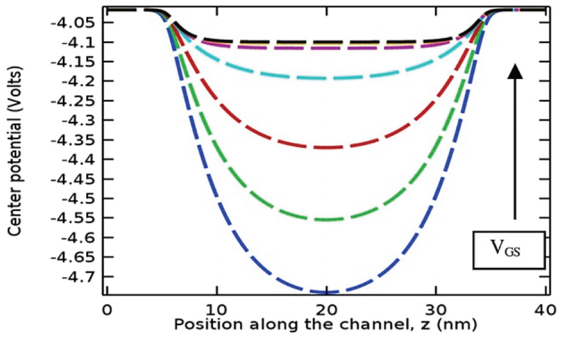


Fig. 4. Center potential along the channel length at various gate voltages (start: -0.2 V, step: 0.2 V, stop:1 V) and V_{DS} =0 V.

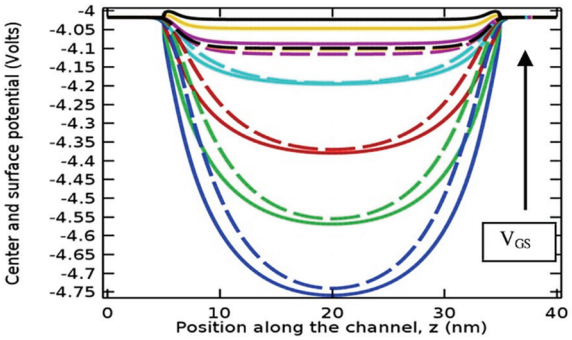


Fig. 5. Comparison of the center and surface potential along the channel at various gate voltage V_{GS} (start:-0.2, step: 0.2 V, stop: 1 V) and V_{DS} = 0 V.

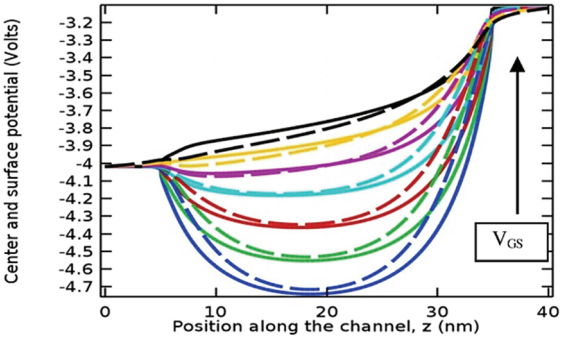


Fig. 6. Comparison of the center and surface potential along the channel at various gate voltages V_{GS} (start: -0.2, step: 0.2 V, stop: 1 V) and V_{DS} = 0.9 V.

4. Conclusions

In this paper, we have studied the potential distribution in the body of the Cylindrical Gate-All-Around (CGAA) MOSFET$_S$, using the finite element, numerical method by solving the Poisson's equation in the cylindrical coordinate system. The results show excellent accuracy comportment of the potential in the channel of CGAA.

References

[1]. T. K. Sachdeva, Dr. S. K. Aggarwal, Dr. A. K. Kushwaha, Design, analysis and simulation of 30 nm cylindrical gate all around MOSFET, *IJARCCE*, Vol. 5, Issue 10, October 2016, pp. 358-360.

[2]. M. Kessi, A. Benfdila, A. Lakhlef, Investigation on cylindrical gate-all-around (GAA) tunnel FETS scaling, in *Proceedings of the 30th International Conference on Microelectronics (MIEL'17),* Niš, Serbia, 2017, pp. 199-202.

(021)

Simulation of Low-Temperature Crystallization in Germanium Thin Films

Y. Kogure, T. Funayama and Y. Uchida
Teikyo University of Science, Adachi-ku, Tokyo, Japan
Tel.: +81-047-411-6265
E-mail: kogure@ntu.ac.jp

Summary: Low-temperature crystallization of germanium thin films has been simulated by means of molecular dynamics. Tersoff bond order potential was adopted for calculating the interactions between germanium atoms. Amorphous model was prepared by quenching the molten system at 1800 K. The model was consisted of about 1000 or 5000 atoms and free boundary condition was adopted. Then these amorphous systems were kept at temperatures, 400 K or 600 K, for 500,000 steps and crystallization was really observed. To investigate the atomistic process of crystallization the cross sectional view of the atomic configuration, the change of the mean potential energy, the radial distribution function and the trajectory of atomic displacement were evaluated. Boundary conditions between the sample and the substrate were investigated in detail.

Keywords: Germanium, Molecular dynamics, Crystallization, Amorphous, Radial distribution function, Tersoff potential.

1. Introduction

Metal induced crystallization has been extensively studied as a powerful method of crystallization. The present authors have been engaged in the study to fabricate the germanium thin films on the flexible substrates in the project to improve the yes/no device for TLS patients, however it is not yet to be usable [1]. Problems are fitting and durability to use in daily life. In our experimental study germanium films are deposited at 60 ℃ and crystallized at 150 ℃ (423 K). However, the microscopic process of the mechanism of crystallization is not well understood in many cases. Molecular dynamics simulation using reliable interatomic potential is a powerful way to visualize microscopic processes of crystallization. One of the present authors has been applied the molecular dynamics simulation on the studies of crystal defects and mechanical properties of metals [2]. The program code developed in the studies can be used in the present investigation.

2. Method of Simulation

The bond order potential function developed by Tersoff et al, is used in the simulation. The potential energy depends on the bond length and bond angle. The potential energy is described as

$$E = \sum_i E_i, \qquad E_i = \frac{1}{2}\sum_{j \neq i} V_{i,j}, \tag{1}$$

$$V_{ij}(r) = f_C(r)[f_R(r) + b_{ij} f_A(r)], \tag{2}$$

$$\begin{aligned} f_R &= A\exp(-\lambda r), \\ f_A &= -B\exp(-\mu r), \end{aligned} \tag{3}$$

where b_{ij} is related to the coordination number and represent the many body nature of the potential. The truncation function $f_C(r)$ and other variables are described as

$$f_C(r) = \begin{cases} 1, & r < R \\ \frac{1}{2} + \frac{1}{2}\cos\left[\pi \frac{(r-R)}{S-R}\right], & R < r < S \\ 0, & r > S \end{cases}, \tag{4}$$

$$\begin{aligned} b_{ij} &= \kappa_{ij}(1 + \beta^n \zeta_{ij}^n)^{-1/2n}, \\ \zeta_{ij} &= \sum_{k \neq i,j} f_C(r_{ik}) g(\theta_{ijk}), \\ g(\theta_{ijk}) &= 1 + \frac{c^2}{d^2} - \frac{c^2}{d^2 + (h - \cos\theta_{ijk})^2}. \end{aligned} \tag{5}$$

The force acting on an atom is calculated by differentiating the expression for energy, Eq. (1), by distance *r*. The equation of motion an atom is solved by integrating the potential numerically by the Verlet algorithm. The time interval for the numerical integration is chosen to be $\Delta t = 1.0 \times 10^{-15}$ sec , which is much smaller than the period of the atomic thermal vibration.

The molecular dynamics simulations are performed by using a FORTRAN code developed the present authors and results are visualized by Visual Basic 6 (Microsoft)

3. Results and Discussion

3.1. Particle-like Samples

For the simulation to investigate the fundamental mechanism of crystallization a small specimen consists of 1332 atoms is prepared. As an initial

condition, atoms are arranged in diamond structure with {100} boundary surfaces as shown in Fig. 1(a). The length of one side of cube is about 3 nm. The radial distribution function (RDF) of the structure is also shown in the right. The free boundary condition is adopted. Then the temperature is increased up to 1800 K. The molten state is quenched and amorphous state is realized.

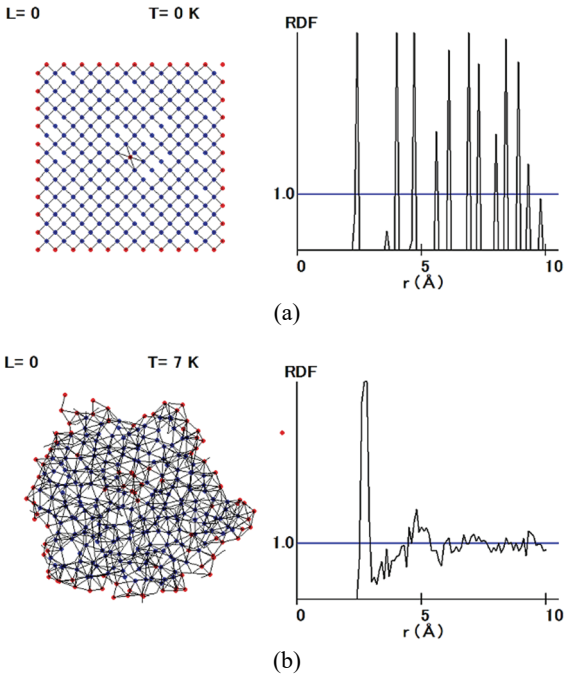


Fig. 1. Configuration of atoms (a) in perfect crystal and (b) in amorphous state. The radial distribution functions are shown in right hand side.

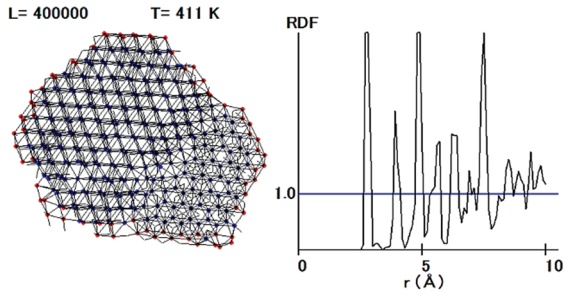


Fig. 2. Configuration of atoms and radial distribution function in crystallized state.

The atomic structure and the RDF of amorphous state are shown in Fig. 1(b). A completely disordered structure of amorphous is seen.

The simulation of the low temperature crystallization starts from the amorphous state.

The temperature of the amorphous specimen was maintained at 411 K and 600 K. As an example of the structure of crystallized sample at 400 K is shown in Fig. 2. It is seen that the sample is consisted of two grains and the RDF in right hand side shows a spike-like change characteristic of crystal is seen. The potential energy can be calculated by Eq. (1). The change of the potential energy is shown in Fig. 3. It monotonically decreases at the first 100 thousand steps, and the first crystallization is completed in this time domain. After that, the potential energy slightly increases and decreases again. Changes in grain structure occur in this region. The grain structures at typical time steps, (a) 100000, (b) 250000, (c) 400000, are also shown in the figure. The grain structure in the specimen is changing at the constant temperature. It is also seen that the outer shape of the sample also changes. It can be understood that the free surfaces of the specimen plays an important role in polycrystallization. In some cases, several tens of atoms were released from the sample to the outside, and crystallization occurred as a result of this. This may be related to collective motion of metal atoms promoting crystallization. Crystallization seems to have accidental features. Even in the simulation with the set temperature of 600 K, the same behavior was quantitatively observed.

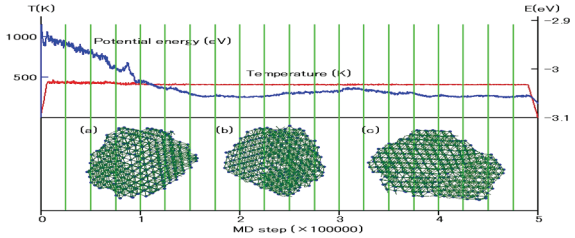


Fig. 3. Change of potential energy and typical grain structures at 400 K.

3.2. Plate-lile Samples

A flat plate sample was prepared to simulate crystallization in the state close to a thin film. This is composed of 4852 atoms in the form of four particles arranged in the horizontal direction (Fig. 1(a)) in the previous section. The temperature of this sample was raised to 1,800 K to bring it into a molten state, then quenched to realize an amorphous state (Fig. 4(b)).

Simulation of polycrystallization was performed using this amorphous state as an initial state. Two types of boundary conditions are adopted between the substrate and the sample in the simulation: (i) the substrate and the sample are in close contact and Atoms can slide on the surface, (ii) Loose contact with the base plate (allowing withdrawal within 5 A).

In the boundary condition (i), crystallization has hardly progressed because atoms are mostly fixed at the lower end of the sample. On the contrary, in the boundary condition (ii), it can be seen that polycrystallization is more advanced because of the boundary condition close to the free surface even at the lower end. Fig. 6 shows the time change (step) of the average potential energy of atoms in the sample, with the blue lines for the boundary condition (i) and the red lines for the boundary condition (ii). The upper graph shows the results for 400 K and the lower graph shows the results for 600 K, and both have similar behavior. In the boundary condition (i), the potential energy is almost constant. On the contrary, it can be seen that in

the boundary condition (ii), after the initial violent rise and fall, it is relaxed to a lower level. It seems that energy is reduced by polycrystallization.

The trajectories of the movement of atoms in the sample during the crystallization process under each boundary condition are shown in Fig. 7. Results for 400 K and 600 K are summarized. Small solid circles indicate the initial position of each atom, and the curve following it indicates the trajectory of movement. In accordance with Fig. 6, the result of the boundary condition (i) is shown by blue lines and the result in (ii) is shown by red. In the boundary condition (i), it can be seen that small horizontal movements occur at both temperatures. In the boundary condition (ii), large motion with rotation is seen at 400 K. At 600 K, large horizontal movements also occurs. Investigating the microscopic behaviors of atoms as described above is useful in studying the mechanism of crystallization.

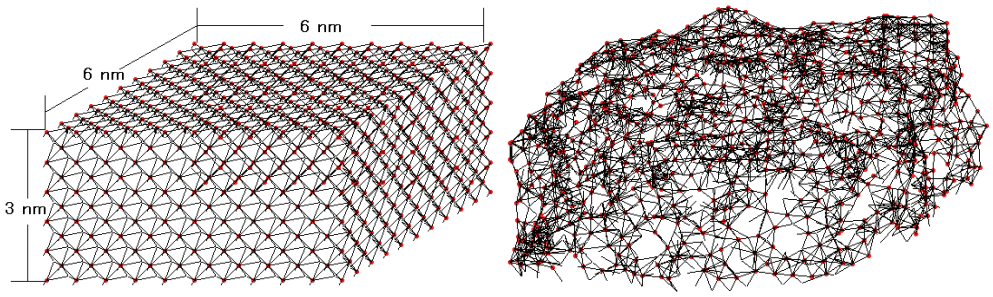


Fig. 4. Preparation of plate-like sample.

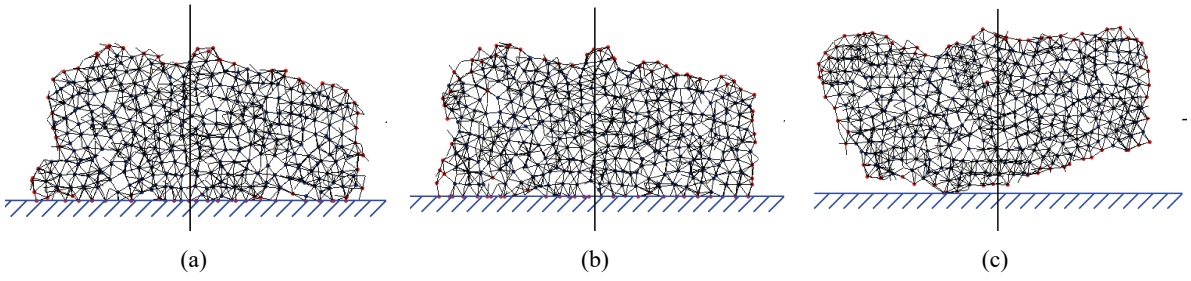


Fig. 5. Cross-sectional view of the plate-like sample. (a) initial smorphous state, (b) after annealing under boundary condition (i), and (c) under boundary condition (ii).

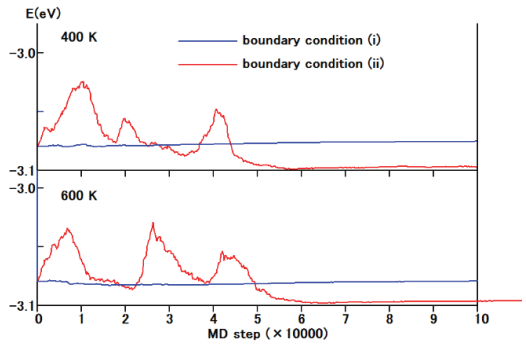


Fig. 6. Change of the mean potential energy.

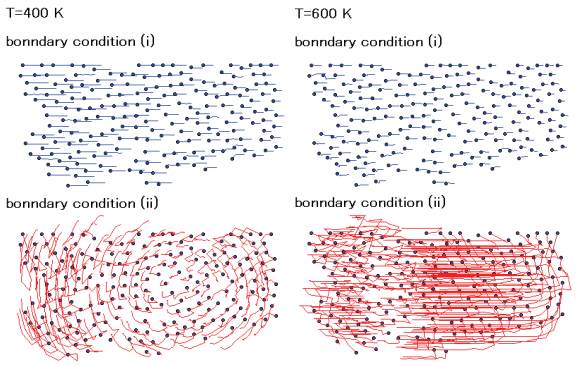


Fig. 7. Trajectory of atoms at 400 K and 600 K under the boundary conditions (i) and (ii).

4. Conclusions

Low-temperature crystallization of amorphous Ge has been simulated by using the empirical Tersoff potential. The crystallization is observed at the temperatures 400 K and 600 K. The process of crystallization was monitored thorough the cross sectional view of the atomic structure and the RDF. Change in the potential energy associated with the crystallization was observed. Boundary conditions between the sample and the substrate were investigated in detail for the plate-like samples. These results seem to be useful for the development of medical devices.

References

[1]. Y. Uchida, T. Funayama, Y. Kogure, W. Yeh, Low-temperature Cu-induced poly-crystallization of electrodeposited germanium thin film on flexible substrate, *Physica Status Solodi C*, Vol. 13, 2016, pp. 864-867.

[2]. Y. Kogure, Y. Hiki, Atomistic simulation of shear mode deformation of nanocrystalline copper with different grain sizes, *Materials Transactions*, Vol. 55, Issue 1, 2014, pp. 64-68.

(025)

TCAD-RAD Subsystem for BJT/HBT and MOSFET Structures Simulation Taking into Account Radiation Effects

K. O. Petrosyants, M. V. Kozhukhov and D. A. Popov
National Research University Higher School of Economics (Moscow Institute of Electronics and Mathematics), 34 Tallinskaya, 123458, Moscow, Russia
Tel.: +7-495-772-9590,15208
E-mail: kpetrosyants@hse.ru

Summary: The universal TCAD-RAD software version is presented for bipolar and MOSFET structure modeling taking into account neutron, electron, gamma, proton irradiation. The new set of adequate radiation models for physical based parameters of BJT/HBT and MOSFET structures is developed and built-in Sentaurus Synopsys software tool. For bipolar and MOS devices used for radiation hardened BiCMOS ICs design the good agreement for simulated and experimental I-V characteristics is achieved. The error is not more than 10-20 %.

Keywords: bipolar and MOS transistors, neutron, electron, gamma, proton irradiation, radiation induced device parameters degradation, device modeling, TCAD software.

1. Introduction

The electronic devices employed in space vehicles, RF and telecommunication systems, nuclear energy control, military and other systems are subjected to different types of irradiation (neutrons, electrons, gamma rays, protons, heavy particles and others). To provide the reliable operation range of the electronic devices under irradiation conditions the special strategy "radiation hardened by design" is used. The key point of this strategy is consistent device modeling taking into account radiation effects.

2. State-of-the-Art

In most publications, the experimental characteristics of irradiated devices are presented. But there are few works on the TCAD simulation of BJT/HBT and MOSFET structures after radiation influence. Unfortunately, in this line the possibilities of the common-used commercial TCAD software tools [1, 2], are limited to simple particular cases for traditional device structures. Besides they don't contain radiation-dependent physical parameters for novel device structures. The special rad-oriented system [3] takes into account only gamma rays and single events and doesn't account for neutrons and protons.

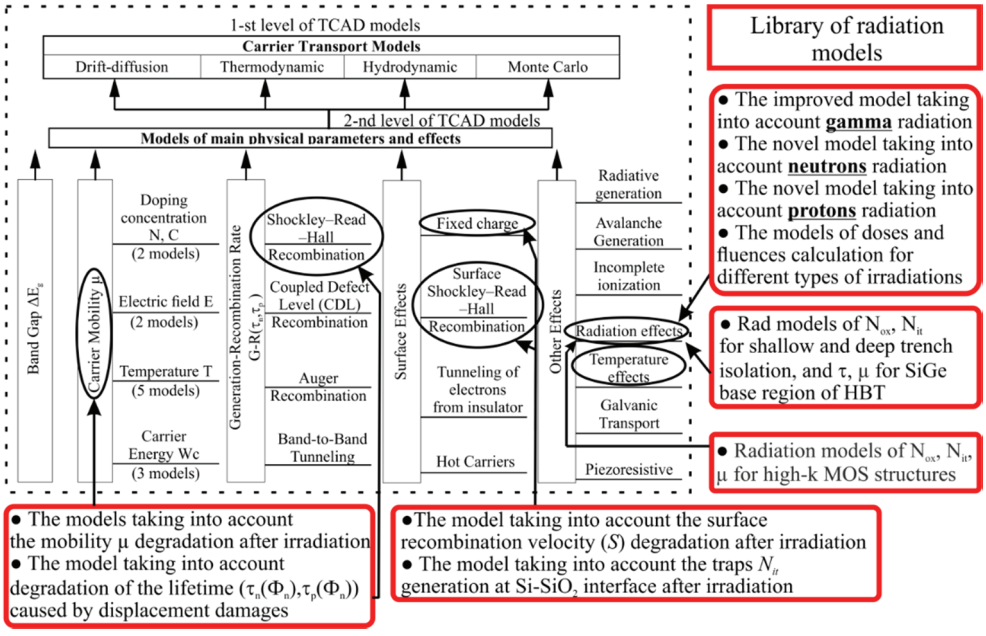


Fig. 1. Radiation models of device electro physical parameters included in the TCAD-RAD system.

3. TCAD-RAD Subsystem

In this work, the universal TCAD-RAD subsystem is presented. It consists of two parts: standard Sentaurus Synopsys software core [1] and the special library of radiation models for physical parameters and electrical characteristics of BJT/HBT and MOSFET structures taking into account neutron, gamma-rays and proton irradiation. Note that the models for neutrons and protons were not included in TCAD formerly.

The LIBRARY consists of 4 segments:

Common controller carries two functions: 1) selection for given type of irradiation the set of radiation-dependent physical parameters and their models which are responsible for device electrical characteristics degradation; 2) conversion the energy or dose rate of particles into total dose D and/or fluence Φ;

Gamma radiation models are based on carrier ionization effects. The adequate models of radiation-dependent parameters (N_{ox}, N_{it}, S_0, μ) for novel Si BJT/ SiGe HBT and for MOSFET/SOI MOSFET with high-k gate oxide structures are added [4];

Neutron models are based on displacement effects. The adequate models of radiation-dependent parameters (τ, μ, n/p) are included. They take into account the dependencies on neutron fluence, doping levels injection effectivities of electrons and holes [5];

Proton model was developed by authors [6]. It is based on additive approach combined the ionization and displacement effects influence on device structure.

4. Library of Radiation Models

The basic physical parameters describing the carrier transportation (μ_n, μ_p), surface (S_n, S_p) and volume (R_n, R_p) recombination, charge collection in bulk (Q_n, Q_p) and oxide (Q_{ox}) volumes, and on semiconductor/oxide interfaces (Q_{it}) are radiation-dependent.

So the library of physical parameter models for different types of irradiation is the key element of the TCAD-RAD software tools. In the wide-used commercial TCAD tools [1, 2] the library of radiation models is poor and not applicable for most practical requirements.

In this work the version of Synopsys Sentaurus RAD tool with the complete library of radiation-dependent physical parameter models valid for gamma rays, neutron and proton irradiation is presented.

a. Gamma radiation models. Irradiation of BJTs/HBTs and bulk/SOI MOSFETs by gamma-rays results in the generation of electron-hole pairs in bulk silicon regions; the increase of surface recombination velocity (S) and volume recombination rate (R); creation of traps at the Si-SiO_2 interfaces (N_{it}); collection of positive charge in the gate/STI/BOX oxide (Q_{ox}); decrease of carrier mobility (μ).

For BJTs/HBTs it leads to base and collector leakage currents increase, current gain and maximal/cut-off frequencies degradation; for MOSFETs – to gate/drain leakage current increase, threshold voltage (V_{th}) and subthreshold slope (S) degradation.

In the commercial TCAD version only one degradation factor – the space charge in SiO_2 oxide (Q_{ox}) dependence on gamma dose is taken into account correctly.

Therefore, in order adequately to take into account all the factors caused by gamma radiation influence on the characteristics of Si BJTs/SiGe HBTs and bulk/SOI MOSFETs it is necessary additionally to introduce into TCAD tool the physical expressions for the concentration of traps N_{it} and the surface recombination velocity S at the interfaces Si-SiO_2 depending on the absorbed dose of gamma radiation $D\gamma$:

$$N_{it}(D_\gamma) = a_{it} \cdot D_\gamma^{\,b_{it}}, \qquad (1)$$

where a_{it}, b_{it} are the fitting parameters that have different values for EB spacer and STI/DTI surfaces.

The model parameters a_{it}, b_{it} are defined from experimental dependencies of Si-SiO_2 interface traps concentrations on absorbed dose D_γ [7] (see Fig. 2).

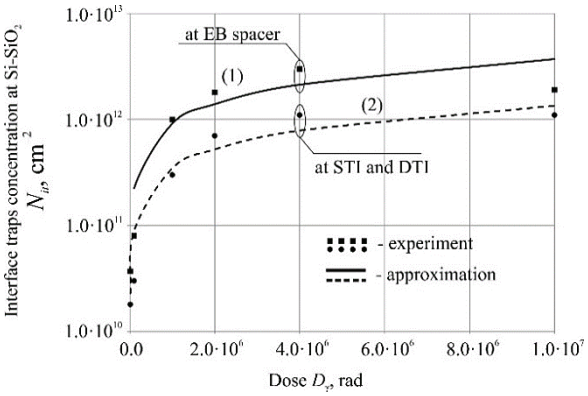


Fig. 2. Dependence of traps concentration at Si-SiO_2 interfaces of EB spacer and shallow and deep trench isolation on absorbed dose D_γ.

The surface recombination velocity is proportional to the density of traps at Si-SiO_2 interfaces [8, 9]:

$$S(D_\gamma) \cong \sigma v_{th} N_{it}(D_\gamma), \qquad (2)$$

where $\sigma = \sqrt{\sigma_n \cdot \sigma_p}$, σ_n, σ_p are the capture cross-sections for electron and hole traps; v_{th} is the thermal velocity.

The modified dependence on radiation dose for the charge carrier mobility μ_{eff} was introduced. The model takes into account the mobility decrease caused by radiation induced surface states on the SiO_2/Si interfaces:

$$\mu_{\text{eff}}(\text{D}) = \frac{\mu_0}{1+\alpha N_{it}(D)}, \qquad (3)$$

where μ_0 is the pre-rad mobility, $N_{it}(D)$ is the silicon-oxide interface trap density, α is a fitting parameter.

Note that the developed models of radiation-dependent parameters (N_{it}, S, Q_{ox}, μ) for novel deep submicron SiGe HBT [6] and high-k gate SOI MOSFET [4, 10] structures differ from the corresponding models for conventional BJT and MOSFET structures. For example in Fig. 3 the radiation-dependent parameter N_{it} at HfO_2, BOX and STI interfaces of 45 nm MOSFET with HfO_2 gate oxide is presented.

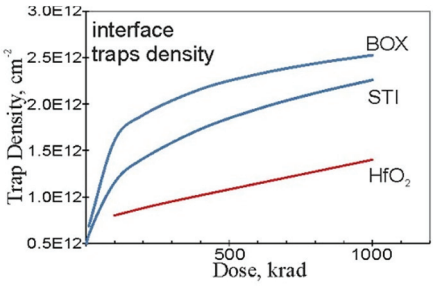


Fig. 3. Trap densities N_{it} at different interfaces of 45 nm MOSFET with HfO_2 gate oxide structure.

The dependences of recombination velocity $S(D_\gamma)$, the traps concentration $N_{it}(D_\gamma)$ at Si-SiO_2 interfaces of EB spacer and STI/DTI and carrier mobility $\mu(D_\gamma)$ on absorbed dose were included in the Synopsys Sentaurus using the physical model interface (PMI).

b. Neutron radiation models. The silicon physical parameters, such as the lifetime of the minority charge carriers (τ), mobility (μ) and the concentration of nonequilibrium charge carriers (n/p), are degraded after impact of neutrons in consequence of the displacement defects formation [11]. The decrease of the minority carrier lifetime is the main factor that influences on the device characteristics. For BJTs/HBTs it is the increase of base current, reduction of the current gain and cut-off/maximum frequencies.

For MOSFETs it is the transconductance g_m and saturation current I_{sat} decrease, and the shift of threshold voltage ΔV_{th}.

In all the commercial versions of TCAD the minority carrier lifetimes τ_n, τ_p are not depended on radiation influence.

So for simulation of minority carrier lifetime decrease due to displacement effects after neutron irradiation the following equation was introduced:

$$\frac{1}{\tau_\phi} = \frac{1}{\tau_0} + \Phi_n \cdot K_\tau, \qquad (4)$$

where τ_0, τ_Φ are the minority carrier lifetimes before and after irradiation; Φ_n is the neutron fluence; K_τ is the coefficient of radiation-induced alteration of carrier lifetime.

It was shown experimentally that for modern npn and pnp Si BJTs/SiGe HBTs the parameter K_τ in (4) depends on the doping concentration N_{dop} and the injection efficiency $\delta = n_{min}/n_{maj}$ (where n_{min}, n_{maj} – minority and majority carrier concentrations) [12, 13]. Therefore, the special equation for K_τ (δ, N_{dop}) was introduced [6].

The expression (4) for the lifetime with alteration coefficient K_τ (δ, N_{dop}) was added to the standard Shockley-Read-Hall recombination model using the PMI. Along with the radiation effects, the developed model (4) takes into account the dependence of the lifetime on the temperature. The combined influence of radiation and temperature is the important factor for modern Si BJTs and SiGe HBTs working in harsh conditions.

In Fig. 4 the current gain damage factor $d = \beta(\Phi_n)/\beta(0)$ for the SiGe HBT 8WL after neutron irradiation is presented. It is seen that the improved model (4) provides better results than the classic Gregory model [14].

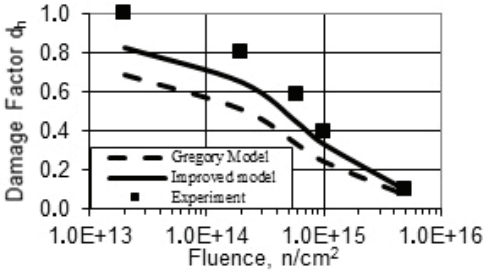


Fig. 4. The current gain damage factor for the SiGe HBT 8WL after neutron irradiation.

c. Proton radiation model. The proton irradiation involves simultaneously the ionization and displacement damages in semiconductor device structures. Conformably to TCAD modeling of BJT/HBT and MOSFET structures the radiation model for protons was first developed in our works [6, 15]. It is based on additive approach combined two models: model for gamma rays describing the ionization effects and model for neutrons describing the displacement effects. Both models were discussed above.

For the correct modeling of the Si BJT/SiGe HBT and MOSFET characteristics, it is necessary to determine the values of the neutron fluence Φ_n and the gamma dose D_γ equivalent to proton fluence Φ_p. For this purpose, the following equations were used:

$$\Phi_n = K_D \cdot \Phi_p, \; D_\gamma = K_{I_p}(E) \cdot \Phi_p, \qquad (5)$$

where $K_D = \delta_{cp}(E)/\delta_{cn}(E)$, K_D – proportion coefficient; $\delta_{cp}(E)$, $\delta_{cn}(E)$ are the energy-dependent non-ionization energy losses (NIEL) for protons and neutrons respectively [11]; $K_{i_p}(E)$ is the proton linear energy transfer (LET) in material with the same energy [16]. The special converter was developed and included in MODEL LIBRARY for realization of the procedure (5).

5. Simulation Results

The potentialities of TCAD-RAD subsystem (Fig. 1) are illustrated by means of examples of Si

BJTs/ SiGe HBTs and SOI MOSFETs which are used for rad-hard BiCMOS ICs design (see Figs. 5-10).

The discrete Si npn BJT 2T378 with following parameters: current gain $\beta = 70$, cut-off frequency $f_T = 1.9$ GHz and $f_{max} = 5.1$ GHz is used in microwave amplifier hybrid ICs. The radiation-hardness of Si BJT after neutron irradiation was analyzed with developed model. The BJT structure for TCAD simulation is presented in Fig. 5.

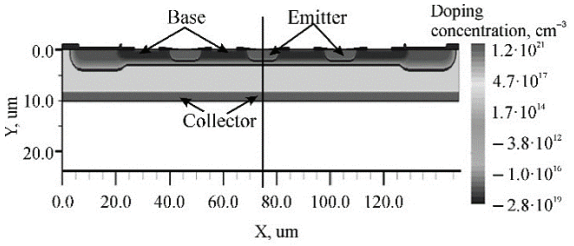


Fig. 5. TCAD interpretation of the Si BJT 2T378 structure.

In Fig. 6 experimental and simulated results for the current gain of the Si BJT before and after neutrons irradiation are shown.

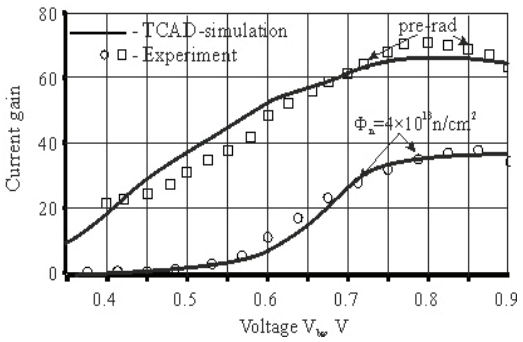


Fig. 6. Current Gain of Si BJT 2T378 with f_T/f_{max}=2.0/5.1 GHz after neutron irradiation.

It is seen in Fig. 6 that the radiation hardness is limited by fluence $\Phi_n = 4 \cdot 10^{13}$ 1/cm^2 at which the pick values of current gain decrease twice. The error of the experimental and simulated results is not more than 15 %.

The next two examples illustrate the results of the radiation hardness after gamma irradiation modeling for modern deep submicron devices with bipolar and MOS structures.

The SiGe HBT with parameters $\beta = 450$, $f_T = 100$ GHz, $f_{max} = 200$ GHz fabricated by 0.13 µm BiCMOS 8HP technology was investigated [17]. The Gummel I-V characteristics of I_b and I_c for different gamma doses are presented in Fig. 7 and confirm the experimentally observed fact that in SiGe HBTs only the base current is growing after irradiation; at the same time the collector current does not change their values. It is seen a good agreement between simulated and measured characteristics in dose range up to 30 Mrad.

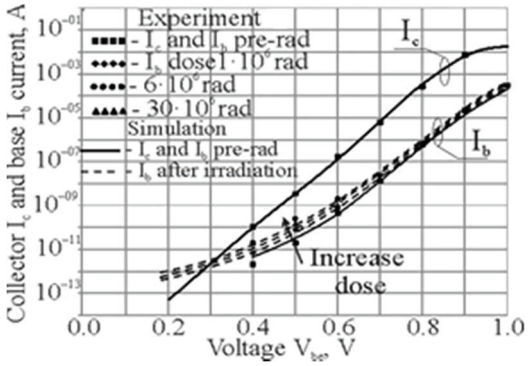


Fig. 7. Gummel characteristics of I_b, I_c for SiGe HBT 8HP after gamma irradiation.

The 45 nm high-k SOI n-MOSFET (W = 0.45 um, $t_{HfO2} = 2$ nm) before and after gamma irradiation [18] was modeled (Fig. 8). It is seen that the SOI MOSFET drain leakage current is growing after radiation influence. The total I_d leakage current is caused basically by parasitic STI channel induced by gamma irradiation. The maximum value of Id_{leak} is limited as 1.0 µA, so the transistor radiation hardness is limited by dose 1.0 Mrad.

Figs.9 and 10 illustrate the results obtained using the developed models taken into account proton irradiation effects.

The 180 nm SiGe HBT with $\beta = 250$, $f_T = 120$ GHz, $f_{max} = 100$ GHz [19] was selected for proton radiation hardness investigation with the Synopsys Sentaurus. The comparison of simulated results with experimental data for current gain is presented in Fig.9 for the irradiated and non-irradiated device. Using 50 % current gain fall down criteria the proton irradiation upper limit is defined as $5 \cdot 10^{13}$ 1/cm^2.

In Fig.10 the measured [20] and simulated I_dV_g characteristics of 0.25/8 um SOI n-MOSFET before and after proton irradiation are presented. The protons cause a stronger impact than gamma radiation so in comparison with Fig.8 for gamma irradiation we can see in Fig.10 not only leakage current increase but also threshold voltage shift. As a result the transistor radiation hardness in this case is limited by dose 500 krad.

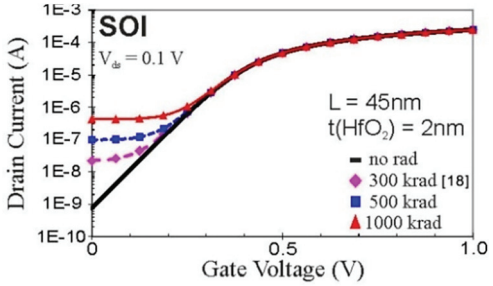


Fig. 8. I_dV_g characteristics of 45 nm SOI high-k MOSFET after gamma irradiation (W = 0.45 um, t_{HfO2}=2 nm).

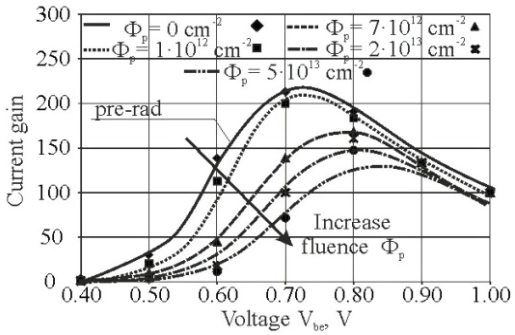


Fig. 9. Current Gain of SiGe HBT 7HP with A_E = 0.2×4.52 um^2 f_T/f_{max} = 150/180 GHz after proton irradiation.

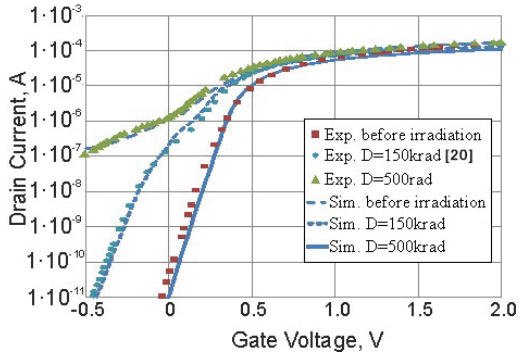


Fig. 10. SOI n-MOSFET characteristics after proton irradiation (L/W = 0.25/8 um, t_{ox} = 7.5 nm, t_{Si} = 50 nm, t_{BOX} = 190 nm).

6. Conclusions

The universal and complete library of radiation-dependent physical parameter models for Si BJT/SiGe HBT and bulk/SOI MOSFET structures simulation taking into account neutron, gamma and proton irradiation was developed in the framework of Synopsys Sentaurus TCAD.

The following novelties were introduced into commercial TCAD physical model library:

1) New segment of neutron radiation models which include: improved equations for electron and hole carrier lifetime taken into account the dependence on neutron fluence, doping concentration and injection efficiency; improved equation for carrier mobility depending on neutron fluence;
2) New segment of proton radiation model based on additive approach combined displacement and ionization damage mechanisms. Two partial models for neutrons and gamma rays are used to calculate simultaneously. The special converter was developed to determine the values of neutron fluence Φ_n and gamma dose D_γ equivalent to proton fluence Φ_p;
3) Segment of gamma radiation models was essentially improved:
   - The modified dependence on dose for carrier mobility $\mu_{eff}(D_\gamma)$ was introduced;
   - The surface recombination velocity $S(D_\gamma)$ for Si-SiO_2 interfaces was included;
   - Approximations of experimental dependencies for traps concentrations $N_{it}(D_\gamma)$, $N_{ot}(D_\gamma)$ at the Si-SiO_2/Si-HfO_2 interfaces and in bulk volumes separately for gate oxide, p-n spaces, BOX, STI/DTI structures were introduced for modeling of both conventional bipolar and MOS transistors and modern deep submicron Si BJTs/SiGe HBTs and bulk/SOI high-k MOSFETs.

Good agreement between simulated and experimental I-V and f_T/f_{max} characteristics for all the devices was achieved. The simulation error is not more then 10-20 %.

The possibilities of TCAD-RAD subsystem with the developed radiation models were illustrated by means of examples of Si BJTs/SiGe HBTs and bulk/SOI MOSFETs which were used for rad-hard BiCMOS ICs design.

References

[1]. TCAD Sentaurus User Manual J-2014.09, *Synopsys*.
[2]. Silvaco Radiation Effect Module, www.silvaco.com
[3]. Cagenda Integrated Solution for EDA/TCAD/ RadHard, http://www.cagenda.com
[4]. K. O. Petrosyants, et al., 45 nm High-k MOSFETs on bulk silicon and SOI substrates modeling to account for total dose effects, in *Proceedings of the International Workshop on Reliability of Micro- and Nano-Electronic Devices in Harsh Environment (IWRMN-EDHE'17),* 2017, pp. 1-3.
[5]. K. O. Petrosyants, et al., Si BJT and SiGe HBT performance modeling after neutron radiation exposure, in *Proceedings of the IEEE East-West Design & Test Symposium (EWDTS'11)*, 2011, pp. 267-270.
[6]. K. O. Petrosyants, et al., Physical TCAD model for proton radiation effects in SiGe HBTs, *IEEE Trans. Nucl. Sci.*, Vol. 63, Issue 4, August 2016, pp. 2016-2021.
[7]. S. Put, E. Simoen, S. Van Huylenbroeck, C. Claeys, M. Van Uffelen, P. Leroux, Effect of airgap deep trench isolation on the gamma radiation behavior of a 0.13 um SiGe:C NPN HBT technology, *IEEE Trans. Nucl. Sci*., Vol. 56, Issue 4, August 2009, pp. 2198-2204.
[8]. H. J. Barnaby, B. Vermeire, M. J. Campola, Improved model for increased surface recombination current in irradiated bipolar junction transistors, *IEEE Trans. Nucl. Sci*., Vol. 62, Issue 4, August 2015, pp. 1658-1664.
[9]. C. Claeys, E. Simoen, Radiation Effects in Advanced Semiconductor Materials and Devices, Vol. 57. *Springer Science & Business Media*, 2013.
[10]. D. Rideau, Y. M. Niquet, O. Nier, et al., Mobility in high-K metal gate UTBB-FDSOI devices: From NEGF to TCAD perspectives, in *Proceedings of the IEEE International Electron Devices Meeting (IEDM'13)*, 2013, pp. 12.5.1-12.5.4.

[11]. C. Poivey, G. Hopkinson, Displacement damage mechanism and effects, in *Proceedings of the ESA-EPFL Space Center Workshop*, Jun. 2009.

[12]. O. L. Curtis, Effects of oxygen and dopant on lifetime in neutron-irradiated silicon, *IEEE Trans. Nucl. Sci*., Vol. 13, Issue 6, Decemebr 1966, pp. 33-40.

[13]. E. N. Vologdin, D. S. Smirnov, Empirical relations for dependence of the coefficient of radiation-induced alteration of carrier life time in silicon at the neutron irradiation from injection and doping level, *Questions of Atomic Science and Technics, Series: Physics of Radiation Effects on Radio-Electronic Equipment*, Vol. 2, June 2010, pp. 17-22.

[14]. B. L. Gregory, C. W. Gwyn, Application of neutron damage models to semiconductor device studies, *IEEE Trans. Nucl. Sci.,* Vol. 17, Issue 6, December 1970, pp. 325-333.

[15]. K. O. Petrosyants, D. A. Popov, M. V. Kozhukhov, General approach to TCAD simulation of BJT/HBT and MOSFET structures after proton irradiation, in *Proceedings of the International Workshop on Reliability of Micro- and Nano-Electronic Devices in Harsh Environment (IWRMN-EDHE'17)*, 2017, pp. 1-3.

[16]. I. P. Bezrodnih, A. P. Tyutnev, V. T. Semenov, Radiation Effects in Space Environment. Part 1. Radiation in the Near-Earth Space, *JCS Corporation 'VNIIEM'*, Moscow, 2014, pp. 64-65 [in Russian].

[17]. K. C. Praveen, N. Pushpa, Y. P. Prabakara Rao, G. Govindaraj, J. D. Cressler, A. P. G. Prakash, Application of advanced 200 GHz Si–Ge HBTs for high dose radiation environments, *Solid-State Electronics*, Vol. 54, Issue 12, 2010, pp. 1554-1560.

[18]. S. T. Liu, A. Hurst, H. L. Hughes, et al, Total dose radiation response of a 45 nm SOI Technology, in *Proceedings of the IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S'10),* 2010, pp. 1-2.

[19]. J. P. Comeau, A. K. Sutton, B. M. Haugerud, J. D. Cressler, Wei-Min Lance Kuo, P. W. Marshall, R. A. Reed, A. Karroy, R. Van Art, Proton tolerance of advanced The SiGe HBTs fabricated on different substrate materials*, IEEE Trans. Nucl. Sci*., Vol. 51, Issue 6, Dec. 2004, pp. 3743-3747.

[20]. Y. Li, et. al, Anomalous Radiation Effects in Fully-Depleted SOI MOSFETs Fabricated on SIMOX, *IEEE Trans. Nuc. Sci*., Vol. 48, Issue 6, 2001, pp. 2146-2151.

(026)

Monolithic III-V/CMOS Technology, Unified Device Compact Models and Hybrid Process Design Kit

X. Zhou and S. B. Chiah
School of Electrical and Electronic Engineering, Nanyang Technological University,
Block S1, 50 Nanyang Avenue, Singapore, 639798
Tel.: +65-67904532, fax: +65-67933318
E-mail: exzhou@ntu.edu.sg

Summary: The SMART-LEES (Singapore MIT Alliance for Research and Technology – Low Energy Electronic Systems) program is directed towards finding a new innovation path in the semiconductor industry to create novel integrated circuits. It is established by incorporating III-V material layers into existing Si-CMOS platform, thus, hybrid III-V/Si circuits can be designed and fabricated on a single chip, allowing novel application circuits to be created beyond traditional approach and capabilities. This paper presents a summary of the essential elements in this program, including monolithic III-V/CMOS technology, unified device compact models, and hybrid process design kit.

Keywords: Compact model, HEMT, Hybrid circuit design, Hybrid process design kit, III-V, Monolithic technology.

1. Introduction

Conventional mainstream Si-CMOS has approached its fundamental limits after several decades of scaling, as evident from saturated trend of the Moore's law. How to sustain the growth of this industry has become a major challenge, and it also prompts motivations for innovative paths to new integrated circuits (IC). Recently, new IC technologies employing III-V materials have emerged as promising candidates for new device building blocks, such as GaN devices on 200-mm CMOS-compatible GaN-on-Si process [1] and wafer-scale integration of III-V-on-Si on 200-mm wafers [2]. They both leverage on existing mature Si-CMOS infrastructure, while the latter has distinctive differences and advantages compared with the former.

In the wafer-scale integration of III-V-on-Si led by the Singapore MIT Alliance for Research and Technology (SMART) Low Energy Electronic Systems (LEES) program [3], III-V materials and devices, such as high electron-mobility transistors (HEMTs) on GaN/InGaAs platforms and light-emitting diodes (LEDs) on GaN/InGaP platforms, are co-integrated monolithically with the conventional foundry Si-CMOS process, allowing new hybrid circuits in both III-V and Si worlds to be designed and fabricated on a single chip. As shown in Fig. 1, it represents a "vertical" innovation model that exploits different (III-V/Si) material platforms, through III-V/Si co-integration processes, building from III-V/Si devices to hybrid integrated circuits/systems on a single die, as opposed to extending the current CMOS foundry and fabless models "horizontally." Successful implementation of the new platform provides a path to new innovative applications that are not easily achievable with separate III-V and Si chips.

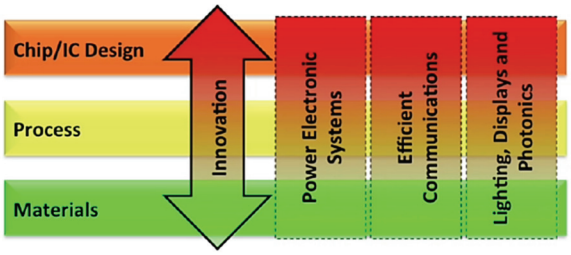


Fig. 1. The SMART-LEES vertical innovation model [3].

Fig. 2 shows a top-level view of the LEES platform [4], in which Si-CMOS front-end of a hybrid design is first fabricated in a commercial foundry; then, it is sent for the LEES "double-layer bond-and-transfer" (DL-BaT) process [5] to form an engineered substrate containing both Si and compound semiconductor (CS) material layers on which III-V devices can be formed; followed by sending it back to the foundry for back-end processing, which looked like the wafer never left the Si-fab. A hybrid process design kit (PDK) [6], including III-V device models and design rules and combining with the foundry PDK, has been developed for use in the hybrid circuit design.



Fig. 2. Top-level view of the LEES III-V/Si co-integrated platform [4].

This paper describes the three major aspects of the vertical innovation project under the SMART-LEES program [3], namely, monolithic III-V/CMOS co-integrated technology, unified III-V and Si device compact modeling (CM), and hybrid PDK for hybrid III-V/CMOS circuit design.

2. Innovative Technology, Modeling and Design

2.1. Monolithic III-V/CMOS Technology

The LEES monolithic III-V/CMOS technology is achieved through the DL-BaT process [5], from which various engineered "CMOS + *X*" substrates for HEMTs/LEDs can be obtained. Following this, hybrid wafer process flow is shown in Fig. 3, starting from the hybrid GaN + CMOS wafer from foundry in (a) up to back-end-of-line (BEOL) processing in (f).

2.2. Unified III-V/CMOS Device Compact Models

Two GaN-HEMT compact models are being developed in LEES project, MVSG (which is now a CMC standard model) and XSIM, the former being quasi-ballistic (QB) based and the latter drift-diffusion (DD) based (which is also scalable and compatible with generic Si-MOSFET models). Other CS models (InGaAs-HEMT, HBT, and LED) are also developed. A comparison of the two models' fit to the 45-nm GaN-HEMT data is shown in Fig. 4 [7].

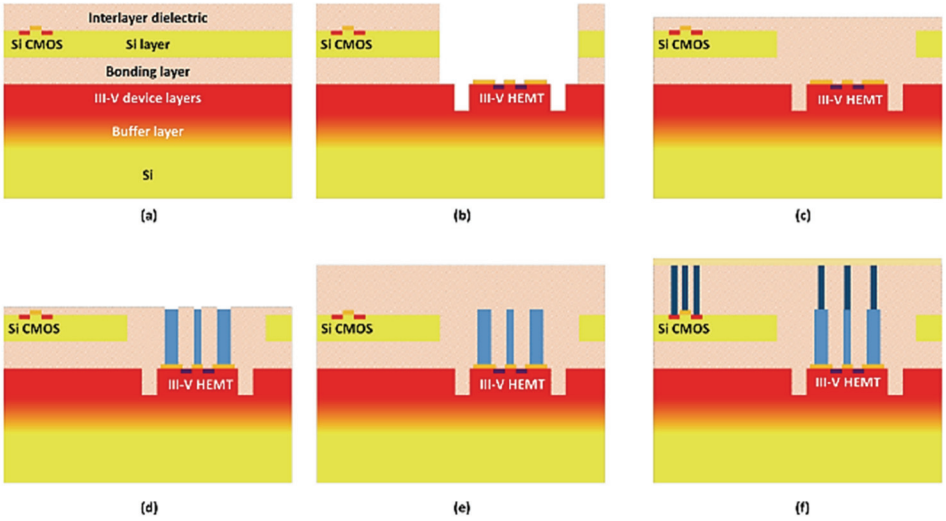


Fig. 3. LEES monolithic III-V/Si hybrid wafer processing flow [4]: (a) Starting hybrid GaN + CMOS wafer; (b) Window opening in III-V regions and device fabrication using adapted III-V device fabrication processes; (c) Re-filling of III-V windows and planarization of the wafer surface; (d) Formation of W-plugs that bring the GaN device contacts to the contact plane of the CMOS devices; (e) Redeposition of ILD and planarization; (f) BEOL processing in foundry.

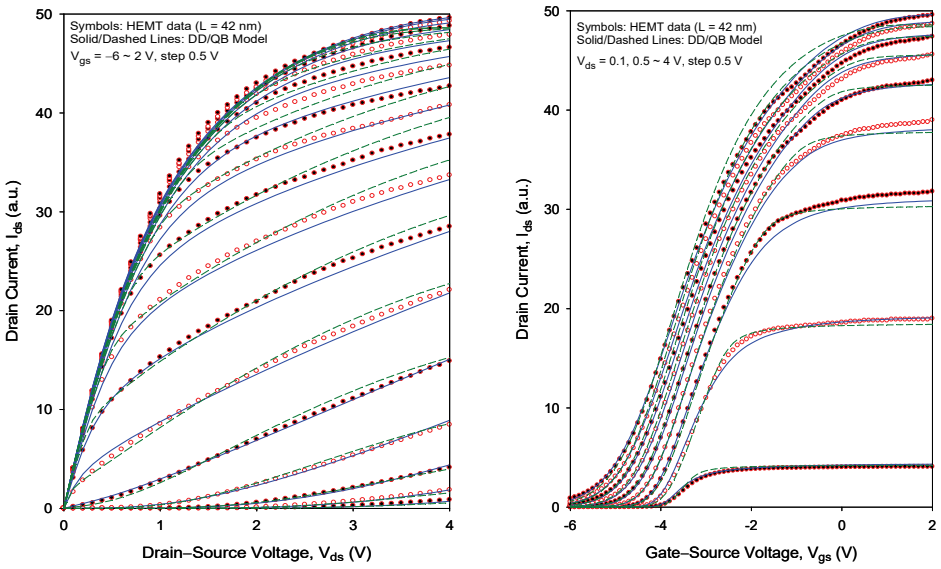


Fig. 4. Comparison of DD (solid line) and QB (dashed line) models with the measured 42-nm GaN-HEMT data (symbol) for the I_{ds}–V_{ds} (left) and I_{ds}–V_{gs} (right) characteristics [7].

2.3. Hybrid III-V/CMOS Process Design Kit

III-V device CMs and design rules are implemented in the LEES PDK, and integrated with the foundry PDK for hybrid circuit design. It allows III-V and Si device schematic and layout to be used in the same Cadence EDA toolkit. An example is shown in Fig. 5.

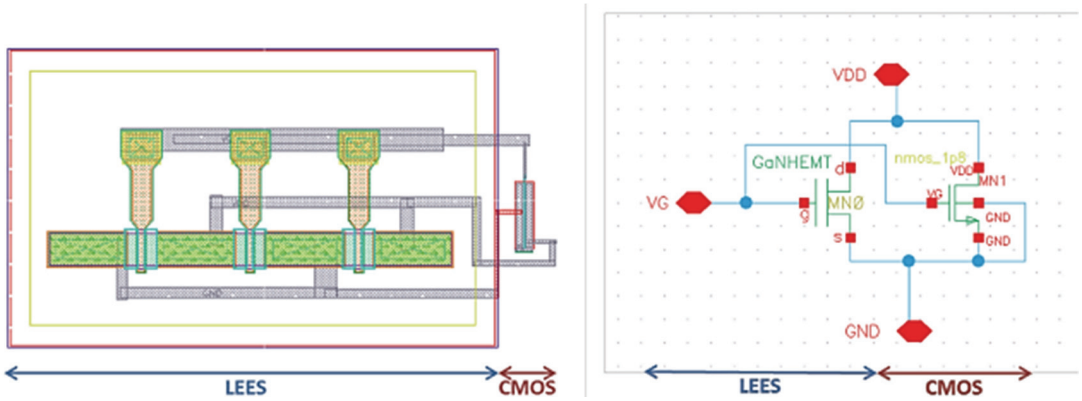


Fig. 5. LEES hybrid PDK augments foundry Si-CMOS PDK with III-V components (layout and schematic) within the same familiar design environment [8].

3. Summary

The SMART-LEES program, now at the Phase II of its second 5-year, has demonstrated a unique approach to monolithic integration of III-V/Si devices and the potential to creating novel integrated circuits beyond traditional CMOS capabilities.

Acknowledgements

This work is supported in part by the National Research Foundation, Prime Minister's Office, Singapore through the Singapore MIT Alliance for Research and Technology's Low Energy Electronic Systems SMART-LEES Subaward No. II-01.

References

[1]. EE Times, IMEC makes GaN-on-silicon, http://www.eetimes.com/document.asp?doc_id=1266423

[2]. Compound Semiconductor Magazine, Singapore MIT Alliance Focuses On Wafer-scale Integration, http://www.compoundsemiconductor.net/article/89988-singapore-mit-alliance-focuses-on-wafer-scale-integration.html

[3]. Singapore MIT Alliance for Research and Technology (SMART) Low Energy Electronic Systems (LEES), http://www.circuit-innovation.org/

[4]. E. A. Fitzgerald, K. E. Lee, S. F. Yoon, S. J. Chua, C. S. Tan, T. Palacios, X. Zhou, J. S. Chang, D. A. Kohen, L. Zhang, K. H. Lee, Z. H. Liu, S. B. Chiah, T. Ge, Enabling the integrated circuits of the future, in *Proceedings of the 11th International Conference on Electron Devices and Solid State Circuits (EDSSC'15)*, Singapore, June 2015, pp. 1-4.

[5]. K. H. Lee, S. Bao, E. A. Fitzgerald, C. S. Tan, Integration of III-V materials and Si-CMOS through double layer transfer process, *Japanese Journal of Applied Physics*, Vol. 54, 2015, 030209.

[6]. S. B. Chiah, X. Zhou, K. Lee, C. Y. Ng, D. Antoniadis, E. A. Fitzgerald, A hybrid process design kit: Towards integrating CMOS and III-V devices, in *Proceedings of the NSTI Nanotech (WCM-Nanotech'16)*, Washington, DC, May 2016, Vol. 4, pp. 313-317.

[7]. X. Zhou, J. B. Zhang, B. Syamal, Z. M. Zhu, H. T. Zhou, S. B. Chiah, Top-down drift-diffusion versus bottom-up quasi-ballistic formalism in device compact modeling, in *Proceedings of the 20th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES'13)*, Gdynia, Poland, June 2013, p. 53.

[8]. Compound Semiconductor Magazine, Building The ICs of The Future, https://compoundsemiconductor.net/article/98881-building-the-ics-of-the-future.html

(028)

A Project-based Integrated Circuit Design and Characterization Course: A Case Study

A. Abusleme [1] and M. Pérez-Sanagustín [2]
[1] Dept. of Electrical Engineering, Pontificia Universidad Católica de Chile,
Vicuña Mackenna 4860, Santiago, Chile
[2] Dept. of Computer Science, Pontificia Universidad Católica de Chile, Vicuña Mackenna 4860, Santiago, Chile
Tel.: + 562 2354 4809, fax: + 562 2354 4809
E-mail: angel@uc.cl

Summary: This paper presents a case study of the recently-implemented microelectronics curriculum in a university in South America, with an emphasis on the capstone, project-based course on chip design and characterization. During the course that spans two semesters, the students go through a complete chip design flow, including layout, verification, tape out and testing. Examples of students design projects include operational amplifiers, data converters, simple sequential digital circuits, and test structures. The course reception, assessed via student surveys, was positive. The novelty of the course lies in the concurrence of a number of factors that include the exposure to a complete mixed-signal IC design and characterization flow, the fabrication through MOSIS educational program, the use of free software tools, and the course impartation in a developing country that does not possess a prior history in IC design.

Keywords: Microelectronics education, Learn-by-doing, IC layout, Class project, IC design flow with free tools, MOSIS educational program.

1. Introduction

The Mead & Conway Revolution c.~1979 led to the introduction of a formal integrated circuit (IC) design curriculum in a number of Electrical Engineering and Computer Science programs around the world, allowing a new generation of students to prepare properly for the already rising microelectronics industry [3]. The revolution, enabled by the availability of IC foundries accessible for chip designers, contributed significantly to the great success of microprocessor design companies in the early 80's.

Some examples of the courses and curricular changes driven by the revolution, for both undergraduate and graduate programs, are reported in the literature [21, 6, 4, 2, 5, 20, 18, 10, 12, 13, 16, 15, 1, 22]. In general, these examples include detailed description of courses and course sequences in semiconductor physics, IC design and fabrication. The design courses cover analog, digital, mixed-signal, and RF electronics, and include theoretical lectures, homework (HW) assignments, hands-on CAD design projects, design submission for fabrication, and laboratory measurements. Some works report the use of free EDA (electronic design automation) tools, whereas others promote the use of commercial tools. Of those that report IC fabrication, some use the MOSIS [17] service whereas others have established a partnership with one or more IC foundries. Table 1 presents a comparison between the courses and programs reported.

In a typical microelectronics curriculum, IC design and manufacturing are rather decoupled, which allows chip designers to detach from the issues faced in the fabrication facility - kilometers or continents away. This has facilitated the Mead & Conway Revolution to reach developing countries as well, as seen in Table 1. However, an evident pattern arises from the table: the works reporting curricular changes in developing countries are rather recent, and there are still many places where microelectronics is "something done somewhere else". The reason for this can be linked to the old and questionable paradigm that bootstraps design and fabrication in a single, expensive discipline with large barriers to entry. However, the technology-enabling capability of the nowadays systems-on-a-chip, applicable to any local industry or scientific research need, is a strong argument for the inclusion of microelectronics design in curricula all over the world, without a compelling need to include fabrication.

In Chile, the Mead & Conway revolution arrived in 2011 with the offering of the first courses in microelectronics at Pontificia Universidad Católica de Chile (UC): IEE3433 Analog IC Design, and IEE3753 Digital IC Design. Both courses include a final project, the former at circuit-design level using Linear Technology L Tspice [14] for simulations, whereas the latter at HDL (hardware description language) level using Xilinx ISE Webpack [25] and Synopsys tools. These courses that reinforced other electronics courses available at that time, were followed by IEE3443 VLSI Data Converter Design and IEE3423 IC Design and Characterization. A strong program in microelectronics became available within a 3-year period, opening new research and teaching possibilities.

This paper presents the details of the capstone course IEE3423 IC Design and Characterization offered at UC, along with the microelectronics curriculum that leads to it. The project-based course allows students to take a design from a previous course

– analog, digital or mixed-signal – to silicon, fabricated through the MOSIS Educational Program (MEP).

The objective of this work is to assess the course as a generic formative tool within an Electrical Engineering program, and its role in producing IC designers. With this paper, we also expect to demonstrate how such a course can be implemented in developing countries on a constrained budget, in order to facilitate its adoption.

Table 1. Comparison between courses and IC design programs reported elsewhere.

Work	Location	Level	IC domain	Circuit	Layout	Fabrication	Testing	EDA Tools
[21] (1988)	England	Senior/Grad.	Digital	✓	✓	×	×	Commercial
[6] (1993)	USA	Undergrad.	Mixed Signal	✓	✓	Not required	✓	Not specified
[4] (1996)	USA	Senior	Analog/Digital	✓	✓	Encouraged	✓	Free/Comm.
[2](1997)	USA	Graduate	Analog/Digital	✓	✓	×	×	Free/Comm.
[5] (1997)	USA	Senior	Analog	✓	✓	×	✓	Not specified
[20] (2001)	USA	Undergrad.	Digital	×	×	Custom	✓	Commercial
[18] (2004)	Singapore	Senior	RF	✓	✓	Ext. foundries	✓	Commercial
[10] (2006)	USA	Senior	Mixed Signal	✓	✓	MOSIS	×	Commercial
[12] (2010)	USA	Junior/Senior	Digital	✓	✓	×	×	Free
[13] (2010)	Taiwan	Graduate	Analog	✓	✓	TSMC	✓	Commercial
[16] (2011)	USA	Senior/Grad.	Digital	✓	✓	×	×	Commercial
[15] (2011)	Argentina	Undergrad./Grad.	Analog/Digital	✓	✓	MOSIS	✓	Commercial
[1] (2012)	Pakistan	Undergrad.	Digital	✓	✓	×	×	Commercial
[22] (2013)	Bulgary	Undergrad.	Analog/Digital	✓	✓	×	×	Free
This work	Chile	Senior/Grad.	Mixed Signal	✓	✓	MOSIS	✓	Free/Comm.

2. Course Context, Description and Methodology

Chile is a democratic country in the southwestern part of America. Most population and services are concentrated in Santiago, the capital city. Chile has a stable political system and a strong, growing economy; however, it only invests 0.4 % of its Gross Domestic Product (GDP) in research. The main contribution to the Chilean GDP and exports is copper mining. The electronics industry is not well developed. Only a few companies design products using discrete components, and no companies design ICs.

At the time the course in this work was introduced, the Electrical Engineering Program at the School of Engineering-UC was an 11-semester [1] undergrad program leading to the Electrical Engineer (EE) degree, or to the Industrial Engineer degree with diploma in EE. The EE program begins with set of mathematics and basic sciences courses, the same for all engineering programs offered by the school. After two and a half years, students should pick their field and take a set of mandatory and optional courses towards the EE degree (~35 students per year), or the Industrial Engineer degree with a diploma in EE (~35 students per year). The latter option has some courses on finance and management in addition to the core in EE.

2.1. Microelectronics Curriculum

The students who follow the curriculum in microelectronics acquire competencies that allow them to design ICs in Chile for research purposes, or abroad for industry purposes, and to pursue an eventual academic career in the area. Fig. 1 shows the course sequence[2].

The program in microelectronics, taught in Spanish, begins with IEE2413 Electronics, a one-semester undergraduate course taught every semester, that follows a circuit analysis course. IEE2413 is mandatory for all students in the major and covers basic circuit analysis, simulation and design using operational amplifiers, transistors and diodes. After completing the course, the students can analyze, simulate and design moderately complex electronic circuits. The course has two lectures, a problem session and a questions-and-answers session per week. Lectures are recorded using an effective, low-budget recording system and uploaded to a video hosting service as a reward when the student attendance is higher than 90 %. Videos from previous semesters allow implementing flipped classroom techniques.

[1] Currently, a curricular change is being implemented. The new curriculum includes an eight-semester Bachelor's degree, with a major in Electrical Engineering and a minor in another field, followed by a two-semester professional degree or a MSc program.

[2] IEE2483 and IEE2783 have recently been fused into a single laboratory course; other smaller changes have also taken place. However, for the purpose of presenting the results between 2012 and 2016, the course sequence shown here was active in this time period.

Grading is based mostly on individual work, which includes weekly HW assignments, four exams and an oral final exam intended only for the students whose grade is close to the passing threshold. The exams are closed-book, but students are allowed to use a handwritten equation sheet that they must turn in a week before the evaluation, thus ensuring that they have studied the material in advance. L Tspice is used for circuit simulation throughout the course. The coursework includes a final, open-ended design project, carried out in groups of two or three students, and simulated using L Tspice. The course withdrawal rate is around 10 %, whereas the failure rate is around 25 %. The workload is 10 hours per week.

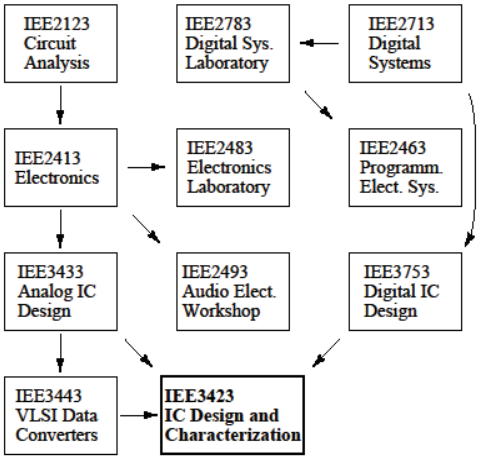


Fig. 1. Course sequence that leads to the course presented.

IEE2413 is followed by IEE2483 Electronics Laboratory. In this course students team up in groups of two and follow partially-guided experiments that include device characterization and simple amplifier design and testing. The workload is 5 hours per week.

IEE2493 Audio Electronics Workshop is an optional project-based course in which students build an audio amplifier using discrete components. Grading takes into account the electrical and mechanical implementation.

The curriculum in microelectronics continues with IEE3433 Analog IC Design, a graduate-level course taken by an average of 15 students every year. The contents include advanced MOSFET models, g_m/I_D design techniques, amplifier topologies, current mirrors, differential pair, noise analysis, bandwidth estimation techniques, stability, bandgap references, and trends in technology. The course has two lectures and a problem session per week, and requires a workload of 10 hours per week. Lectures are recorded and uploaded for future reference. Student work includes assignments to be solved individually, written midterm and final exams and a design project. For the project, students grouped in teams of two must design an operational amplifier or an operational transconductance amplifier following a set of specifications. Their designs are targeted on a commercial 0.5-micrometer CMOS process available for fabrication through MOSIS. Designs are simulated using L Tspice. In the first iteration, the students turn in a working design which is reviewed by the instruction team. The feedback provided is used by the students to improve their designs, presented orally a week later.

IEE3433 is followed by IEE3443 VLSI Data Converters, a graduate-level course taken by an average of 5 students every year. The course contents include sampling and quantization, digital-to-analog converters, analog-to-digital converter (ADC) families, track-and-hold circuits, flash ADCs, successive approximation register ADCs, pipeline ADCs, oversampling converters and technology trends. The workload is 10 hours per week and the grading process is similar to that of IEE3433, with two differences: the final exam is replaced by a presentation, and the design project topic is chosen by the students. The presentation requires students to read and understand one ADC paper from a recent conference, to reproduce some theoretical analysis and simulation results, and to challenge the conclusions. The oral presentation is subject to peer assessment [11] through students questions. Design projects, intended for one or two students, are designed for the same CMOS process used in IEE3433, simulated using either MATLAB (behavioral simulation) or L Tspice, and presented orally in another session. Projects are designed using a top-down approach.

Complementary to these courses, a digital track runs in parallel. It begins with IEE2713 Digital Systems, focusing on the fundamentals of Boolean algebra, logic gates, combinational and sequential logic circuits, and the basics of FPGAs. The course assessment includes a final FPGA design. The workload is 10 hours per week.

Then in IEE2783 Digital Systems Lab, students spend 5 hours per week to put their digital design knowledge in practice. The course has evolved from designs based on discrete logic gates to FPGA. The final project involves the implementation of a simple game on an FPGA that displays images in a VGA monitor and a gets the user input from a joystick.

IEE2463 Programmable Electronic Systems focuses on the fundamentals of microcomputer architectures and programming, and includes 16 hands-on experiences.

IEE3753 Digital IC Design, a 10-hour-per-week grad-level course, deepens on digital design using Verilog. The assignments include a complex project implemented on an FPGA. Examples of past projects include oscilloscopes, microprocessors and electronic games. The students also generate a GDS file for a generic fabrication process.

All the courses presented in this subsection include project-based learning concepts [24] and some employ a flipped-classroom teaching methodology [8]. The capstone for the curriculum introduced is detailed next.

2.2. IEE3423 IC Design and Characterization

The capstone in the microelectronics curriculum is IEE3423 IC Design and Characterization. Although

not considered an official capstone within the EE curriculum, due to the high level of specificity and the small number of students that take it, it is a *de-facto* capstone for the students interested in IC design[3].

This course serves as a culmination for the learning process that allows students to put together the knowledge and skills included in all the preceding courses, and prepares them to face the engineering practices found in industry through the execution of a major project. The competencies involved in the course include system-level electronics design, circuit-level design using realistic device models and constraints, circuit-level simulation, layout techniques, verification procedures, testing, teamwork and communication skills. The material for the course includes [17, 19, 9].

In this course, students are given complete freedom to design and implement any circuit (analog, mixed-signal or digital) on a chip. The course has three lectures at the beginning of the semester, which include IC fabrication processes, layout techniques, design rules (including lambda rules), mismatch issues, and the software used in the course, which includes Magic layout editor and Netgen layout-vs-schematic (LVS) tool [19]. On-demand tutorials are also provided.

The grading scheme begins with a HW assignment where students work individually on the analog design flow, designing a simple amplifier that uses NMOS and PMOS transistors, poly-poly capacitors and resistors. The assignment is guided on a step-by-step recipe and includes floorplanning, layout, design rule check (DRC), LVS against netlist, post-layout simulation and generation of a GDS file. Although the pad frame is not required at this point, students are encouraged to take into account the location of inputs, outputs and power supply nodes. After the assignment, the students work on their projects throughout the semester. This work begins with the definition of their project, discussed with the lecturer, and which may use circuit blocks from a previous semester. Following this, students design their circuit, work on the IC layout including pad frame, verify the design and iterate as needed before generating the GDS file, respecting the fabrication deadlines.

Although the course requires a dedication of 10 hours per week during one semester, in practice students devote ~7 hours per week during one semester in order to have their layout finished, and the next semester they complete the course workload in testing the chip, which includes the design of a custom PCB. Since an official grade is required after the first semester, students get an *incomplete* grade that is replaced after the IC is tested. Finally, the students write a report for MOSIS to fulfill the MEP requirement. Grading is based on the layout and the IC performance.

2.3. Administrative Issues

One of the difficulties in the implementation of this course arises from the time span, requiring at least two semesters for layout, fabrication and testing. Since all courses at UC must be graded at the end of the semester, the *incomplete* grade has become customary in IEE3423. This result may affect students who require a grade at the end of the semester to fulfill an academic milestone or to apply for a scholarship or get a GPA award. A less frequent problem arises when the student has already completed the requirements to obtain the degree, and enroll in the course without a need for the credit. The student may withdraw the course after tape out, leaving a chip untested and a pending MEP report.

Another option to overcome the administrative time span issue is to let students audit the course during the first semester and take it for credit during the second semester. In this case, the level of engagement of the student towards the course may become compromised when auditing, leading to a high withdrawal rate.

3. Class Project Examples

Since all the courses that lead to IEE3423 include a final project, there are previous designs that students can reuse to implement on a chip. The most typical circuit block implemented in IEE3423 is an operational amplifier capable of driving an oscilloscope probe and a resistive load, thus it can be configured and tested in a feedback loop. Fig. 2 shows an example of an IEE3423 IC layout. It includes a pad frame that uses cells from the FreePDK library from Oklahoma State University [7] and two circuits in the core: an operational amplifier (top left) and an offset-cancelling comparator. This 1.5 mm × 1.5 mm chip was designed between March and July 2012, taped out in July, and tested in November.

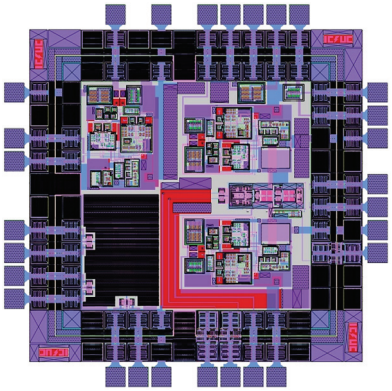


Fig. 2. Layout of an analog IC designed by students of IEE3423 using Magic layout tools.

Since students are given freedom to choose their project, a wide variety of designs have resulted from the 20 students[4] who have taken this course. They include operational amplifiers with rail-to-rail

[3] Our experience with the course will eventually help us to include IC design competencies in our official capstone course.

[4] Three students in 2012, four in 2013, seven in 2014, four in 2015 and one in 2016.

operation, a sigma-delta ADC (chip microphotograph shown in Fig. 3), bandgap references that use a parasitic PNP transistor, a flash ADC, a digital counter, a digital filter, and test structures such as a comparator array, a ring oscillator, and spiral inductors.

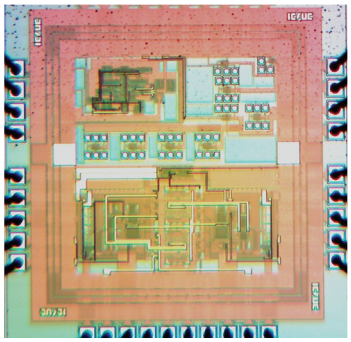


Fig. 3. Microphotograph of an IC designed by students of IEE3423. The top half includes an operational amplifier and several test transistors. The bottom half is a sigma-delta ADC.

During IEE3423, students learn not only about a typical IC design flow but also how to deal with deadlines. This skill is crucial in IC layout, since it is usually enjoyable to improve a layout, but the time invested in refinements can be better used in a more robust verification through post-layout simulations.

4. Course and Program Reception

This section aims to present the perception left by the course on students and lecturer. Qualitatively, the students attitudes have been hugely positive throughout the course, starting from the first lecture, going through the familiarization with the software and design flow, experiencing the submission for fabrication of an IC layout and finishing with the chip testing. Most students show great interest in having a successful project; with this motivation, the students of IEE3423 have achieved a number goals not intended in the course conception, such as developing scripts to automate some of the EDA tools tasks, and learning circuit topologies to improve the specifications. Since the projects and the students background are all different, each design is a particular case, requiring a custom set of abilities and knowledge. In its current state, this course is limited to ~10 students per year, since it is difficult for a lecturer to follow and advise on a greater number of projects.

From a lecturer standpoint, the course is an absolute success. The students who enroll every year experience the engineering profession exercise in a meaningful project and become aware of the difficulties to surpass in real life. After the course, the students are capable of appreciating the work behind any engineering project. Additionally, they develop their engineering criteria that allow them to estimate the difficulty of a design task before executing it. Within these criteria, the students also develop a clear sense of the variables in electronics, such as signal/noise levels, currents, frequency, area, and a notion of the design envelope in a CMOS process.

This course not only meets the purpose of allowing students to act as IC design engineers during a year, but also serves as a catalyst for the student maturation, since everything they have learned in previous courses now seems to have a purpose. After succeeding in IEE3423, the students show overall stronger engineering abilities that become evident in research discussions. Students that take IEE3423 usually perform better as teaching assistants of other electronics courses; however, it is not clear if this is a consequence of the course, or related with the student inherent motivation for electronics.

From a researcher perspective, the performance of a student through the course is well related to his/her performance as a research assistant. Usually, students who show a great interest in the course and who persevere in order to achieve an outstanding design, also are more capable in their research tasks. In this sense, from a principal investigator perspective, the course may also serve as a filter to discriminate over the student aptitudes and attitudes towards difficult tasks.

Although the microelectronics program reception among faculty members has been positive, there are some questionings since in Chile there is no IC industry, so the competencies learned in these courses may not be useful in the local engineering practice. Additionally, the EDA tools cost and maintenance is a strong barrier for startups to develop ICs in Chile, thus some faculty members believe that there is no point in forcing the development of a local IC industry. However, this argument is shortsighted, considering the possibility of preparing the ground and support for the eventual landing of a global IC design company in Chile.

5. Course Evaluation

The purpose of this research is to assess the course as a generic formative tool within an EE program, and to conclude on the value of the course in producing IC designers.

5.1. Participants and Methodology

The participants of this research are all 12 students that have completed IEE3423 between 2012 and 2015 [5]. They were invited to fill a voluntary,

[5] We also wish to evaluate the course from an employer standpoint; however, the lack of a microelectronics industry in Chile made this task impossible to complete.

anonymous online survey. Not all students completed all questions.

5.2. Data Collection and Analysis

The survey, consisting of 10 questions that include multiple choice, rating scale, and open-ended questions, was administered through Survey Monkey [23]. The survey was split into five parts aiming to assess the participants background, their motivation for taking the course, their appreciation for the course content, their learning achievements, their satisfaction level, and their opinion on what is good and what can be improved.

5.3. Results

Almost 85 % of the subjects were undergrad students at the moment of taking the course; among those, 70 % already had the intention to pursue a grad degree. This figure contrasts the Departmental average of undergrad students that pursue a grad degree (30 %) and shows an intrinsic motivation within the course students. More than 90 % of the enrollees had an interest in IC design. Regarding future job preferences, 18 % show an interest in academia, whereas 64 % tilt toward the IC industry. This is peculiar in a country without such an industry.

All students declared that effectively learned IC design flow and layout design during the course, whereas 89 % declared that learned hierarchical top-down design, IC verification, and testing skills. All students consider that the course contributed in the development of their EE and IC design skills. Only 67 % consider that the course served as an exposure to the EE profession. This figure is puzzling and can be explained by the feeling among students that microelectronics is still something done professionally somewhere else.

Finally, students were asked to comment on the positive aspects of the course, and on those that can be improved. Among the former, students value the chance to design chips as part of their academic program, and to learn a topic not taught anywhere else in Chile at the time of enrollment. After completing the course, the students acknowledge an improvement in their design skills, from specifications to implementation and characterization. They also mentioned the use of free tools with basic features, which requires them to understand the mask design details, hidden from users in more advanced EDA tools. The students also value the profound development of general EE skills and criteria through a capstone design course. Finally, they also appreciate the HW assignment, which was useful for the development of their projects.

Among the aspects that can be improved, the students feel that the documentation and references are insufficient; that formal project management procedures must be taught and enforced through regular milestones checks; that the course could include more lectures with a wider range of contents, such as semiconductor physics, testing procedures and digital design flow; that the course should be offered as a two-semester course; that the students should have access to previous designs in order to reuse cells that have already been characterized; and that the course should be restricted to graduate students only, due to the required engagement.

6. Conclusions

An IC design and characterization capstone course in a South American university has been presented, along with the microelectronics program that leads to it. Without a tradition in microelectronics, this initiative represents the first sustainable effort in Chile that allows regular EE students to learn all phases of IC design, from behavioral to physical design, verification, submission for fabrication and testing. The resulting chips designed between 2012 and 2016, fabricated through the MEP, include operational amplifiers, data converters, digital circuits and test structures. A positive reception from students and faculty members has been appreciated. The capstone requires a 2-semester time span. This can be solved via administrative flexibility.

Without a local IC industry, it is not easy to justify within the academic community the existence and the efforts put into such an IC design program. However, without microelectronics-capable engineers in the industry, this is a chicken-and-egg problem. In future years, the capstone should include material on entrepreneurship to encourage students to launch a startup and catalyze the birth of a local IC industry.

Acknowledgements

We thank the students who have enrolled in the course. Their effort has made possible the results shown here; the MOSIS service for funding students projects through the MEP; Oklahoma State University for the FreePDK; Linear Technology for the development and distribution of L Tspice; Xilinx for the development and distribution of Xilinx ISE Webpack; Synopsys for the software provided through an academic agreement; FONDECYT 1170345 grant; and Tim Edwards for supporting the Open Circuit Design software package.

References

[1]. M. Bhatti, A. Minhas, M. Najam-ul Islam, M. Bhatti, Z. Ul Haque, S. Khan, Curriculum design using mentor graphics higher education program (HEP) for ASIC Designing from synthesizable HDL to GDSII, in *Proceedings of the IEEE International Conference on Teaching, Assessment and Learning for Engineering (TALE'12)*, 2012, pp. W1D-1-W1D-6.

[2]. B. Carlson, A VLSI circuit design course for practitioners and researchers, in *Proceedings of the IEEE International Conference on Microelectronic Systems Education (MSE'97)*, 1997, pp. 9-10.

[3]. M. Casale-Rossi, The heritage of Mead & Conway: What has remained the same, what has changed, what was missed, and what lies ahead, *Proceedings of the IEEE*, Vol. 102, Issue 2, 2014, pp. 114-119.
[4]. R. Caverly, Technology-based analog and digital microsystem design, in *Proceedings of the 26th Annual Conference Frontiers in Education Conference (FIE'96),* Vol. 1, 1996, pp. 330-333.
[5]. R. Caverly, A project oriented undergraduate CMOS analog microelectronic system design course, in *Proceedings of the IEEE International Conference on Microelectronic Systems Education (MSE'97),* 1997, pp. 87-88.
[6]. D. Comer, Putting mixed signal VLSI technology into the curriculum, in *Proceedings of the Twenty-Third Annual Conference Engineering Education: Renewing America's Technology*, 1993, pp. 426-428).
[7]. FreePDK, https://goo.gl/gVZnXe
[8]. D. Gonzalez-Gomez, J. S. Jeong, D. Airado Rodríguez, F. Cañada-Cañada, Performance and perception in the flipped learning model: An initial approach to evaluate the effectiveness of a new teaching methodology in a general science classroom, *Journal of Science Education and Technology*, Vol. 25, Issue 3, 2016, pp. 450-459.
[9]. L. E. Han, V. B. Perez, M. L. Cayanes, M. G. Salaber, CMOS Transistor Layout KungFu, http://www.eda-utilities.com/CMOS_Transistor_Layout_KungFu.pdf
[10]. T. Hudson, E. R. Doering, G. Lee-Thomas, Teaching mixed-signal integrated circuit design to undergraduates, *IEEE Transactions on Education*, Vol. 49, Issue 1, 2006, pp. 39-48.
[11]. A. Jaime, J. M. Blanco, C. Domínguez, A. Sanchez, J. Heras, I. Usandizaga, Spiral and project-based learning with peer assessment in a computer science project management course, *Journal of Science Education and Technology*, Vol. 25, Issue 3, 2016, pp. 439-449.
[12]. E. Kougianos, S. Mohanty, P. Patra, Digital nano-CMOS VLSI design courses in electrical and computer engineering through open-source/free tools, in *Proceedings of the International Symposium on Electronic System Design (ISED'10)*, 2010, pp. 265-270.
[13]. W. L. Lin, W. C. Cheng, C. H. Wu, H. M. Wu, C. Y. Wu, K. H. Ho, C. A. Chan, A novel analog integrated circuit design course covering design, *IEEE Transactions on Layout, and Resulting Chip Measurement*, Vol. 53, Issue 2, 2010, pp. 282-287.
[14]. Linear Technology: L Tspice IV Getting Started Guide, https://learn.sparkfun.com/tutorials/getting-started-with-ltspice
[15]. J. Lipovetzky, A. De La Plaza, M. Inza, A. M. Lutenberg, P. Carra, F. Barbeito, N. Dangiolo, L. Rigoni Lopez, Work in progress – Development of an integrated circuits course that includes the full experience of designing an ASIC in a CMOS process, in *Proceedings of the Frontiers in Education Conference (FIE'11)*, 2011, pp. T3H-1-T3H-3.
[16]. J. Lu, B. Taskin, From RTL to GDSII: An ASIC design course development using Synopsys R University Program, in *Proceedings of the IEEE International Conference on Microelectronic Systems Education (MSE'11)*, 2011, pp. 72-75.
[17]. MOSIS, http://www.mosis.org
[18]. B. L. Ooi, M. S. Leong, A novel course on microwave monolithic integrated circuit design, theory, and characterization, *IEEE Transactions on Education*, Vol. 47, Issue 1, 2004, pp. 134-140.
[19]. Open Circuit Design, http://opencircuitdesign.com/
[20]. D. Parent, Y. Dessouky, S. Gleixner, G. Young, E. Allen, Microelectronics process engineering program at SJSU, in *Proceedings of the Fourteenth Biennial University (Government) Industry Microelectronics Symposium*, 2001, pp. 128-134.
[21]. A. Rucinski, A course in VLSI semicustom design in a small school environment, *IEEE Transactions on Education*, Vol. 31, Issue 2, 1988, pp. 93-100.
[22]. K. Shtereva, I. Genchev, Teaching integrated circuits design using LASI, in *Proceedings of the 8th International Symposium on Advanced Topics in Electrical Engineering (ATEE'13)*, 2013, pp. 1-4.
[23]. Survey Monkey, http://www.surveymonkey.com
[24]. R. E. Toolin, Striking a balance between innovation and standards: A study of teachers implementing project-based approaches to teaching science, *Journal of Science Education and Technology*, Vol. 13, Issue 2, 2004, pp. 179-187.
[25]. Xilinx: ISE 10.1, Quick Start Tutorial, http://www.eng.auburn.edu/~strouce/class/elec4200/qst.pdf

(029)

Colossal Permittivity and Dielectric Relaxation in (Li, Al) Co-doped ZnO Ceramics

Dong Huang and Francis C. C. Ling
The University of Hong Kong, Department of Physics, Pokfulam Road, Hong Kong, China
Tel.: + 852 2559 9152, fax: + 852 2241 5248
E-mail: ccling@hku.hk

Summary: Due to the applications of energy storage and electronic device miniaturization, research on novel dielectric materials with colossal permittivity (CP) larger than 1000 and low dielectric loss has been receiving extensive attention. In many conventional CP materials like $CaCu_3Ti_4O_{12}$ [1], (Li, Ti) co-doped NiO [2] and copper oxide [3], the CP is usually associated with two mechanisms, namely the effects of internal barrier capacitance (IBLC) [4] and ferroelectricity. Liu et al [5] recently reported a new class of CP materials with the origin of the CP related to the electron-pinned defect formed via the co-doping of acceptor and donor [5]. For (In, Nb) co-doped TiO_2 ceramics, CP of ~6×10^4, low dielectric loss, good temperature- and frequency-stability were reported. Through donor and acceptor hetero-ionic co-substitutions in oxides, electrons in the donor hopping contributes for the CP and the acceptor holds the electrons thus suppressing the dielectric loss. ZnO is a wide band gap material recently attracted focused attention because of its potential in applications of optoelectronic, photovoltaic, transparent conducting electrode, spintronic and sensors, etc. [6]. This abstract reports the study of ZnO co-doped with Li acceptor and Al donor ($Zn_{0.99}(Li_{0.1}, Al_{0.2})_{0.033}O$). X-ray diffraction and scanning electron microscope (with EDS) studies reveal no secondary phase and the dopants are evenly distributed in the ceramic sample. Fig. 1 shows its dielectric constant and dielectric loss as a function of the frequency at room temperature, revealing the CP phenomenon with low dielectric loss ($\varepsilon_r \approx 9862$, $\tan\delta \approx 0.159$ at frequency of 1 kHz) at room-temperature.

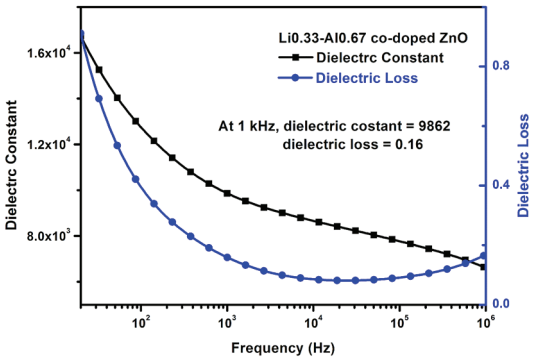


Fig. 1. Dielectric constant and dielectric loss against frequency for the $Zn_{0.99}(Li_{0.1}, Al_{0.2})_{0.033}O$ sample.

With the aim to understand the origin of the CP, dielectric spectroscopic study was conducted at 403 K. Two relaxation peaks (1 and 2) namely at the frequencies of 10^2 Hz and 10^5 Hz were identified. Annealing at 900 °C in oxygen decreases the permittivity to 2250, and at the same time removes the relaxation peak 1 in the dielectric analysis. According to the relaxation peak frequency and the annealing result, the relaxation of peak 1 is associated to interface polarization and to the oxygen-poor site at the grain boundary. Peak 2 persists after the annealing process. Arrhenius analysis shows that peak 2 has the activation energy of 0.7939 eV and the frequency factor of f_0 = 6.47×10^{14} Hz, which is associated with the relaxation of the electron pinned defect dipole.

Keywords: Colossal permittivity, ZnO ceramics, Interfacial polarization, Oxygen-poor defect, Grain boundary, Defect-dipole.

References

[1]. M. A. Subramanian, et al., High dielectric constant in $ACu_3Ti_4O_{12}$ and $ACu_3Ti_3FeO_{12}$ phases, *Journal of Solid State Chemistry*, Vol. 151, Issue 2, 2000, pp. 323-325.
[2]. J. Wu, et al., Giant dielectric permittivity observed in Li and Ti Doped NiO, *Physical Review Letters*, Vol. 89, Issue 21, 2002, 217601.
[3]. S. Sarkar, P. K. Jana, B. K. Chaudhuri, Colossal internal barrier layer capacitance effect in polycrystalline copper (II) oxide, *Applied Physics Letters*, Vol. 92, Issue 2, 2008, 022905.
[4]. M. T. Buscaglia, et al., High dielectric constant and frozen macroscopic polarization in dense nanocrystalline $BaTiO_3$ ceramics, *Physical Review B*, Vol. 73, Issue 6, 2006, 064114.
[5]. W. B. Hu, et al., Electron-pinned defect-dipoles for high-performance colossal permittivity materials, *Nature Materials*, Vol. 12, Issue 9, 2013, pp. 821-826.
[6]. Ü. Özgür et al., A comprehensive review of ZnO materials and devices, *J. Appl. Phys*., 2005, Vol. 98, Issue 4, 041301.

(030)

Effect of Resistive Switching Cycling on the Physical Characteristics of Ni/HfO_2/n^+-Si RRAM Devices

J. Muñoz-Gorriz [1], E. Miranda [1], J. Suñé [1], M. C. Acero [2], M. B. Gonzalez [2], and F. Campabadal [2]

[1] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain
[2] Institut de Microelectrònica de Barcelona, IMB-CNM, CSIC. Campus UAB, 08193 Bellaterra, Spain
Tel.: + 34935813530, fax: + 34935812600
E-mail: Jordi.Munoz.Gorriz@uab.cat

Summary: In this work, the unipolar resistive switching characteristics of Ni/HfO_2/n^+-Si RRAM devices are investigated. Inspection by scanning electron microscope after Ni removal revealed small hillocks and defects in the active area caused by the electrical stress during cycling. In addition, for severely damaged devices the set voltage is found to exceed the forming voltage. This behavior is correlated to the high current levels reached in the low resistance state which originate a remarkable physical degradation of the top metal electrode. These results point out the importance of considering current excess in the reset phase.

Keywords: Ni, HfO_2, MIS, Resistive switching, RRAM.

1. Introduction

Nowadays, NAND Flash technology dominates the non-volatile memory market [1]. However, these memories are currently reaching the scaling limit because their information retention capability is seriously affected by the reduction of the vertical dimension of the gate stack [2]. To overcome this limitation, a number of alternative non-volatile memory technologies have recently been proposed [3]. In this connection, resistive random access memory (RRAM) is considered a promising candidate to substitute Flash [4]. This type of memory consists in a capacitor-like structure with an insulating film sandwiched between two metal electrodes (MIM structure), or one metal electrode and one semiconductor electrode (MIS structure) in which a filamentary pathway is created. If materials are properly chosen, these memory devices are CMOS-compatible with the potentiality of having high scalability, low power consumption, and a high write/read speed.

RRAM devices rely on the resistive switching (RS) mechanism [4], which is related to the alternate switching between two different resistive states, the high resistance state (HRS) and the low resistance state (LRS). The occurrence of these two states is attributed to the formation and rupture of a conductive filament (CF) spanning the dielectric film [5, 6]. The CF is generated by the diffusion of conductive defects as a consequence of the application of an electric field. The transition from HRS to LRS is referred to as the set process, whereas the opposite transition is called the reset process.

Among the different materials used for the fabrication of RRAM devices, HfO_2-based RRAM devices have shown good RS performance [7, 8]. In the case of MIS structures with Ni as top metal electrode, unipolar resistive switching is observed, *i.e.* the set and reset processes occur for the same voltage polarity. For positive voltages, the RS behavior is associated to the generation and degradation of Ni CF [9, 10]. In these devices, two mechanisms contribute to RS: electrochemical diffusion, where Ni cations migrate from the positive electrode (anode) to the negative electrode (cathode) to be reduced and deposited; and metallic migration by Joule heating, where the Ni is melt and dissolved in the dielectric. During set both mechanisms contribute whereas during reset the Joule heating occurs [10-12].

In order to use these devices as memory cells, their reliability must be evaluated. In this work, the degradation of Ni/HfO_2/n^+-Si devices during RS cycling is analyzed and the impact of the electrical stress on the device physical characteristics evaluated. After assessing the resistive switching behavior under positive bias, an unusual electrical behavior is observed which has been attributed to the degradation of the metal electrode as observed by scanning electron microscope (SEM) inspection of the HfO_2 surface after Ni removal. This effect would represent a reliability concern and would eventually lead to device failure.

2. Experimental

2.1. Samples Description

The studied devices are field-oxide isolated Ni/HfO_2/n^+-Si capacitors with two HfO_2 thicknesses, 20 nm and 10 nm, and active areas of 5×5 μm^2 and 2×2 μm^2. The devices were fabricated on (100) n-type CZ silicon wafers with resistivity (7–13) mΩ·cm according to the following process flow: after a

standard wafer cleaning, a wet thermal oxidation process was carried out at 1100 °C leading to a 200-nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Prior to the HfO_2 deposition, a cleaning in H_2O_2/H_2SO_4 and a dip in HF (5 %) were done. The HfO_2 layer was grown by atomic layer deposition at 225 °C using Tetrakis (Dimethylamido)-Hafnium (TDMAH) and H_2O as precursors, and N_2 as carrier and purge gas. The top metal electrode, a 200-nm-thick Ni layer, was deposited by magnetron sputtering and patterned by a lift-off process. A top-view optical image of a 2×2 μm^2 device is shown in Fig. 1.

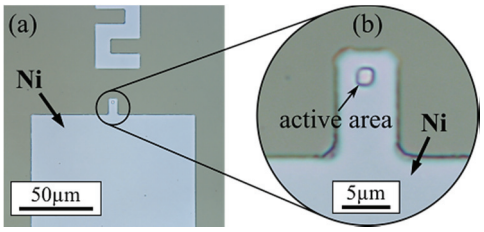


Fig. 1. (a) Optical image of a pristine Ni/HfO_2/n^+-Si device. (b) Zoom in image of the 2×2 μm^2 active area.

2.2. Characterization Procedure

Current–voltage (I-V) characteristics of the devices were measured at room temperature using a HP-4155B semiconductor parameter analyzer. The voltage was applied to the top Ni electrode, while the Si substrate was grounded. In the present investigation, devices were subjected to positive unipolar RS cycles.

In Fig. 2, typical I-V curves corresponding to the forming process and the first RS cycle are shown. Initially, a voltage sweep is applied to the samples for activating the RS property (the forming process) driving the device to the LRS. By applying successive positive voltage sweeps, the device switches from the LRS to the HRS and *vice versa*. Notice that these processes have characteristic voltages: forming ($V_{forming}$), set (V_{set}) and reset (V_{reset}) voltages. The irreversible dielectric breakdown of the HfO_2 film is prevented by using a current limit (I_{cc}) of 100 µA, both in the forming and set processes. A total of 5 and 100 RS cycles were performed to the different devices available.

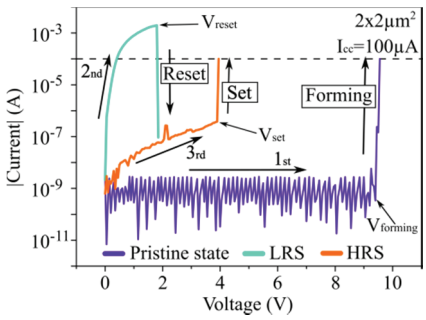


Fig. 2. Typical I-V characteristics of a RS cycle performed on a Ni/20 nm-HfO_2/n^+-Si sample.

In order to analyze the effect of the electrical stress on the physical characteristics of the devices, after the electrical measurements, the Ni layer was etched off using (H_2O:HNO_3) (4:1). In this way the HfO_2 surface was exposed and could therefore be inspected using a SEM.

3. Results and Discussion

3.1. Resistive Switching Assessment

From the experimental characterization of RS, a first analysis corresponds to the forming voltages of the different structures considered. Since $V_{forming}$ is, in fact, the voltage at which the dielectric breakdown occurs, the cumulative probability function, *F*, should follow a Weibull distribution. This is confirmed by the linear Weibull plots obtained for each oxide thickness and device area represented in Fig. 3. As expected, a thicker oxide layer exhibits a higher forming voltage, and, for each thickness, a larger device area exhibits a lower forming voltage. In Table 1 a summary of the most significant parameters is reported.

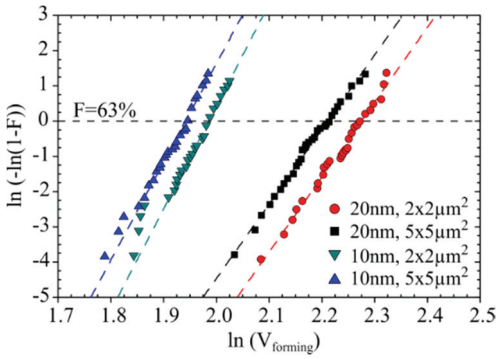


Fig. 3. Weibull plot of the forming voltages ($V_{forming}$ in V) for the different types of devices.

Table 1. Fitting parameters of the Weibull plots.

HfO_2 thickness (nm)	Area (μm^2)	$V_{forming}$ (V) (F=63 %)	Slope
20	5×5	9.13	21.1
20	2×2	9.72	21.3
10	5×5	6.97	27.9
10	2×2	7.30	29.0

Typical I-V characteristics for 5 RS cycles are plotted in Fig. 4 for the two oxide thicknesses investigated. They show unipolar resistive switching behavior: the set process occurs at voltages lower than $V_{forming}$, and the reset process takes place at voltages lower than V_{set}. This is the most common behavior observed. However, in some devices, as the RS cycling proceeded, at some point V_{set} values higher than $V_{forming}$ were measured (Fig. 6(d)), being this phenomenon observed for both areas and dielectric thicknesses.

The statistical analysis of the RS parameters is represented in Fig. 5 for devices with 20 nm-thick HfO_2 and 100 RS cycles. In Fig. 5(a), the Cumulative Distribution Function (CDF) for V_{set} and V_{reset} are given for the two device active areas. The mean and standard deviation values of these two parameters are indicated in Table 2. In Fig. 5(b), CDF of the current values at $V = 0.5$ V are represented, corresponding to a LRS resistance mean value of 2.4×10^3 Ω (2.4×10^3 Ω) for devices with area 5×5 μm² (2×2 μm²) and to a HRS resistance mean value of 3×10^6 Ω (3.8×10^7 Ω) for devices with area 5×5 μm² (2×2 μm²).

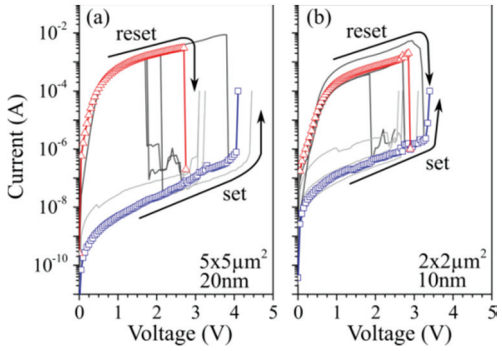


Fig. 4. Typical I-V characteristics of 5 RS cycles for devices with (a) 20 nm-thick HfO_2 and area 5×5 μm², and (b) 10 nm-thick HfO_2 and area 2×2 μm².

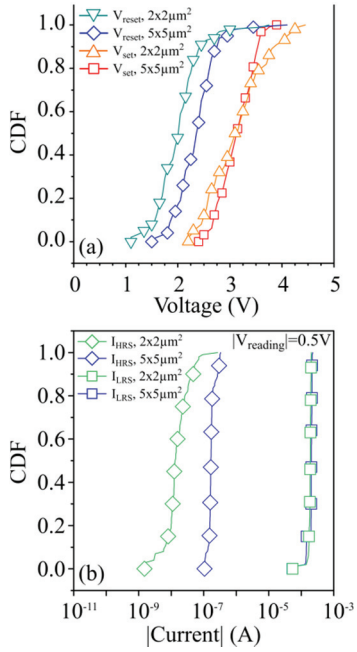


Fig. 5. Cumulative Distribution Function (CDF) of (a) the set and reset voltages and (b) the current at $V = 0.5$ V at the HRS (I_{HRS}) and the LRS (I_{LRS}) for 100 RS cycles in devices with a 20 nm-thick HfO_2 layer. Results for the two active areas are shown.

Table 2. Mean and standard deviation of V_{set} and V_{reset}.

Area (μm²)	V_{set} (V)		V_{reset} (V)	
	Mean	St. Dev.	Mean	St. Dev.
5×5	2.96	0.53	2.34	0.38
2×2	3.11	0.54	1.99	0.43

3.2. Physical Characterization

After performing the electrical characterization of the devices with typical RS behavior, the SEM inspections after Ni etching revealed a small hillock (see Fig. 6(a)) on the HfO_2 surface likely located at the CF position, similarly to the results reported for negative unipolar RS [13].

In the case of devices showing set voltages larger than the forming voltage, however, SEM inspections indicated that the metal layer was severely damaged, with a large structure extending not only on the active area but also over the contact pad. This is shown in Fig. 6(b), which corresponds to a device with a 10 nm-thick HfO_2 layer and whose I-V characteristics are represented in Fig. 6(d). The generation of this structure was observed in all the samples in which $V_{set}>V_{forming}$, yet it was also observed in some samples with $V_{set}<V_{forming}$. Moreover, this large degraded area in the top metal electrode was more frequent for devices with areas of 2×2 μm² than of 5×5 μm².

In order to explain the observed consequences of degradation in these devices, the cycling I-V characteristics were thoroughly analyzed. Previous to the anomalous behavior, a reset sweep with current values higher than 10 mA was detected in all devices showing this type of behavior, for both HfO_2 thicknesses. Not only was the effect observed in experiments consisting in 5 RS cycles but also in longer experiments. As an example, the results obtained for a 20 nm-thick HfO_2 in a 100 RS-cycles experiment are shown in Fig. 7.

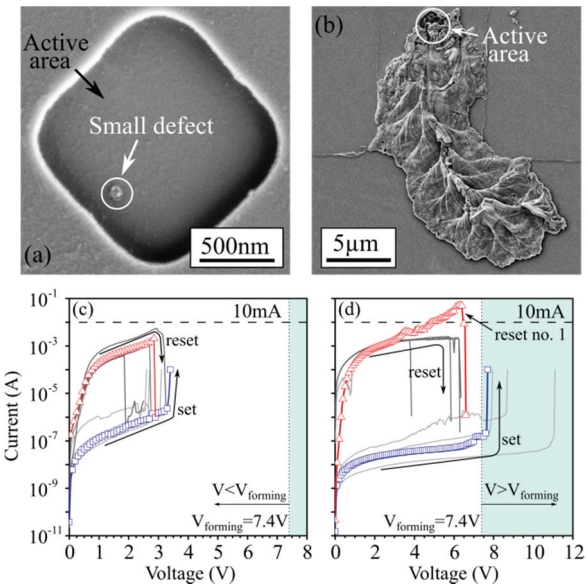


Fig. 6. SEM images after Ni etching of devices with a 10 nm-thick HfO_2 layer of (a) a device with the I-V characteristics shown in (c), and of the unusually degraded device (b) with the electrical characteristics in (d).

Note that, when plotting the V_{set} and V_{reset} values as a function of the cycle number (see Fig. 7(b)), V_{set} is lower than $V_{forming}$ until cycle no. 45 is reached. After this cycle not only V_{set} and V_{reset} increase but also their

variability. As indicated in Fig. 7(a), at cycle number 45, the current slowly increases over 10 mA until the resistance switches from the LRS to the HRS, i.e., the same behavior as in the case of the device shown in Fig. 6(d). Note that in these reset processes, the current slowly increases to values higher than 10 mA, meaning that the degradation is progressive. These results point out that during these resets, the thermal energy dissipated by Joule effect is high enough to melt the top electrode and generate the structures observed in Fig. 6(b) and Fig. 7(b).

It is important to mention that despite large set voltages are needed, the device still shows RS cycles. So the high energies dissipated and the damage generated did not destroy the switching capability of the device. Just higher voltages are required to induce the resistance transitions.

A possible explanation for the increase of V_{set} and V_{reset} is that degradation operates as a series resistor with the MIS device. Therefore, only part of the voltage sourced by the measurement system drops across the CF, *i.e.* high V_{set} values measured are overestimated.

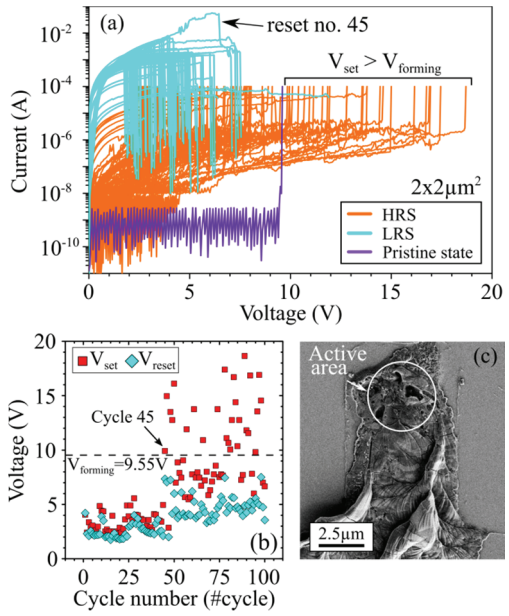


Fig. 7. (a) I-V characteristics of a sequence of 100 RS cycles in a Ni/20 nm-HfO_2/n^+-Si structure with an anomalous behavior. (b) V_{set} and V_{reset} values as a function of cycle number. The dashed line indicates the $V_{forming}$ value. (c) SEM image of the device after Ni etching.

4. Conclusions

Unipolar RS cycling of Ni/HfO_2/n^+-Si devices can cause severe physical degradation of the Ni electrode. In the vast majority of cases, small defective structures are generated likely localized at the CF position. However, when the current in the low resistance state reaches values higher than 10 mA, the high energies dissipated by Joule heating at the very moment of the reset event, lead to the appearance of a large damaged area in the metal electrode. Despite the devices are still switching, higher set voltages are needed and variability increases. This is a serious reliability concern. Moreover, the large damaged area can extent to adjacent devices when placed in a cross-bar configuration. In view of these results, limiting the current in the low resistance state would be also compulsory to prevent physical degradation of the metal electrode.

Acknowledgements

This work has been partially funded by the Spanish MINECO and FEDER though projects TEC2014-52152-C3-1-R, TEC2017-84321-C4-4-R, and TEC2014-54906-JIN. The authors acknowledge the reviewer's suggestions to improve the quality of this paper.

References

[1]. J. S. Meena, S. M. Sze, U. Chand, T-Y Tseng, Overview of emerging nonvolatile memory technologies, *Nanoscale Research Letters*, Vol. 9, 2014, 526.

[2]. K. Prall, Scaling non-volatile memory below 30 nm, in *Proceedings of the IEEE Non-Volatile Semiconductors Memory Workshop*, 2007, pp. 5-10.

[3]. B. DeSalvo, V. Sousa, L. Perniola, C. Jahan, S. Maitrejean, J. F. Nodin, C. Cagli, V. Jousseaume, G. Molas, E. Vianello, C. Charpin, E. Jalaguier, Emerging memory technologies: challenges and opportunities, in *Proceedings of the International Symposium on VLSI Technology, System, and Applications (VLSI-TSA'12)*, 2012, pp. 1-2.

[4]. J. S. Lee, S. Lee, T. W. Noh, Resistive switching phenomena: A review of statistical approaches, *Applied Physics Reviews*, Vol. 2, 2015, 031303.

[5]. L. Goux, I. Valov, Electrochemical processes and device improvement in conductive bridge RAM cells, *Physica Status Solidi A*, Vol. 213, 2016, pp.274-288.

[6]. K. M. Kim, D. S. Jeong, C. S. Hwang, Nanofilamentary resistive switching in binary oxide system; a review on the present status and outlook, *Nanotechnology*, Vol. 22, Issue 25, 2011, pp. 1-17.

[7]. B. L. Ji, Q. Ye, S. Gausepohl, S. Deora, D. Veksler, S. Vivekanand, H. Chong, H. Stamper, T. Burroughs, C. Johnson, M. Smalley, S. Bennett, V. Kaushik, J. Piccirillo, M. Rodgers, M. Passaro, M. Liehr, In-Line-Test of variability and bit-error-rate of HfO_x-based resistive memory, in *Proceedings of the IEEE International Electron Devices Meeting (IEDM'14)*, 2014, pp. 1-4.

[8]. K. L. Lin, T. H. Hou, Y. J. Lee, J. W. Chang, J. H. Lin, J. Shieh, C. T. Chou, T. F. Lei, W. H. Chang, W. Y. Jang, C. H. Lin, Switching mode and mechanism in binary oxide resistive random access memory using Ni electrode, *Japanese Journal of Applied Physics*, Vol. 52, 2013, pp. 1-5.

[9]. K. L. Lin, T. H. Hou, J. Shieh, J. H. Lin, C. T. Chou, Y. J. Lee, Electrode dependence of filament formation in HfO_2 resistive-switching memory, *Journal of Applied Physics*, Vol. 109, 2011, 084104.

[10]. A. Rodríguez-Fernández, S. Aldana, F. Campabadal, J. Suñe, E. Miranda, F. Jiménez-Molinos, J. B. Roldán,

M. B. Gonzalez. Resistive switching with self-rectifying tunability and influence of the oxide layer thickness in Ni/HfO_2/n+-Si RRAM devices, *IEEE Transactions on Electron Devices*, Vol. 64, Issue 8, 2017, pp. 3159-3166.

[11]. X. Wu, D. Cha, M. Bosman, N. Raghavan, D. B. Migas, V. E. Borisenko, X. X. Zhang, K. Li, K. L. Pey, Intrinsic nanofilamentation in resistive switching. *Journal of Applied Physics*, Vol. 113, 2013, 114503.

[12]. X. Wu, S. Mei, M. Bosman, N. Raghavan, X. Zhang, D. Cha, K. Li, K. L. Pey, Evolution of filament formation in Ni/HfO_2/SiO_x/Si-based RRAM devices, *Advanced Electronic Materials*, Vol. 1, 2015, 1500130.

[13]. S. Claramunt, Q. Wu, M. Maestro, M. Porti, M. B. Gonzalez, J. Martin-Martinez, F. Campabadal, M. Nafría, Non-homogeneous conduction of conductive filaments in Ni/HfO_2/Si resistive switching structures observed with CAFM, *Microelectronic Engineering,* Vol. 147, 2015, pp. 335-338.

(031)

Off-the-Shelf Implementation of a Memcapacitor Emulator Based on Voltage Amplifier with Flux-Controlled Gain

F. Romero [1], A. Medina [1], D. Gamez [1], A. Godoy [1], D. Morales [1], A. Ohata [2] and N. Rodriguez [1]
[1] Pervasive Electronics Advanced Research Laboratory, Fac. Ciencias, University of Granada, Campus Fuente Nueva SN, 18071 Granada, Spain
[2] Japan Aerospace Exploration Agency, Kanagawa, Japan
Tel.: + 34 958 241 000 ext. 20053
E-mail: franromero@ugr.es

Summary: In this work we present a voltage-controlled memcapacitor emulator fully implemented with commercially available electronic components. The circuit is based on a voltage amplifier with flux-controlled gain. As a result of the Miller effect, over a feedback capacitor, the input capacitance is modulated according to the input flux. The feasibility of the proposed circuit has been verified through a practical implementation. The experimental measurements confirm that the circuit behavior follows the model of a memcapacitor.

Keywords: Memcapacitor, Miller effect, Voltage-gain, Amplifier.

1. Introduction

Since its inception, the memristor (circuit element relating the electrical magnitudes charge (q) and flux (φ) [1]), has attracted the attention of many researches because its application in different emerging areas, such as storage-class memories or neuromorphic computing. The concept of mem-devices, where the memristor belongs, was generalized to capacitive and inductive devices in 2009 [2]. Nonetheless, and in contrast to memristors, due to the technical difficulties associated to the fabrication of solid-state memcapacitors (or meminductors), device emulators have been proposed to replace them in practical research implementations [3-6] until they become available.

This work presents a novel and simple implementation with off-the-shelf components of a memcapacitor emulator based on the Miller effect: Section 2 introduces the relationship between Miller effect and memcapacitance; Section 3 presents an implementation with commercially available analog components completed with its experimental test; and finally, the main conclusions are drawn in Section 4.

2. Memcapacitance and Miller Effect

Memcapacitance (C_M) establishes a n^{th}-order non-linear relation between charge (q) and voltage (v) over time (t) [2]:

$$q(t) = C_M(\boldsymbol{x_n}, v, t)v(t), \tag{1}$$

$$d\boldsymbol{x_n}/dt = f_M(\boldsymbol{x_n}, v, t). \tag{2}$$

C_M depends on the state-vector (history) of the system ($\boldsymbol{x_n}$). A particular case of memcapacitive systems is the voltage-controlled memcapacitor [2], whose capacitance only depends on the input flux ($x = \varphi$):

$$q(t) = C_M(\varphi)v(t), \tag{3}$$

where the flux is defined as the time integral of the voltage:

$$\varphi = \int_{t_0}^{t} v(\tau)d\tau, \tag{4}$$

The proposed emulator circuit, shown in Fig. 1a, can be modelled by Eq. (3) thanks to the Miller effect. It mirrors the role of a voltage-controlled memcapacitor since its input impedance, Z_{in}, corresponds to a capacitance whose value depends on the flux of the input voltage as is derived below.

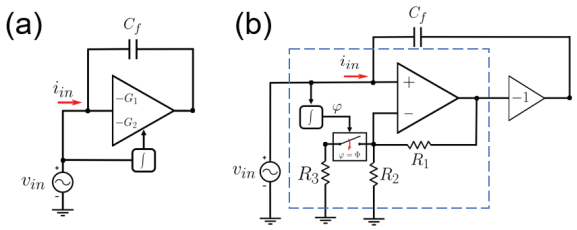


Fig. 1. (a) Simplified schematic of the proposed memcapacitor emulator circuit based on the Miller effect. The flux switches the amplifier voltage-gain according to a flux threshold-level, (b) Detailed circuit implementation. The dotted rectangle encloses the flux-controlled gain amplifier.

Assuming that the amplifier operates in ideal conditions, the input impedance of the circuit in Fig. 1a, is given by Eq. (5).

$$Z_{in}(s) = \frac{v_{in}(s)}{i_{in}(s)} = \frac{Z_{C_f}(s)}{1-G} = \frac{1}{s\cdot(1-G)\cdot C_f}, \qquad (5)$$

where C_f is the feedback capacitance connecting the input and output terminals of the amplifier and G the voltage-gain. Therefore, the input capacitance is *1-G* times the value of C_f (Miller effect). But, as indicated in Fig. 1a, the underlying feature to achieve the memcapacitive behavior is to implement a switchable amplifier gain as a function of the flux level:

$$G(\varphi) = \begin{cases} -G_1 & if\ \varphi \le \Phi \\ -G_2 & if\ \varphi > \Phi \end{cases}, \qquad (6)$$

being Φ the threshold value of the flux (triggering flux). In this way, the circuit of Fig. 1a, can be modelled as a memcapacitor, where the input capacitance (memcapacitance), C_M is given by:

$$C_M = C_f \cdot \big(1 - G(\varphi)\big). \qquad (7)$$

3. Implementation and Experimental Results

The practical circuit of the memcapacitor emulator of Fig. 1a is schematized in Fig. 1b and its implementation with off-the-shelf devices shown in Fig. 2a. Two dual-operational amplifiers (LM358 [8]) were used to implement the voltage integrator, the inverting output amplifier and a flux-threshold comparator, the output of which enables/disables an analog switch (ADG1219 [9]) to control the gain of the amplifier stage.

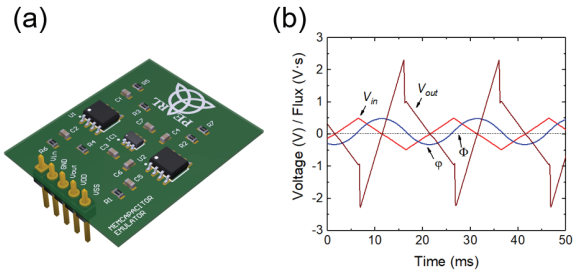


Fig. 2. (a) Prototype of the memcapacitor emulator using commercial devices, (b) Experimental result of the output voltage of the amplifier for a triangular input signal (f = 50 Hz). A gain switching can be appreciated according to the flux-level (φ) and the triggering flux value (Φ).

The configuration selected for this demonstrator includes: C_f = 10 nF, G_1 = 2 V/V, G_2 = 5 V/V and Φ = 0 V·s. The gains of the amplifier are achieved by discrete resistors (R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 3.3 kΩ) according to Fig. 1b. The time-domain results, shown in Fig. 2b, demonstrate the gain switching according to the flux level when the input is a triangular signal of 500 mV of amplitude and 50 Hz of frequency. Fig. 3a shows the pinched hysteresis loop of the *q-v* curve, which is the distinctive electrical signature of memcapacitors [2]. As seen, q is zero whenever v_{in} is zero, fulfilling the condition of Eq. (3). Fig. 3b shows the measured input capacitance, switching between the two values given by Eq. (7). As noticed, there are two possible values of capacitance for a given voltage, depending the one seen at the input of the emulator on the history of the circuit (flux).

Finally, we would like to mention that several units of the prototype presented can be combined to conform more complex networks with the aim of assessing neuromorphic circuits.

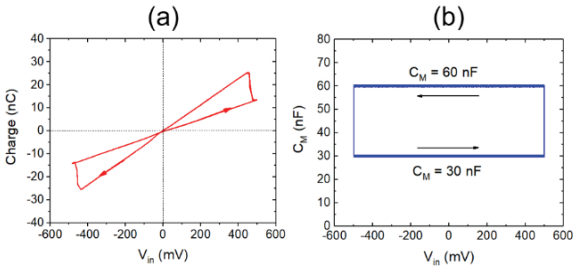


Fig. 3. (a) Experimental pinched hysteresis loop of the *q-v* characteristic of the emulated memcapacitor with a triangular input signal at the frequency of f = 50 Hz, (b) Capacitance values as a function of the input voltage showing two levels.

4. Conclusions

A memcapacitor emulator circuit, fully implemented with off-the-shelf components, has been presented. The constitutive equations of memcapacitance are satisfied thanks to the Miller effect over a physical capacitor and a flux-controlled gain. This result constitutes one of the simplest and more powerful approaches to replicate a voltage-controlled memcapacitive system.

Acknowledgements

This work has been supported by the Spanish Government through the projects TEC2017-89955-P, TEC2017-92416-EXP, TEC2014-59730, and the grant FPU16/01451.

References

[1]. L.O. Chua, Memristor – The missing circuit elements, *IEEE Transactions Circuit Theory,* Vol. 18, Issue 5, 1971, pp. 507-519.

[2]. M. D. Ventra, Y. V. Pershin, L. O. Chua, Circuit elements with memory: memristors, memcapacitors, and meminductors, *Proceedings of the IEEE*, Vol. 97, Issue 10, 2009, pp. 1717-1724.

[3]. X. Y. Wang, A. L. Fitch, H. H. C. Iu, W. G. Qi, Design of a memcapacitor emulator based on a memristor, *Physics Letters A*, Vol. 376, Issue 4, 2012, pp. 394-399.

[4]. M. P. Sah, C. Yang, R. K. Budhathoki, H. Kim, H. J. Yoo, Implementation of a Memcapatiro emulator with off-the-shelf devices, *Elektronika ir Elektrotechnika*, Vol. 19, Issue 8, 2013, pp. 54-58.

[5]. D. S. Yu, Y. Liang, H. Chen, H. H. C. Iu, Design of a pratical memcapacitor emulator without grounded restriction, *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 60, Issue 4, 2013, pp. 207-211.

[6]. M. P. Sah, R. K. Budhathoki, C. Yang, H. Kim, Mutator-based meminductor emulator for circuit applications, *Circuits, Systems, and Signal Processing*, Vol. 33, Issue 8, 2014, pp. 2363-2383.

[7]. J. M. Miller, Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit, *Scientific Papers of the Bureau of Standards*, Vol. 15, Issue 351, 1920, pp. 367-385.

[8]. LM358, LM258, LM158, LM2904, Dual Operational Amplifiers Datasheet, *Texas Instrument*, 2017.

[9]. ADG1219: Low Capacitance, Low Charge Injection, ±15 V/12 V iCMOS SPDT in SOT-23, *Analog Devices*, 2017.

(033)

Investigation of the Changes in the Electronic Properties of Spray Deposited Zirconium Oxide Films as a Function of UV-Ozone Treatment

Abayomi T. Oluwabi, Ilona Oja-Acik, Atanas Katerski, Erki Kärber, Arvo Mere and Malle Krunks
Laboratory of Thin Film Chemical Technologies, Department of Materials and Environmental Technology, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia
Tel.: +372-6203369, fax: +372-6202798
E-mail: abayomioluwabi@gmail.com

Summary: UV-ozone treatment of sprayed zirconium oxide (ZrO_x) thin film was adopted before making a capacitor with Al/ZrO_x/p-Si structure. Atomic Force Microscopy reveals a smooth, and dense film with root mean square roughness ~0.26 nm for UV-ozone treated ZrO_x dielectric films. The electrical performance of the device was tested through current voltage (I-V) and impedance characterization; which showed that by increasing the UV-ozone exposure time, the leakage current density was reduced by 3 orders of magnitude, and the capacitance was in the range 290-266 nF/cm^2. The thickness of the zirconium oxide layer was around 20 nm and the calculated relative permittivity (k) at 1 kHz was in the range 5.8-6.6, varying with sample treatment duration. The surface wettability measurement revealed a reduction in the films contact angle from 48^o to 7^o at increasing the UV-ozone exposure time from 0 to 2 hours.

Keywords: Spray pyrolysis, Zirconium oxide, Thin Film Transistor, UV-Ozone, XPS, Wettability, High-k oxides.

1. Introduction

Zirconium oxide (ZrO_x) semiconductor material offers excellent applicability in flexible electronics [1], thin film transistors (TFT) [2], sensors [3, 4], display technology [1], and memory technology [5, 6] due to its unique thermal stability, optical, and electronic properties. Additionally, in TFT applications ZrO_x has been employed as a plausible replacement for silicon oxide dielectric layer, owing to its high permittivity (k) (~25), band gap (5.1-7.8 eV), and low leakage current [7-9]. The fabrication of ZrO_x dielectrics by a wet chemical process still lags behind, because of high processing temperature (above 400 ^{o}C), arising from the need to decompose or degrade the large organic moiety from the films matrix, which in turn could lead to high thermal budget [10, 11].

Different authors have reported solution-processed high-k ZrO_x dielectric films with good quality after several heat treatment conditions and the fabricated devices exhibited promising electrical performance [12-15]. In comparison with semiconductor thin films, solution-processed high-k dielectrics generally need high annealing temperatures to attain the compact structure needed to prevent leakage current. For instance, according to Park et al., peroxo-ZrO_x dielectric exhibited a low leakage current with high breakdown strength (3.4 MV/cm) at 500 ^{o}C [12]. Lee et al. [13] fabricated a solution-processed ZrO_x TFT on a glass substrate; however, the desired carrier mobility (~25 cm^2/Vs) was achieved at high annealing temperature of 500 ^{o}C. Ha and co-workers [14] employed solution-processed ZrO_x as a gate dielectrics layer of ZTO-TFTs, which demonstrated low operating voltage (<5 V) and high channel carrier concentration; however, the optimized annealing temperature of the ZrO_x dielectric film was as high as 500 ^{o}C. Oja et.al [16], Juma et.al [17], and Oluwabi et. al [18, 19] have deposited metal oxide films by spray pyrolysis; however, the desired morphology, and electrical properties was attained after annealing at temperatures above 700 ^{o}C.

In recent years, different approaches have been reported regarding material selection, and curing conditions that can reduce the processing temperature (<250 ^{o}C) of solution processed films [20-22]. These approaches can be grouped into: (1) chemical methods that deals with the chemistry of precursor solution to facilitate low external temperature [23]. Example of such approach is combustion synthesis [10, 24, 25], and (2) annealing methods that uses alternative energy source or mediated annealing conditions to reduce processing temperature of metal oxides thin films [23]. Examples of such approach are vapor, photo, and vacuum annealing [26], to decrease the processing temperature of conventional solution processed films.

Among annealing methods, photo-assisted annealing, such as UV, laser, and pulsed light, are hopeful alternative to traditional high-thermal annealing, because light energy can directly illuminates the surface of the film, thereby, efficiently utilizing the energy from the light source. For example, Kim et al. proposed an effective way to fabricate solution-processed metal oxide films using deep ultraviolet (DUV) irradiation at 150 °C [27]. Although the approach was highly efficient, but the high cost of such UV equipment may render it unattractive for production. Therefore, it is of great significance to develop a facile and low-cost route to fabricate high-

quality dielectrics, which would be suitable as a gate-dielectric layer in TFT application.

Herein we present a systematic study of the effect of a cost-effective UV-ozone (UVO) treatment at room temperature for solution-processed zirconium oxide (ZrO_x) dielectric. The film was deposited by chemical spray pyrolysis method, and the influence of UVO treatment was investigated: on both the films surface, and electrical properties. It is essential to point out that UVO treatment is newly introduced for spray deposited ZrO_x dielectric films and it will be informative for future studies, opening the possibility to deposit metal oxide films onto flexible substrates for electronic applications. The deposition temperature reported in this study differs from a related work on the characterization of ZrO_x deposited by a chemical method [28]. Most literature usually adopts thermal annealing plus UV treatment, whereas in this present work, the photochemical post-deposition treatment was done at room temperature.

1.1. Mechanism of UV-ozone Irradiation

The mechanism of UVO irradiation has been widely studied owing to its broad applicability in different fields. For the production of ozone, two regions of wavelength have been significantly reported the light with $\lambda < 243$ nm splits the atmospheric oxygen molecules, while the light with $240 < \lambda < 320$ nm decomposes ozone molecules to oxygen free radicals (O), which effectively performs the oxidative treatment of the ZrO_x films. The chemical reactions involved when the atmospheric air is used for ozone production are illustrated as follows [29]:

$$O_2\,(\text{air}) + (\lambda<243\ \text{nm}) \rightarrow 2O.\ (\text{free radicals}),$$

$$O\cdot + O_2 \rightarrow O_3\ (\text{Ozone}),$$

$$O_3 + (240\ \text{nm} < \lambda < 320\ \text{nm}) \rightarrow O_2 + O,$$

$$O\cdot + O_3 \rightarrow 2O_2$$

2. Experimental Details

The films were deposited (T_{dep}) at 200 °C by the ultrasonic spray pyrolysis (USP) technique, which utilizes a nebulizer operated at 1.5 MHz. The nebulized precursor solution consisted of Zirconium acetylacetate ($Zr(acac)_4$) and methanol. The resulting aerosol was transported onto a heated p-Si-wafer with the aid of air as the carrier gas (flow rate; 3 L/min). After the deposition process, UVO cleaning process was carried out using a commercially available UVO system (NOVASCAN PSD-series) with UV-light (184.9 nm and 253.7 nm) generated from mercury vapor lamp. The UVO exposure time was varied at 30, 60, and 120 min respectively. The corresponding sample data in fig. are labelled as UVO-0, UVO-30, UVO-60, UVO-120 for 0, 30, 60, and 120 min of exposure time, respectively.

The surface morphology of the films was studied using a NT-MDT solver 47 pro Atomic Force Microscopy (AFM) system; the measurement was performed in the non-contact mode with a resolution in the range of 3 nm, and the investigated area was 500 nm × 500 nm per scan. The surface morphology of the samples was analyzed through the 3D AFM scan, and surface roughness was analyzed in accordance with the ISO 4287/1 standard. The wettability of the ZrO_x dielectric films was studied using a DSA 25-KRÜSS instrument. The contact angle (CA) of water on the film surface was measured at room temperature using the sessile drop fitting method. X-ray photoelectron spectroscopy (XPS) measurements were performed on a Kratos Axis Ultra DLD (delay line detector) spectrometer in conjunction with a 165 mm hemispherical electron energy analyzer. Analyses were carried out with a monochromatic Al Kα X-ray source (1486.6 eV) operating at 150 W. The XPS spectra were recorded using an aperture slot of 300 μm × 700 μm and a base pressure of 2×10^{-9} Torr. The spectrometer was configured to operate with a 20 eV pass energy and a 90° take-off angle from the surface. The spectra were calibrated using C 1s core level peak centered at a binding energy of 285.0 eV.

Al contact were made using Quorum K975X vacuum evaporator on top of the ZrO_x film surface with a contact area of 1.7 mm^2, giving $Al/ZrO_x/p\text{-}Si$ structure. The crystalline p-Si wafer was contacted through indium metal electrode. The I-V curves were measured by applying a DC bias voltage from -1 to 1 V, while impedance measurements were taken by applying AC signal of amplitude 20 mV in the frequency range of 100 Hz – 1 MHz using AUTOLAB PGSTAT30/2.

3. Results and Discussion

3.1. Surface Morphology and Wettability

Fig. 1 shows the AFM deflection images for both untreated (Fig. 1a) and UVO-treated (Fig. 1b, c) ZrO_x dielectric films. The root mean square (RMS) roughness value was calculated from the AFM height profile of a scanned area 500 nm × 500 nm. The UVO-treated dielectric films demonstrated a lower surface roughness (0.26, 0.32 nm for UVO-30, and UVO-60 respectively) than untreated ZrO_x dielectric films (0.43 nm for UVO-0), indicating that by increasing the UVO exposure time, the surface of the ZrO_x dielectric film became significantly smoother. Generally, it is important that the gate-dielectric layer of a TFT device is sufficiently smooth for a reliable device performance [10]. The surface roughness reduction due to UVO treatment could be a result of removal of complex organic ligands from the film surface and formation of a dense metal-oxygen-metal bond network [11].

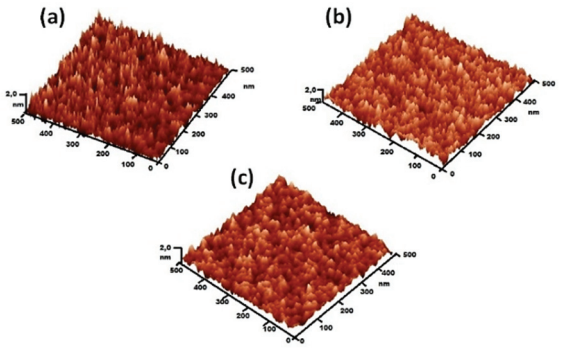


Fig. 1. AFM morphologies of (a) UVO-O, (b) UVO-30, (c) UVO-120 ZrOx thin films.

The wettability of the ZrO_x dielectric surface was studied by measuring the water contact angle (CA). Fig. 2 shows the droplet pictures alongside the mean CA values of water on both UVO-0 and UVO-120 treated ZrO_x dielectric films. It also shows the changes in CA values with aging. In the observed results, the UVO-120 treated ZrO_x dielectric is super-hydrophilic with CA of 7, while the UVO-0 film is hydrophilic with CA of 48. A similar behavior was reported for ZrO_x thin films grown by dip-coatings [30]; however, for ZrO_x dielectric films deposited by both sputtering [31] and electrochemical methods [32], a hydrophobic property was indicated. Gromyko et.al have also reported a difference in CA values for ZnO rod grown by both spray and electrodeposition methods [33].

Furthermore, after both samples were kept in a Petri-dish they were allowed to age for three days. It was observed that the CA increases slightly in both UVO-120 and UVO-0 ZrO_x dielectric films. This suggests that the hydrophilic properties could be lost because of surface contamination or adsorption of moisture (water molecule). For example, the surface oxidative treatment of the ZrO_x dielectric film occurs simultaneously with the removal of the organic compound present on the film surface, which in turn makes the surface very active. The wettability result supports the AFM result as explained earlier in this section.

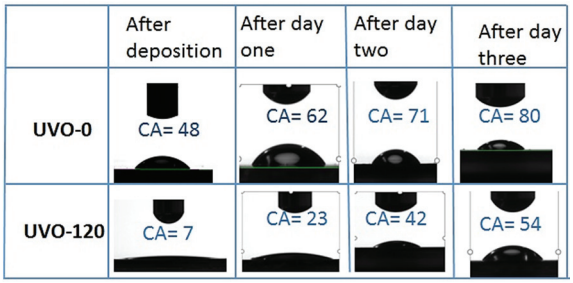


Fig. 2. Images of the contact angle measurements (water) for both treated (UVO-120) and untreated (UVO-O) ZrO_s thin film and their corresponding contact angle after aging for three days.

3.2. XPS Characterization

To study the surface composition of the deposited ZrOx dielectric film, XPS measurement was carried out. Fig. 3 shows the survey XPS spectra for both the UVO treated and untreated ZrO_x dielectric films. The spectra showed zirconium features at Zr 3s (432.4 eV), Zr 3d (182.0, 184.4 eV), Zr 3p (346, 322 eV), and Zr 4p (30.8 eV) [34, 35]. The C 1s peak of adventitious carbon is present at 284.6 eV for all films including the UVO-treated samples. Auger peaks for O (KLL) were also detected at the high binding energy region. The peak intensity of Zr 3d increases slightly with increasing UVO exposure time. In addition, the intensity of O 1s peak was increased. Herein our discussion will be based on the O 1s, and Zr 3d core levels, and making correlation between the UVO-0 and UVO-60 samples.

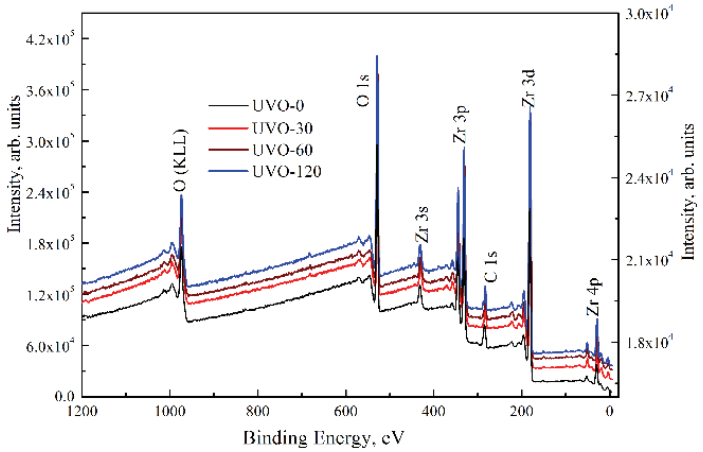


Fig. 3. XPS survey spectra of ZrO_x thin films at different UV-ozone treatment time.

The O 1s binding energies (BE) of UVO-0 and UVO-60 ZrO_x dielectric films are shown in Fig. 4. All the XPS spectra are asymmetric, and they were deconvoluted using Lorentzian-Gaussian (function pseudo-Voigt) distribution. In the O 1s core level of UVO-O sample, the peaks observed were centred at the binding energy (BE) value of 530.0, 531.0, and 532.0 eV. It is known that the peak centred at 530.0 eV

represents the oxygen in the oxide lattice (M-O). Similarly, the peaks located at 531.0 and 532.0 eV were related to the oxygen vacancy in the lattice (V_O) and the bonded oxygen in hydroxide-related (M–OH) species respectively [36, 11]. In contrast to the UVO-O samples, the peaks on the XPS spectra of UVO-60 sample are all located at a higher BE, centred at BE of 530.4, 531.6, and 532.2 eV. It is also known that the peak located at 530.4 eV corresponds to the M-O-M bonding [37, 11], which is an indication that UVO treatment is effective for surface oxidation, thereby leading to the formation of M-O-M network on the dielectric surface. Similar position of M-O-M peak at 530.4 eV has been reported for spin-coated ZrO_x films [11].

Atomic concentrations of all the components (ZrO, Vo, −OH, H_2O) found in O1s core level spectrum of UVO-0, UVO-30, UVO-60, and UVO-120 ZrO_x dielectric films were calculated from integrated areas of the O1s spectrum using Scofield´s cross-sections, and their corresponding values are summarized in Table 1. We found that by increasing the UVO treatment time from 0 min to 120 min, ZrO_x dielectric film demonstrated an increase in the M-O-M, and M-OH bonds, and a decrease in the amount of Vo species. This result corresponds well to the wettability study, suggesting that a high amount of –OH group aided hydrophilicity in the UVO treated ZrO_x dielectric films.

Fig. 5 shows the corresponding XPS spectra of Zr 3d core level for both UVO-0 and UVO-60 ZrO_x thin films. All the films showed the typical Zr 3d spectra with spin-orbit doublets ($d_{5/2}$ = 182.3 eV, and $d_{3/2}$ = 184.7 eV) separated by ~ 2.4 eV, which suggests the formation of ZrO_x thin films [17, 39].

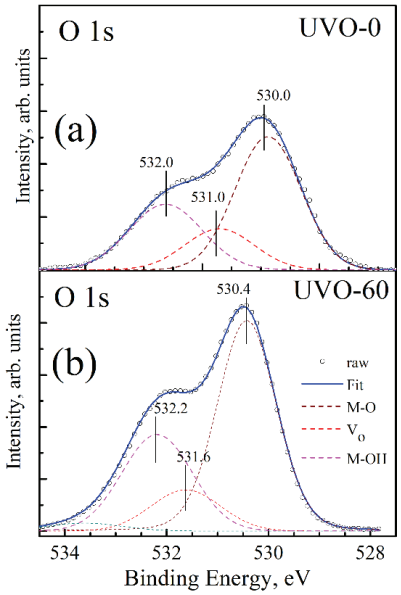


Fig. 4. XPS spectra of O1s core level for (a) UVO-0, (b) UVO-60 ZrO_x dielectric thin films.

Table 1. Binding energy and concentrations of O 1s species for UVO-0, UVO-30, UVO-60, and UVO-120 ZrOx dielectric films.

BE (eV)				Concentration (at %)				Species	Reference
UVO-0	UVO-30	UVO-60	UVO-120	UVO-0	UVO-30	UVO-60	UVO-120		
530.0	530.4	530.4	530.4	27.2	30.2	31.2	29.0	M-O-M	[36, 11]
531.0	531.5	531.6	531.6	17.2	13.2	12.7	10.0	O v	[11, 38]
532.0	532.1	532.2	532.2	29.2	33.4	30.0	34.7	M-OH	[11]
-	-	533.6	533.6	-	-	2.7	9.5	OH abs	[37]

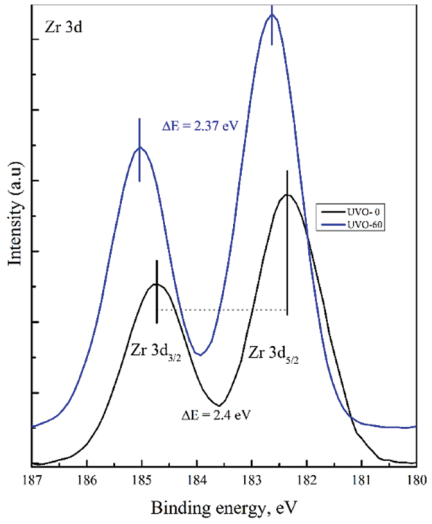


Fig. 5. XPS spectral of Zr 3d core level for (a) UVO-0, and (b) UVO-60 ZrO_x dielectric films.

As the UVO exposure time was increased, both Zr 3d peaks shifted to a higher binding energies. The reason for this shift could be attributed to the progressive oxidization of ZrO_x or to the formation of higher oxidation state M^{n+} ions in the film [40]. Similar BE has been reported for Zr 3d in our previous study on Zr-doped TiO_2 films by spray pyrolysis [17].

3.3. Electrical Characterization

The electrical properties of the ZrO_x dielectric film was assessed by characterizing a metal insulator semiconductor (MIS) capacitor with structure, Al/ZrO_2/p-Si. Fig. 6 shows the plot of leakage current density – voltage (J-V) behavior for ZrO_x dielectric films at different UVO treatment times. An asymmetric behavior can be seen due to the difference in the Schottky barrier height at the electrodes

interface. However, the leakage current was calculated in the reverse bias regime, and it was found that the leakage current in the UVO-0 ZrO_x dielectric film is ~2.0×10^{-5} A/cm^2 at 1 V, a similar result has been reported for ZrO_x dielctric deposited by atomic layer deposition (ALD) [41]. In contrast to the untreated sample, the UVO-treated samples demonstrated a remarkable reduction in leakage current; by increasing the UVO treatment time to 30 min, leakage current was ~ 8.0×10^{-7} A/cm^2 and further increase in exposure time to 2 h yielded a leakage current of ~1.0×10^{-8} A/cm^2 at 1 V. It was reported that UV irradiation ($\lambda > 185$ nm) can produce hydroxyl radical ($OH^{\cdot}$) at a high quantum yield; which however, aids the condensation reaction process of Sol-gel metal oxide precursor films [23]. We inferred that longer UVO exposure time may result in the higher content of metal-oxygen lattice, the lower content of oxygen defects, as shown in the XPS studies (details in Section 3.2), and the degree of densification of ZrO_x film, which effectively helps to reduce the leakage current.

The zero-bias barrier heights of both the untreated and UVO-treated ZrOx dielectric were calculated by fitting the right part of Fig. 6 into the expression [38]

$$\emptyset_B = \frac{kT}{q} In\left(\frac{AA^*T^2}{I_o}\right), \qquad (1)$$

where A is the effective area of the capacitor, A^* the effective Richardson constant is equal to 36 Acm^{-2}T^{-2} for ZrO_2, assuming an electron effective mass 0.3 m_o for ZrO_x, m_o is free electron mass [41, 28], k is the Boltzmann constant, and $\emptyset_B$ is the Schottky barrier height.

The values of $\emptyset_B$ extracted from Eq. (1) amounted to 0.76, 0.84, 1.04, and 1.09 eV for UVO-0, UVO-30, UVO-60, UVO-120 samples respectively. The increase in $\emptyset_B$ could be due to surface changes at the ZrO_x/electrode interface, which is aided by UVO oxidative treatment.

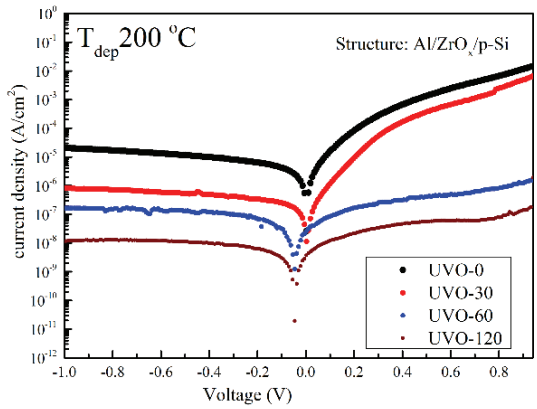


Fig. 6. Current-voltage characteristics of ZrO_x dielctric film at different UVO exposure time under positive and negative biases.

These values compared well with reported in [41, 42]. To explain the changes in the observed barrier height, the effect of charge traps in the dielectric, located at the interfaces of the capacitor constituent layers must be considered [43]. The obtained result is a good indicator for the potential applicability of UVO treatment in reducing the process-temperature of solution-processed dielectric films.

To account for the dielectric property of the deposited ZrO_x films, Capacitance – Frequency (C-F) relation was measured at 0 V biased voltage. Fig. 7 shows the C-F dispersion curve of ZrO_x capacitors measured at different UVO treatment times. The untreated ZrO_x dielectric demonstrated a high capacitance at low frequency region, which suggests the contribution of ionic polarization [10]. On other hand, the UVO-treated samples exhibited a slight increase in capacitance (268, 272, and 290 nF/cm^2 for UVO-30, UVO-60, and UVO-120 samples in respective order), which is stable at the high frequency region. The result obtained from the UVO treated samples revealed that by increasing the UVO exposure time, the contributions from the interface or native oxide capacitance can be eliminated. This result concurs with the AFM, and XPS results on the condensation and defect reduction from the surface of the UVO treated ZrO_x dielectric films.

According to the equation $C = \varepsilon_0 kA/d$: where, 'C' is capacitance, ε_o is the permittivity of free space, 'k' is the relative permittivity, 'A' is the contact area, 'd' is the ZrO_x film thickness (~ 20 nm), the relative permittivity of all the deposited ZrO_x films was calculated. Similar to the capacitance, the value of k increases slightly from 5.8 to 6.6 with an increase in the UVO exposure time. It can be inferred from our previous study on ZrO_x dielectric films by spray pyrolysis that thermal annealing (~800 °C) was needed to obtain k value of 4.8 [19]. However, in this study, with UVO treatment, k value of 6.6 is obtained, thus, indicating the advantage of UVO treatment in improving the properties of high-k oxide dielectric films.

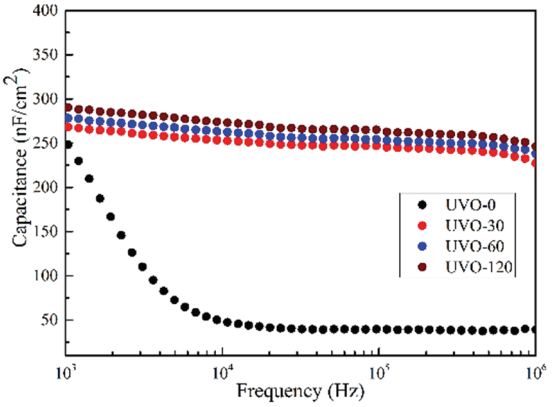


Fig. 7. Relative permittivity curve of Al/ZrOx/p-Si CMOS-device in the frequency range between 1 kHz and 1 MHz.

4. Conclusions

In summary, we demonstrated a good quality low processed temperature ZrO_x dielectric film via

UV-ozone photochemical treatment. The physical and chemical properties of the films were investigated by AFM, wettability, XPS, and electrical measurements. The results showed that by increasing the UVO exposure time, the surface of sprayed ZrO_x dielectric films became more dense, smooth, less defective, and hydrophilic with contact angle down to 7° indicating a successful cleaning property. To demonstrate the electrical performance of the film, a capacitor was fabricated: in which we observed a reduction in the leakage current by 3 orders of magnitude due to the UV-ozone treatment. The UVO treated ZrO_x film attained desirable dielectric properties, such as low leakage current down to 10^{-8} A/cm^2, capacitance of 290 nF/cm^2 and dielectric constant of 6.6 (both at 1 kHz), which elucidates and certifies its applicability as a gate dielectric layer in TFT.

Acknowledgements

This study was financially supported by the Estonian Ministry of Education and Research project IUT194, and by the European Union through the European Regional Development Fund project TK141 "Advanced materials and high-technology devices for energy recuperation systems". Dr. Rainer Traksmaa is appreciated for the AFM measurement.

References

[1]. L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D Anthopoulos, G. Tröster, Metal oxide semiconductor thin-film transistors for flexible electronics, *Appl. Phys. Rev*., Vol. 3, 2016, 021303.

[2]. G. X. Liu, A. Liu, F. K. Shan, Y. Meng, B. C. Shin, E. Fortunato, R. Martins, High-performance fully amorphous bilayer metal-oxide thin film transistors using ultra-thin solution-processed ZrOx dielectric, *Appl. Phys. Lett*., Vol. 105, Issue 11, 2014, 113509.

[3]. S. Avasthi, K. A. Nagamatsu, J. Jhaveri, W. E McClain, G. Man, A. Kahn, J. Schwartz, S. Wagner, J. C. Sturm, Double-heterojunction crystalline silicon solar cell fabricated at 250 °C with 12.9 % Efficiency, in *Proceedings of the* 40th *IEEE Photovoltaic Spec. Conference (PVSC'14)*, 2014, pp. 0949-0952.

[4]. G. Korotcenkov, Metal oxides for solid-state gas sensors: What determines our choice?, *Mater. Sci. Eng. B*, Vol. 139, 2007, p. 1-23.

[5]. D. Ielmini, Resistive switching memories based on metal oxides: Mechanisms, reliability and scaling, *Semicond. Sci. Technol*., Vol. 31, 2016, 063002.

[6]. K. M. Kim, D. S. Jeong, C. S. Hwang, Nanofilamentary resistive switching in binary oxide system: A review on the present status and outlook, *Nanotechnology*, Vol. 22, 2011, 254002.

[7]. C. Y. Chang, W. K. Huang, J. L. Wu, Y. C. Chang, K. T. Lee, C.T. Chen, Room-temperature solution-processed n-doped zirconium oxide cathode buffer layer for efficient and stable organic and hybrid perovskite solar cells, *Chem. Mater.*, Vol. 28, 2015, pp. 242-251.

[8]. H. J. Yoon, K. S. Bang, J. W. Lim, S. Y. Lee, Optical properties of zirconium oxide thin films for semi-transparent solar cell applications, *J. Mater. Sci. Mater. Electron*., Vol. 27, 2016, pp. 11358-11365.

[9]. D. Xiao, G. He, Z. Sun, J. Lv, P. Jin, C. Zheng, M. Liu, Microstructure, optical and electrical properties of solution-derived peroxo-zirconium oxide gate dielectrics for CMOS application, *Ceram. Int*., Vol. 42, 2016, pp. 759-766.

[10]. R. Branquinho, D. Salgueiro, L. Santos, P. Barquinha, L. Pereira, R. Martins, E. Fortunato, Aqueous combustion synthesis of aluminum oxide thin films and application as gate dielectric in GZTO solution-based TFTs, *ACS Appl. Mater. Interfaces*, Vol. 6, 2014, pp. 19592-19599.

[11]. C. Zhu, A. Liu, G. Liu, G. Jiang, Y. Meng, E. Fortunato, R. Martins, F. Shan, Low-temperature, nontoxic water-induced high-k zirconium oxide dielectrics for low-voltage, high-performance oxide thin-film transistors, *J. Mater. Chem. C*,, Vol. 4, 2016, pp. 10715-10721.

[12]. J. H. Park, Y. B. Yoo, K. H. Lee, W. S. Jang, J. Y. Oh, S. S. Chae, H. K. Baik, Low-temperature, high-performance solution-processed thin-film transistors with peroxo-zirconium oxide dielectric, *ACS Appl. Mater. Interfaces*,, Vol. 5, 2013, pp. 410-417.

[13]. C. G. Lee, A. Dodabalapur, Solution-processed zinc–tin oxide thin-film transistors with low interfacial trap density and improved performance, *Appl. Phys. Lett*., Vol. 96, 2010, 243501.

[14]. T. J. Ha, A. Dodabalapur, Photo stability of solution-processed low-voltage high mobility zinc-tin-oxide/ZrO_2 thin-film transistors for transparent display applications, *Appl. Phys. Lett*., Vol. 102, 2013, 123506.

[15]. X. R. Zhao, S. M. Wang, A. J. Li, J. O. Yang, G. D. Xia, J. Zhou, Universal solution-processed high-k amorphous oxide dielectrics for high-performance organic thin film transistors, *RSC Adv*., Vol. 4, 2014, pp. 14890-14895.

[16]. I. Oja, A. Mere, M. Krunks, R. Nisumaa, C.-H. Solterbeck, M. Es-Souni, Structural and electrical characterization of TiO_2 films grown by spray pyrolysis, *Thin Solid Films*, Vol. 515, 2006, pp. 674-677.

[17]. A. Juma, I. Oja Acik, A. T. Oluwabi, A, Mere, V. Mikli, M. Danilson, M. Krunks, Zirconium doped TiO_2 thin films deposited by chemical spray pyrolysis, *App. Surf. Sci.*, Vol. 387, 2016, pp. 539-545.

[18]. A. T. Oluwabi, A. O Juma, I. Oja Acik, A. Mere, M. Krunks, Effect of Zr doping on the structural and electrical properties of spray deposited TiO_2 thin film, *Proceedings of Estonia Academy of Science*, Vol. 67, Issue 2, 2018, pp. 147-157.

[19]. A. T. Oluwabi, I. Oja Acik, A. Katerski, A. Mere, M. Krunks, Structural and electrical characterisation of high-k ZrO_2 thin films deposited by chemical spray pyrolysis method, *Thin Solid Films*, 2018 (Submitted).

[20]. K. Banger, Y. Yamashita, K. Mori, R. Peterson, T. Leedham, J. Rickard, H. Sirringhaus., Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol–gel on chip' process, *Nat. Mater*., Vol. 10, 2011, pp. 45-50.

[21]. Y. S. Rim, H. Chen, T. B. Song, S. H. Bae, Y. Yang, Hexaaqua metal complexes for low-temperature formation of fully metal oxide thin-film transistors, *Chem. Mater*., Vol. 27, 2015, pp. 5808-5812.

[22]. W. H. Jeong, D. L. Kim, H. J. Kim, Accelerated formation of metal oxide thin film at 200 °C using oxygen supplied by a nitric acid additive and residual organic suction vacuum annealing for thin-film transistor applications, *ACS Appl. Mater. Interfaces*, Vol. 5, 2013, pp. 9051-9056.

[23]. J. Leppäniemi, K. Ojanperä, T. Kololuoma, O.-H. Huttunen, J. Dahl, M. Tuominen, P. Laukkanen, H. Majumdar, A. Alastalo, Rapid low-temperature processing of metal-oxide thin film transistors with combined far ultraviolet and thermal annealing, *Applied Physics Letters*, Vol. 105, 2014, 113514.

[24]. B. Wang, X. Yu, P. Guo, W. Huang, L. Zeng, N. Zhou, L. Chi, M. J. Bedzyk, R. P. Chang, T. J. Marks, Solution-processed all-oxide transparent high-performance transistors fabricated by spray-combustion synthesis, *Adv. Electron. Mater.*, Vol. 2, 2016, 1500427.

[25]. M. G. Kim, M. G. Kanatzidis, A. Facchetti, T. J. Marks, Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing, *Nat. Mater*., Vol. 10, 2011, pp. 382-388.

[26]. J. H. Park, J. Y. Oh, S. W. Han, T. I. Lee, H. K. Baik, Low-temperature, solution-processed ZrO_2:B thin film: A bifunctional inorganic/organic interfacial glue for flexible thin-film transistors, *ACS Appl. Mater. Interfaces*, Vol. 7, 2015, pp. 4494-4503.

[27]. Y. H. Kim, J. S. Heo, T. H. Kim, S. Park, M. H. Yoon, J. Kim, M.S. Oh, G.R. Yi, Y.Y. Noh, S. K. Park, Flexible metal-oxide devices made by room-temperature photochemical activation of sol-gel films, *Nature*, Vol. 489, 2012, pp. 128-132.

[28]. G. Reyna-Garcia, M. Garcia-Hipolota, J. Guzman-Mandoza, M. Aguilar-Frutis, C. Falcony, Electrical, optical and structural characterization of high-k dielectric ZrO_2 thin films deposited by the pyrosol technique, *Journal of Material Science: Materials in Electronics*, Vol. 15, 2004, pp. 439-446.

[29]. E. R. Santos, E. C. Burini, S. H. Wang, UV-ozone generation from modified high intensity discharge mercury vapor lamps for treatment of indium tin oxide films, *Ozone Sci. Eng*., Vol. 34, 2012, pp. 129-135.

[30]. A. V. Rudakova, M. V. Maevskaya, A. V. Emeline, D. W. Bahnemann, Light-controlled ZrO_2 surface, *Scientic Report*, Vol. 6, 2016, 34285.

[31]. U. S. Patela, K. H. Patel, K. V. Chauhan, A. K. Chawla, S. K. Rawal, Investigation of various properties for zirconium oxide films synthesised by sputterin, *Procedia Technology*, Vol. 23, 2016, pp. 336-343.

[32]. Y. Hao, D. M. Soolaman, H-Z. Yu, Controlled wetting on electrodeposited oxide thin films: From hydrophilic to superhydrophobic, *J. Phys. Chem. C*, Vol. 117, 2013, pp. 7736-7743.

[33]. I. Gromyko, M. Krunks, T. Dedova, A. Katerski, D. Klauson, I. Oja Acik, Surface properties of sprayed and electrodeposited ZnO rod layers, *Applied Surface Science*, Vol. 405, 2017, pp. 521-528.

[34]. G. Cabillo, L. Lillo, C. Caro, G. E. Buono-Core, B. Chornik, M. A. Soto, Structure and optical characterization of photochemically prepared ZrO_2 thin films doped with erbium and europium, *J. Non-Cryst. Solids*, Vol. 354, 2008, pp. 3919-3928.

[35]. N. L. Zhang, Z. T. Song, Q. Wan, Q. W. Shen, C. L. Lin, Interfacial and microstructural properties of zirconium oxide thin films prepared directly on silicon, *Appl. Surf. Sci*., Vol. 202, 2002, pp. 126-130.

[36]. K. Umeda, T. Miyasako, A. Sugiyama, A. Tanaka, M. Suzuki, E. Tokumitsu, T. Shimoda, Impact of UV/O_3 treatment on solution-processed amorphous $InGaZnO_4$ thin-film, *Journal of Applied Physics*, Vol. 113, 2013, 184509.

[37]. M. Chun, M.-J. Moon, J. Park, Y.-C. Kang, Physical and chemical investigation of substrate temperature dependence of zirconium oxide films on Si(100), *Bull. Korean Chem. Soc*., Vol. 30,, Issue 11, 2009, pp. 2729-2734.

[38]. R. Islam, G. Chen, P. Ramesh, J. Suh, N. Fuchigami, D. Lee, K. A. Littau, K. Weiner, R. T. Collins, K. C. Saraswat, Investigation of the changes in telectronic properties of Nickel oxide due to UV/ozone treatment, *Appl. Mater. Interfaces*, Vol. 9, 2017, pp. 17201-17207.

[39]. A. Kumar, S. Mondal, K. S. R. Koteswara Rao, Low temperature solution processed high-ZrO_2 gate dielectrics for nanoelectonics, *Applied Surface Science*, Vol. 370, 2016, pp. 373-379.

[40]. B. G. Son, S. Y. Je, H. J. Kim, C. K. Lee, C. K. Lee, A. Y. Hwang, J. Y. Won, J. H. Song, R. Choi, J. K. Jeong, High-performance In–Zn–O thin-film transistors with a soluble processed ZrO_2 gate insulator, *Phys. Status Solidi (RRL)*, Vol. 7, 2013, pp. 485-488.

[41]. S.-Y. Lee, H. Kim, P. C. Mclntyre, K. C. Saraswat, J.-S. Byun, Atomic layer deposition of ZrO_2 on W for metal-insulator-metal capacitor application, *Appl. Phys. Lett.*, Vol. 82, 2003, 2874.

[42]. C. Fu-Chien, A review on conduction mechanisms in dielectric films, *Advances in Materials Science and Engineering*, Vol. 2014, 2014, 578168.

[43]. E. Carlos, R. Branquinho, A. Kiazadeh, P. Barquinha, R. Martins, E. Fortunato, UV-mediated photochemical treatment for low-temperature oxide based thin film transistor, *Applied Material and Interface*, Vol. 8, Issue 45, 2016, pp. 31100-31108.

(034)

Design, Implementation and Performance Evaluation of Wireless Sensor Networks for Data Acquisition System (A Case Study of Smart Homes)

S. Abba and I. M. Nyam
Abubakar Tafawa Balewa University (Federal University of Technology),
ATBU, Yelwa Campus Dass Road, P.M.B. 0248, Bauchi State, Nigeria
Tel.: + 234 0811 9717 843
E-mail: saniabba2004@gmail.com

Summary: This research paper presents the performance evaluation of wireless sensor networks (WSN) for data acquisition system (DAQ). The research work considers three important parameters for performance evaluations. These are temperature, humidity and light. Proteus and Arduino integrated design environment (IDE) were used to build a complete WSN system. A real working prototype was designed and implemented. Experimental procedure includes building the hardware architecture of the transmitting nodes, modeling both the communication channels and the receiving master node. A digital-output relative humidity and temperature (DHT22) and light dependent resistor (LDR) sensors were used for the data acquisition system. The values of the sensed parameters are stored on an SD card mounted on the Arduino board which served as the base station. Experimental (case study) results are obtained from the implemented prototype by taking the readings of the sensors stored on the SD card under various conditions and numerous results were collected to demonstrate the efficiency and flexibility of the proposed approach. The proposed approach will assist the smart-home owners to be kept abreast of their environmental condition and equally know what changes would likely to happen. The implemented prototype can be deployed in smart-homes, remote monitoring and healthcare applications.

Keywords: Wireless sensor network (WSN), Data acquisition (DAQ), Performance evaluation, Smart homes, Light dependent resistor (LDR) sensor, Digital-output relative humidity, Temperature DHT22 sensor.

1. Introduction

This research work considers the performance evaluation of wireless sensor network for data acquisition system, which has three parameters namely, Temperature, Humidity and Light. The readings of these parameters are stored as a text file in a media memory card (SD Card) and real time clock will display date and time those parameters are sensed. The sensors with such capabilities are DHT22 and Light Dependent Resistor (LDR) sensors. DHT22 sensor senses both temperature and humidity while light dependent resistor sensor senses light. These components are soldered on a Vero Board together with other digital components that made up the circuit. The fabricated device is powered by battery to enable the sensors to work perfectly.

The data acquisition systems have emerged over some years from electromechanical recorders with few channels to electronic devices possessing the capabilities of measuring hundreds of parameters simultaneously. The most commonly used data acquisition systems make use of magnetic tape and recorders to record the signals. However, with the advent of new technology, the amount of data and the speed and time of collection increases dramatically. Therefore, there is the need to have sophisticated device that can measure environmental parameters in real-time for making an informed decision. The computer based data acquisition system should possess the capabilities of recording extremely accurate, repeatable, and reliable and error free data according to the design specifications and consideration [1].

In order to achieve these design specifications and considerations, the data acquisition system should include: selecting the correct sensors for the target application; the choice of proper wire and shielded cable; signal capturing in proper magnitude; signal and frequency ranging; proper grounding and shielding to avoid loops. In addition, the choice of correct impedance and double ended differential inputs. The smart environment in which the device will be used should also be considered, especially for extremes of ambient temperature, humidity and light Lumina. Therefore, the major goal of this research paper is to notify the smart home users of the changes in the environmental parameters for informed decision making and the most needed recommended practices for smart cities [2].

The state of the art sensor fusion technique in embedded mobile devices is presented by the authors in [3]. The approach is aimed to assist the mobile device users to identify their daily activities using mobile phones. The sensor fusion techniques are used to aggregate data collected from several sensors to enhance reliability in identifying different activities of the mobile phone users. In this regards, the mobile devices to monitor the user's activities have certain drawbacks, these include: low memory, low battery life and low processing capabilities. And this affects most sensor fusion techniques.

A static calibration and analysis of the Velodyne HDL-64E S2 scanning LiDAR system was

demonstrated by the author's work in [4]. The work provided a mathematical model for measurements of the HDL-64E S2 scanner. In order to provide an optimal solution for the laser's internal calibration parameters, a planar feature based least squares adjustment method was demonstrated in a minimally constrained network. The proposed approach, provided a three-fold enhancement in the planar misclosure residual over the standard factory calibration model.

The study of parameter selection for data sampling frequency and segmentation techniques and their effect on classification accuracy was presented. The research work presented the empirical investigation of different data sampling rates, segmentation techniques and segmentation window sizes and how they affect the accuracy of activity of daily living event classification and computational load for two different accelerometer sensor datasets [5].

Advances in heterogeneous communication technologies have enabled sensors to be used in smart cities, things or objects interact with each other while ensuring good network connectivity. However, the existing technologies cannot provide an efficient data acquisition mechanism for flawless and error prone connectivity in smart cities due to the presence of many sensing devices which generates several problems [6-8].

A low-cost microcontroller-based data acquisition device was provided by the authors in [9]. The design consists of a configurable microcontroller-based device with an embedded universal serial bus (USB) transceiver and a 12-bit analogue-to-digital converter. The embedded DAQ device, is preloaded with a firmware program that allows easy data acquisition and generation of analogue and digital signals. It also has the capabilities of data transfer between the device and the application program running on a personal computer through the use of universal serial bus.

The monitoring of cultural heritage in the context of smart cities was demonstrated [10]. The idea is to perform future comparative studies and upload the gathered information into the cloud that will be useful for the conservation of other heritage sites.

The study of the side effect of heterogeneous DAQ hardware was carried out [11]. The major challenge is the lack of an accurate synchronization between samples captured by each device. A low-cost hardware modular DAQ architecture consisting of a baseboard and a set of substitutable modules was presented. However, the system is not efficient enough to solve the presence DAQ requirement. Therefore, a design, implementation and performance evaluation of wireless sensor networks for data acquisition system is very essential.

The fundamental objectives of this proposed design are: time saving; no connection of sensor nodes through wires; inexpensive; quick access to data; accuracy; reliability; data integrity, flexibility, and ease of deployment.

This paper will be of immense importance not just to those who use wireless sensor networks for data acquisition (smart home owners) but also to those who in one way or the other, the result will play a key role in their livelihood. The implemented prototype will go a long way in making a performance evaluation of data acquisition system through wireless sensor networks for monitoring temperature, humidity and light in smart homes much easier.

The rest of the paper is organized as follows: Section 2 presents related literature; Section 3 discusses system architecture and design methodology; Section 4 discusses experimental results and case study; Section 5 provides concluding remarks and plans for future enhancements.

2. Related Work

The work of the authors in [1] discusses the state-of-the-art sensor fusion technique in embedded mobile devices. This approach was aimed to assist the mobile device users to identify their daily activities using mobile phones. The sensor fusion techniques are used to aggregate data collected from several sensors to enhance reliability in identifying different activities of the mobile phone users. Though, the mobile devices to monitor the user's activities have certain drawbacks, these include: low memory, low battery life and low processing capabilities. And this affects most sensor fusion techniques. The author's objective is to present an overview of the state of the art to identify instances of sensor data fusion techniques that are used in mobile devices to track the daily activities of mobile phone users.

In the research work by the authors in [2], a static calibration and analysis of the Velodyne HDL-64E S2 scanning LiDAR system was demonstrated. The work provided a mathematical model for measurements of the HDL-64E S2 scanner. In order to provide an optimal solution for the laser's internal calibration parameters, a planar feature based least squares adjustment method was demonstrated in a minimally constrained network. The work provided the results of the adjustment along with a detailed evaluation of the adjustment residuals. The proposed approach, provided a threefold enhancement in the planar misclosure residual RMSE over the standard factory calibration model. Furthermore, the measurements from the scanner indicated that unmodelled distortions may still be existed in the range measurement. Nevertheless, despite the presence of measurement distortions in the measurements, the whole precision of the adjusted laser scanner data proved to be a practical choice for high accuracy mobile scanning applications.

The authors in [3] study the parameter selection for data sampling frequency and segmentation techniques and their effect on classification accuracy. The authors presented the empirical investigation of different data sampling rates, segmentation techniques and segmentation window sizes and how they affect the accuracy of activity of daily living event classification and computational load for two different accelerometer sensor datasets. The authors presented

results and recommendations for the choice of the best combination of parameters that are identified based on the equivalent Pareto curve.

The work of the authors in [4] presented a low-cost microcontroller-based data acquisition device. The major components of the device consist of a configurable microcontroller-based device with an embedded USB transceiver and a 12-bit analogue-to-digital converter. The embedded DAQ device, is preloaded with a firmware program that allows easy data acquisition and generation of analogue and digital signals. It also has the capabilities of data transfer between the device and the application program running on a personal computer through the use of universal serial bus. Furthermore, the authors developed the LabVIEW drivers for the fabricated device.

The authors in [5] propose monitoring of cultural heritage in the context of smart cities. The idea is to perform future comparative studies and upload the gathered information into the cloud that will be useful for the conservation of other heritage sites. The authors presented the development of an economical and appropriate data acquisition system which integrate wired and wireless communication, and third party hardware tools for increased versatility of the designed system. The proposed device provided the capability of monitoring a complex network of points with high sampling frequency. The device used a wired sensor in a 1-wire bus and a wireless centralized data recording system and monitoring of physical parameters. Furthermore, it is envisaged that the device will possesses the future capability of attaching an alarm system or sending data over the Internet. The development of three board design and over five thousand algorithm lines of codes, demonstrated the efficiency of the proposed system.

The work of the authors in [6], study the side effect of heterogeneous DAQ hardware. The major problem is the lack of an accurate synchronization between samples captured by each device. In order to provide a solution to this problem, the authors proposed a low-cost hardware modular DAQ architecture consisting of a baseboard and a set of substitutable modules. The main objective is the ability to sample all data sources at predictable, fixed sampling frequencies, with a reduced synchronization mismatch of less than one second between heterogeneous signal sources. Experimental results were presented, demonstrating vibration spectrum analyses from piezoelectric accelerometers and a spectrum of quadrature encoder signals. Other approaches are given by the work of the respective authors in the literature [12-17].

3. System Architecture and Design

Fig. 1 illustrates the block diagram of the real-time device monitoring system. Once connection is established, the DHT22 and a light dependent resistor (LDR) sensors will verify the established connection and start reading the temperature, humidity and light Lumina, and the readings or information is displayed by the LCD through the user interface window. Then, a real-time clock (RTC) module is accessed through I2C interface to obtain the current time and date. The SD card is accessed via SPI interface and a new data log file is created. If the file already exist, new data will be written with its new date and time stamp beneath the existed data inside the file. The two sensors will automatically start taking measurement on the indicated parameters temperature, humidity and light [15-18].

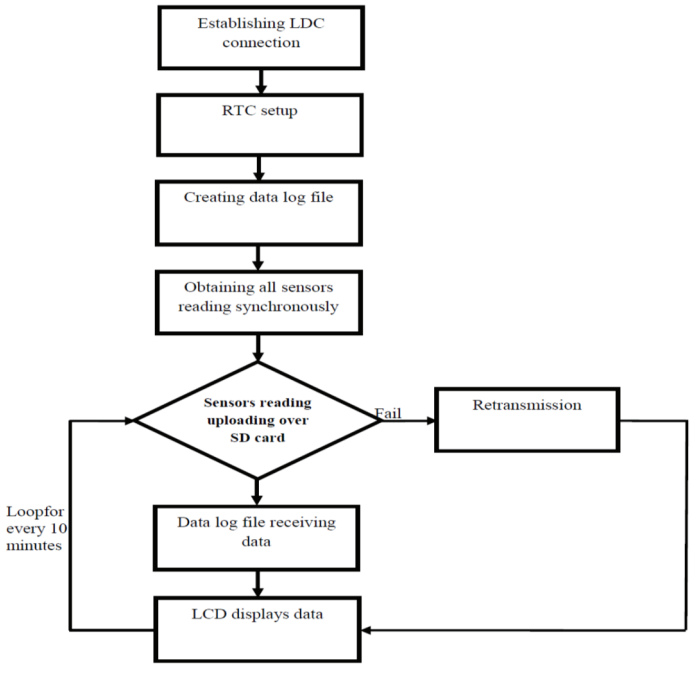


Fig. 1. Real time device monitoring system flow.

Fig. 2 shows the system architecture. The architecture consists of three inputs and two outputs. All electronics operations are controlled by a single microcontroller unit, which is programmed based on how other peripherals components of the system will behave.

This device, consists of two sensors; temperature and humidity (integrated into a single module), and Light (LDR). The temperature and humidity sensors are responsible to detect ambient changes.

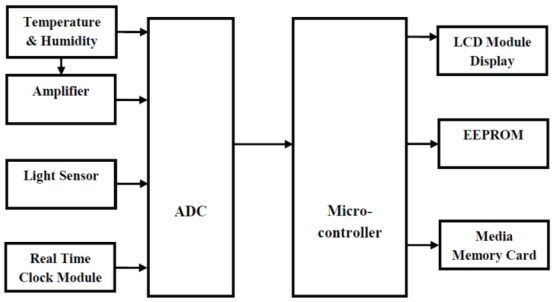


Fig. 2. System Architecture.

The Light sensor is used to detect the Lumina (brightness) of light. The sensor's data readings are registered in the microcontroller unit along with date and time stamp synchronously. The data is then be uploaded over into the data log file monitoring database to provide the smart home users with the real time data.

Fig. 3 illustrates the fabricated device prototype. The casing fabrication was done with plastic, and carefully engineered. The casing is portable like a small box which can be hand held and can be carried about easily [19-23].

4. Experimental Results (Case Study)

Fig. 4 illustrates the temperature sensor readings against time of a smart home as a case study. There are three scenarios namely, morning, afternoon and night as indicated in the figure. And each scenario is boarded with a vertical gold, black and thick red dotted lines for easy understanding.



Fig. 3. The fabricated device prototype.

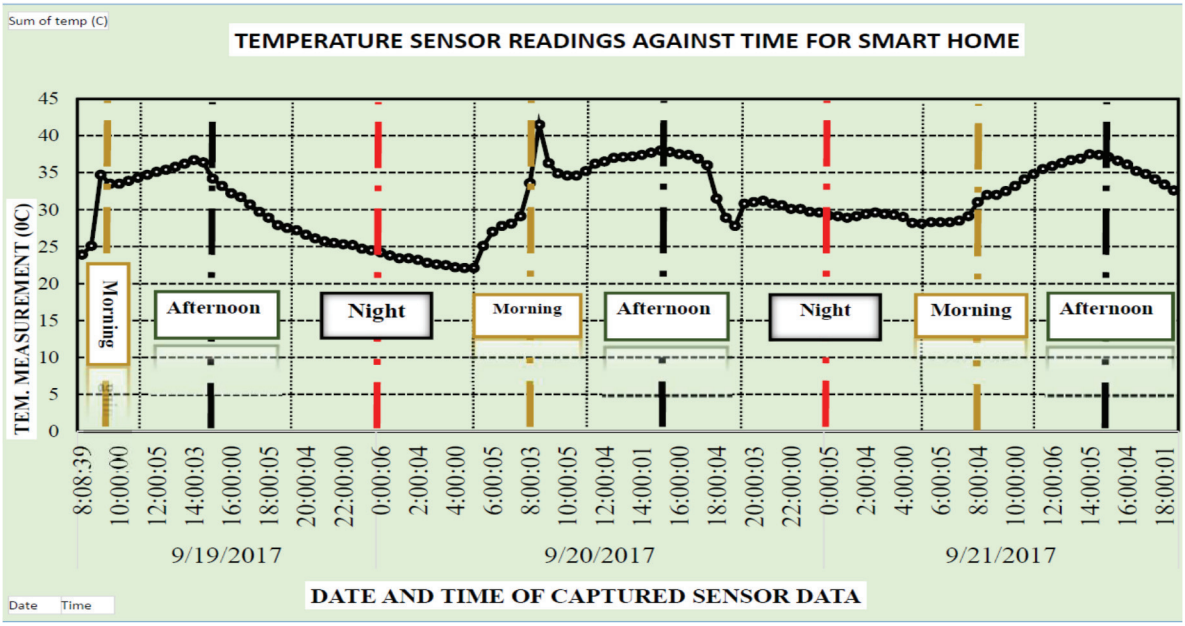


Fig. 4. Temperature sensor readings against time for smart home.

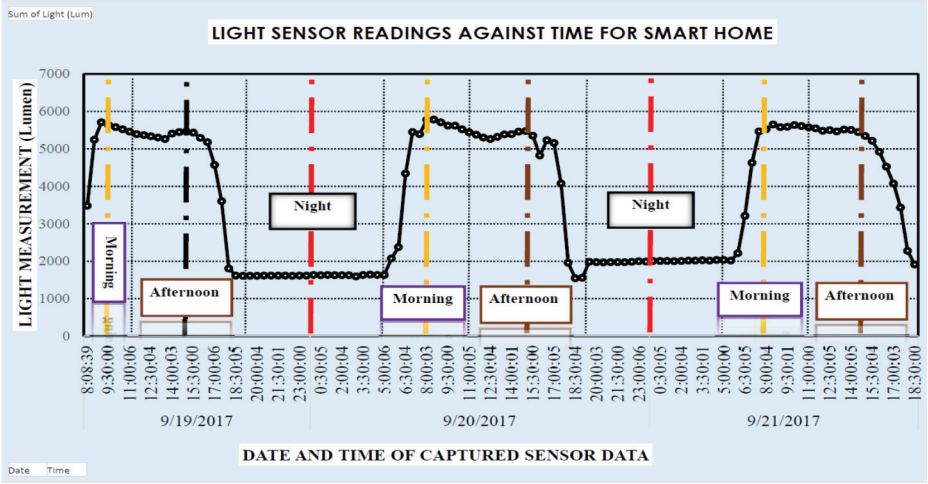


Fig. 5. Light sensor readings against time for smart home.

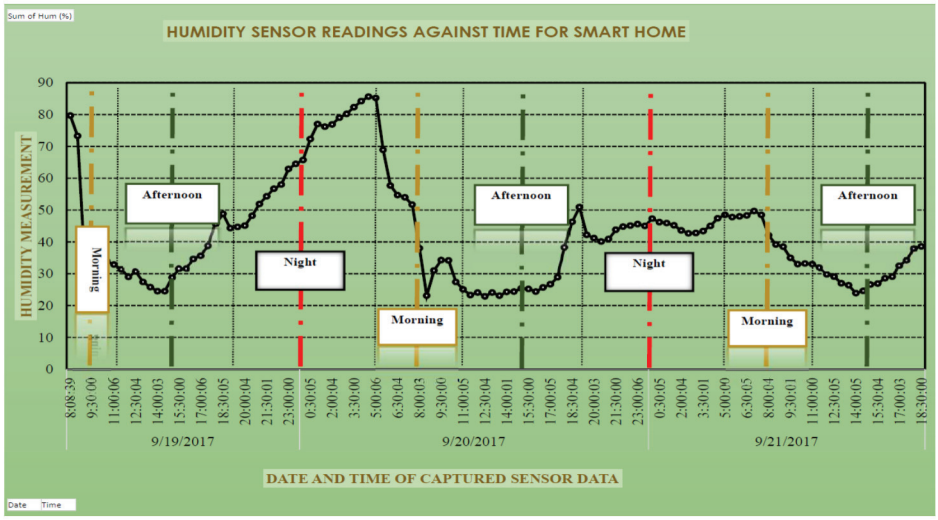


Fig. 6. Humidity sensor readings against time for smart home.

The temperature reading samples were taken once for every 30 minutes. The measurements ran for over 104 samples, and the device had been running for 52 hours and 30 minutes continuously. The temperature reading shows 37 ˚C max and 25 ˚C min, while the temperature during the morning of the first day, obviously dropped by 12 ˚C, and constantly swings between 27 ˚C and 37 ˚C during the morning and drastically dropped during the night.

Fig. 5 shows the light sensing result that is the light Lumina. As can be observed, the light senor's reading is very high during the daylight (morning) and very low at night. During the daytime, the Lumina varies depending on the atmospheric weather condition either cloudy or sunny. This variation ranges between 3480 to 5710 Lumina, and we can observe a significant drop in the light sensor's reading, especially at sunsets (night) to be between 1609 to 1999 Lumina. However, we can observe that where the Lumina reading goes low during the daytime, it shows that the doors and the windows of the smart home were closed/locked by the owners. Similarly, where the Lumina reading goes up during the night time, it is an indication that there was a light flashing either from electric bulb or nearby automobile cars.

Fig. 6 illustrates the humidity sensor readings for smart homes. As can be observed, the humidity readings are higher during the night most especially the day that it rained and lower during a normal day. It can be observed that during the night, the humidity sensor measurements varies in the ranges of 44 to 85. However, humidity measurements dropped to 22 and varies in the ranges of 22 to 85.

These results demonstrate the efficiency and reliability of the fabricated device prototype and its application to smart homes. The device will be of immense importance to the smart home owners to be kept abreast of their environmental condition and equally know what changes are likely to happen and when. The performance of the proposed system is reliable in terms of captured data, speed, accuracy, integrity and capacity in its storage as demonstrated in the experimental results. The fabricated device

prototype can be deployed to smart homes, remote monitoring and healthcare applications.

5. Conclusion and Future Work

This research paper used the capabilities of two sensors with three parameters for the data acquisition system. The sensors include: DHT22 used for measuring temperature and humidity, and a light dependent resistor (LDR) used for measuring light Lumina. The real time clock (RTC) module was used for capturing date and time stamp of the sensed parameters to record their actual readings. The media memory card (MMC) was used as the main base station for the storage of the sensor readings. The methodology used in this paper is the rigorous performance analysis of the data stored on SD Card (base station). The recording of the sensor's measurement into the SD card was done in the interval of 30 minutes. The sensor's reading stored on the SD card with date and time stamped for the three parameters are used to plot the graphs of the three parameters versus time. This approach will helps the smart-home owners to be kept abreast of their environmental condition and equally know what changes are likely to happen and when. The performance of the system is reliable in terms of captured data, speed, accuracy, integrity and capacity in its storage. Experimental results of the fabricated (device) prototype, demonstrates the efficiency and reliability of the proposed approach. Overall, the system can be deployed in smart homes, remote monitoring and healthcare applications.

The future work will considers the integration of a WiFi module to enable transmission, visualization and storage of sensor data over the internet. Smart home users can access the information regarding their environment from remote locations.

Acknowledgements

Special thanks are owed to Dr. Maria Liz Crespo of the Abdussalam International Centre for Theoretical Physics (ICTP), Trieste, Italy and Dr. Iain Darby of the International Atomic Energy Agency (IAEA), Vienna, Austria, for the ICTP workshop / seminar smr 3143, "Joint ICTP-IAEA School on Zynq-7000 SoC and its Applications for Nuclear and Related Instrumentation", August – September, 2017, Trieste, Italy.

References

[1]. Measurement computing corporation, in Data Acquisition Hand Book: A Reference for DAQ and Analog and Digital Signal Conditioning, 3rd Edition, *Measurement Computing Corporation*, 2012, pp. 946-5100.

[2]. I. Yaqoob, I. A. T. Hashem, Y. Mehmood, A. Gani, S. Mokhtar, S. Guizani, Enabling communication technologies for smart cities, *IEEE Communications Magazine*, January 2017, Vol. 55, Issue 1, 2017, pp. 114-122.

[3]. M. P. Ivan, M. G. Nuno, N. Pombo, F. Flórez-Revuelta, From data acquisition to data fusion: A comprehensive review and a roadmap for the identification of activities of daily living using mobile devices, *Sensors*, Vol. 16, Issue 184, 2016, pp. 2-27.

[4]. C. Glennie, D. D. Lichti, Static calibration and analysis of the velodyne HDL-64E S2 for high accuracy mobile scanning, *Remote Sensing,* Vol. 2, 2010, pp. 1610-1624.

[5]. D. B. Sebastian, D. Azzi, R. Khusainov, I. E. Achumba, J. Ries, Sensor data acquisition and processing parameters for human activity classification, *Sensors,* Vol. 14, 2014, pp. 4241-4270.

[6]. R. Fernandes, *et al*., Flexible Wireless Sensor Network for smart lighting applications, in *Proceedings of the IEEE Int. Conference Instrumentation and Measurement Technology (I2MTC'14)*, 2014, pp. 434–39.

[7]. D. I. Tapia,, J. B. Rodridguez, J. M. Corchado, O. Garcia, Wireless Sensor Networks for data acquisition and information fusion: A case study, in *Proceedings of the 13th International Conference on Information Fusion (FUSION'10)*, 2010, pp. 1-8.

[8]. R. R. Brooks, Wireless Sensor Networks: Architecture and protocols, *International Journal of Distributed Sensor Networks,* Vol. 4, Issue 3, 2008, p. 286.

[9]. D. Hercog, B. Gergič, A flexible microcontroller-based data acquisition device, *Sensors*, Vol. 14, 2014, pp. 9755-9775.

[10]. G. D. Fernando-Juan, B. Esteban, P. Merello, Design of a hybrid (wired/wireless) acquisition data system for monitoring of cultural heritage physical parameters in smart cities, *Sensors,* Vol. 15, 2015, pp. 7246-7266.

[11]. J. L. Blanco-Claraco, J. López-Martínez, J. L. Torres-Moreno, A. Giménez-Fernández, A low-cost modular platform for heterogeneous data acquisition with accurate interchannel synchronization, *Sensors*, Vol. 15, 2015, pp. 27374-27392.

[12]. N. Ling, D. Mei-Xia, Design of a remote data monitoring system based on sensor network, *International Journal of Smart Home,* Vol. 9, Issue 5, 2015, pp. 23-30.

[13]. H. Chen, L. Cui, C. Huang, H. Zhu, EasiSim: A scalable simulator for Wireless Sensor Networks, *Wireless Sensor Network,* Vol. 1, Issue *5*, 2009, pp. 467-474.

[14]. D. Yan, Z. Dan, ZigBee-based Smart Home system design, in *Proceedings of the 3rd International Conference on Advanced Computer Theory and Engineering (ICACTE'10),* 2010, pp. V2-650-V2-653.

[15]. 1. M. Xu, L. Ma, X. Feng, L. M. Shao, Design and Implementation of a Wireless Sensor Network for Smart Homes, https://www.researchgate.net/publication/47796829_Design_and_Implementation_of_a_Wireless_Sensor_Network_for_Smart_Homes

[16]. M. Moghavvemi, S. Tan, A reliable and economically feasible remote sensing system for temperature and relative humidity measurement, *Sensors and Actuators A: Physical,* Vol. 117, 2005, pp. 181-185.

[17]. K. Montgomery, K. Chiang, A new paradigm for integrated environmental monitoring, *ACM International Conference Proceeding Series*, 2010.

[18]. S. Abba, J. Lee, FPGA-based design of an intelligent on-chip sensor network monitoring and control using

dynamically reconfigurable autonomous sensor agents, *Int. Journal of Distributed Sensor Networks*, Vol. 2016, 2016, 4246596.

[19]. G. Lehmann, A. Rieger, M. Blumendorf, S. Albayrak, A 3-Layer architecture for smart environment models, in *Proceedings of the 8th IEEE International Conference on Pervasive Computing and Communications Workshops (PERCOM'10)*, 2010, pp. 636-641.

[20]. C. Andrew, Internet of things (IoT) design considerations for embedded connected devices, in White Paper, Embedded Software, TECH12120-w MGC 05-14, *Mentor Graphics Corporation*, 2014, pp. 1-6.

[21]. Jose Miguel Pereira, Octavian Adrian Postolache and Pedro Silva Girao, Analog to digital conversion methods for smart sensing systems, *Advances in Measurement Systems*, 2010, pp. 576-592.

[22]. S. Abba, J. Lee, An autonomous self-aware and adaptive fault tolerant routing technique for Wireless Sensor Networks, *Sensors,*, Vol. 15, 2015, pp. 20316-20354.

[23]. M. T. Lazarescu, Design and field test of a WSN platform prototype for long-term environmental monitoring, *Sensors*, Vol. 15, Issue 4, 2015, pp. 9481-9518.

(035)

Fabrication and Characterization of SAW Resonators Based on Sputtered AlScN Thin Films with High Sc Content

A. Ding [1], M. Reusch [1], Y. Lu [1], N. Kurz [2], T. Christoph [1], V. Lebedev [1], L. Kirste [1], R. Driad [1], A. Žukauskaitė [1] and O. Ambacher [1,3]

[1] Fraunhofer Institute for Applied Solid State Physics IAF, Tullastraße 72, 79108 Freiburg, Germany
[2] Laboratory for Compound Semiconductor Microsystems, Department of Microsystems Engineering IMTEK, University of Freiburg, Georges-Koehler-Allee 103, 79110 Freiburg, Germany
[3] Laboratory for power electronics, Department of Sustainable Systems Engineering INATECH, University of Freiburg, Emmy-Noether-Straße 2, 79110 Freiburg, Germany

Surface acoustic wave (SAW) devices have been successfully used in communication systems as well as physical or chemical sensors. However, ever-increasing demands for volume data processing and sensitivity in electronic and sensing systems require an increase of the operating frequency of SAWs [1]. Such an increase can be achieved by using interdigitated transducers (IDTs) with a finer period, and/or high acoustic velocity materials [2].

Among available piezoelectric materials, aluminum nitride (AlN) has been particularly attractive for SAW applications because of its good electrical, mechanical, and thermal properties, along with relatively high acoustic velocity and compatibility with complementary metal-oxide-semiconductor (CMOS) technology [3]. However, the electromechanical coupling of AlN based SAW devices is relatively low and this limits the possibilities to use AlN-based radio frequency microelectromechanical systems (RF-MEMS) for next generation mobile communications. In recent years, aluminum scandium nitride (AlScN) thin films have attracted much attention because of significantly increased piezoelectric constants compared to pure AlN [4, 5], resulting in higher coupling coefficient [5]. However, with increasing Sc concentration the material becomes softer, leading to decreasing acoustic phase velocity. Therefore, an optimal Sc concentration has to be found for achieving both high electromechanical coupling and high resonant frequencies simultaneously.

To address this issue, the performance of AlScN-based SAW resonators with relatively high Sc content is of particular interest.

In our work, we developed high quality $Al_{1-x}Sc_xN$ (x = 0, 0.32) thin films and evaluated their integration into high frequency $Al_{1-x}Sc_xN$/Si SAW resonators. $Al_{1-x}Sc_xN$(0001) thin films with thicknesses of ~1 µm were sputter-deposited on 4" Si(001) substrates using reactive pulsed DC magnetron co-sputtering. Before deposition, the chamber was evacuated to $< 5 \times 10^{-6}$ Pa. The optimized $Al_{1-x}Sc_xN$ sputtering process was then conducted in Ar/N_2 gas mixture at a combined power P(Al) + P(Sc) of 1000 W at heater temperature of 500 °C resulting in a deposition rate of ~0.14 nm/s [6]. X-ray diffraction (XRD) 2θ/θ scans and 00.2 reflection rocking curve (ω-scan) measurements were performed to evaluate the crystalline quality of the films. As is evident from the XRD 2θ/θ scans (Fig. 1), $Al_{0.68}Sc_{0.32}N$ films are c-axis oriented, and ~1.5° full width at half maximum (FWHM) of 0002 peak rocking curve indicates high crystalline quality of the material.

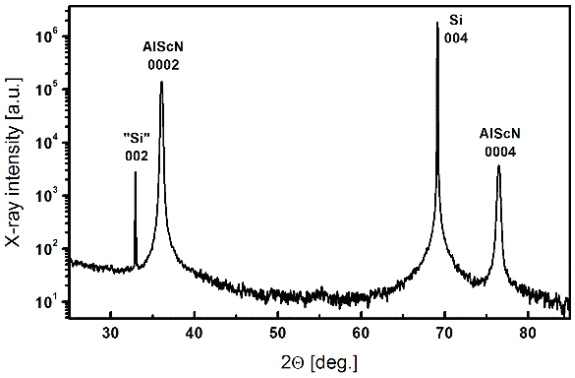


Fig. 1. X-ray diffraction 2θ/θ scans of the AlScN on Si(001).

Film surface and cross-section morphology was investigated using scanning electron microscopy (SEM). The films have dense and well-ordered columnar microstructure typical for sputtered material and a homogeneous pebble-like surface. Atomic force microscopy (AFM) measurements (Fig. 2) revealed very smooth surface with root-mean square (RMS) roughness below 2 nm.

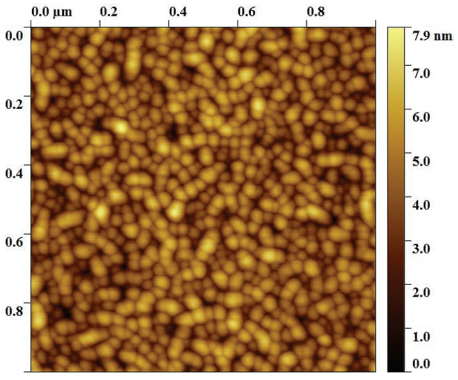


Fig. 2. Atomic force microscopy image of an AlScN film.

To evaluate the potential of these films, high frequency SAW resonators were realized on Al1-xScxN/Si using various IDT and reflector designs (Fig. 3). The process technology was designed around standard fabrication procedures, using stepper lithography and lift-off techniques, suitable for reproducible high yield manufacturing of highly uniform devices.

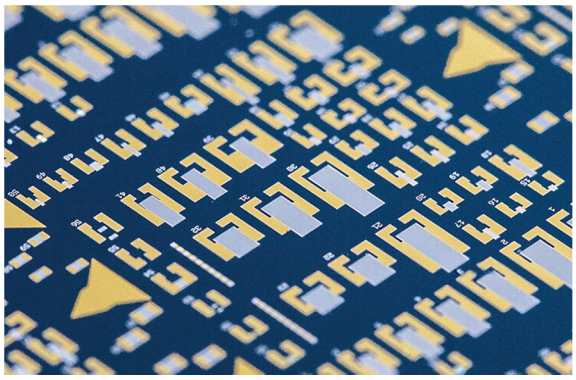


Fig. 3. Optical image of fabricated AlScN/Si devices.

The frequency response of the fabricated resonators was characterized using Agilent E5061B vector network analyzer. The experimentally determined phase velocity dispersion curve in $Al_{0.68}Sc_{0.32}N$ closely matches the theoretical predictions and confirms the high quality of our material. As shown in Fig. 4, $Al_{0.68}Sc_{0.32}N$/Si device exhibited a center frequency of 1.83 GHz, yielding a SAW acoustic phase velocity of 3650 m/s.

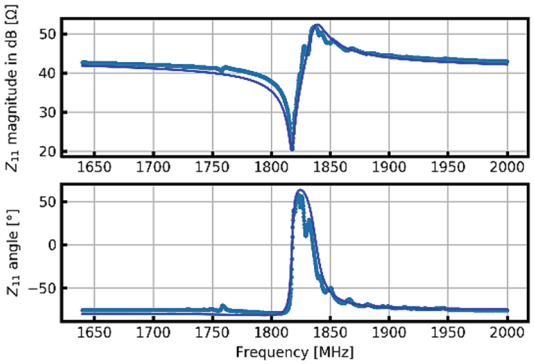


Fig. 4. Frequency response of an AlScN/Si device.

References

[1]. C. Campbell, Surface Acoustic Wave Devices for Mobile and Wireless Communications, *Academic Press*, 1998.

[2]. V. Cimalla, et al., Nanoelectromechanical devices for sensing applications, *Sensors and Actuators B: Chemical*, Vol. 126, Issue 1, 2007, pp. 24-34.

[3]. T. Palacios, et al., Nanotechnology for SAW devices on AlN epilayers, *Materials Science and Engineering: B*, Vol. 93, Issues 1-3, 2002, pp. 154-158.

[4]. M. Akiyama, et al., Enhancement of piezoelectric response in scandium aluminum nitride alloy thin films prepared by dual reactive cosputtering, *Advanced Materials*, Vol. 21, Issue 5, 2009, pp. 593-596.

[5]. G. Wingqvist, et al., Increased electromechanical coupling in w− Sc x Al 1− x N, *Applied Physics Letters*, Vol. 97, Issue 11, 2010, 112902.

[6]. Y. Lu, et al., Surface morphology and microstructure of pulsed DC magnetron sputtered piezoelectric AlN and AlScN thin films, *Physica Status Solidi (A)*, Vol. 215, 2017, 1700559.

(036)

140 mV-Startup Boost Converter for Thermal Energy Harvesting System

Hong-Yi Huang [1], Chun-Lian Chen [1], Jin-Sheng Chen [1], Chun Yi [1] and Kuo-Hsing Cheng [2]
[1] Department of Electrical Engineering, National Taipei University, Taiwan
[2] Department of Electrical Engineering, National Central University, Taiwan
Tel.: + 886-2-86741111, fax: + 886-2-26736500
E-mail: hyhuang@mail.ntpu.edu.tw

Summary: This work presents an ultra-low startup voltage boost converter for thermal energy harvesting. The proposed architecture is composed of an LC-tank oscillator, a 3-stage charge pump and a DC to DC boost converter. A test chip is implemented in a 0.18 µm CMOS technology. The acceptable input voltage range is from 140 mV to 230 mV. The output produces regulated 1.2 V and supplies 120 uA current for charging NiMH battery. The conversion efficiency is 30 % at minimum input voltage of 140 mV. A maximum efficiency of 60 % can be successfully performed. By incorporating the boost converter and a thermoelectric generator (TEG), a miniaturized module is demonstrated for energy harvesting applications.

Keywords: Boost converter, Conversion efficiency, Energy harvesting, Charge pump, Thermoelectric generator.

1. Introduction

The thermal energy is one of the important energy sources for portable and biomedical applications. The miniaturized thermoelectric generator (TEG) devices have been successfully fabricated for small-scale energy harvesting systems which convert minimal thermal energy from human body and environment gradient or heat flow. The TEG produces a very low dc output voltage which may not be suitable for operation of typical IC. This work intends to implement a dc to dc converter that receives ultra-low input voltage and produces a regulated output voltage for charging a NiMH battery for storing energy.

2. Architecture and Circuit Design

Fig. 1 shows the block diagram of the energy harvesting system consisting of six function blocks. In order to receive a minimum dc input voltage, an LC-tank oscillator is adopted as the input stage. As the input dc voltage exceeds the minimum operational voltage of the LC-tank oscillator, an ac output with enhanced amplitude can be transformed. A charge pump is applied to converts a lower dc input to a higher dc output that is sufficient to enable the boost converter. A duty cycle control is able to produce a clock whose duty cycle is 75 % so that the boost converter can ideally produce a dc output that is several times of the input voltage. At last, the charge control circuit supplying a fixed output voltage 1.2 V and output current 120 µ A to NiMH battery for storing energy.

2.1. All Native Differential Drive Charge Pump

Fig. 2 depicts the proposed charge pump adopting all native NMOS device other than NMOS or PMOS, making it suitable for operating at ultra-low voltage. The differential drive charge pump can operate in full cycle of control signal and reduces threshold voltage drop. The conversion efficiency can be higher as well. In addition, the accumulation-mode MOS varactor which has higher capacitance per unit area at low voltage than MiM capacitor is applied. The chip area can be reduced as well as the cost.

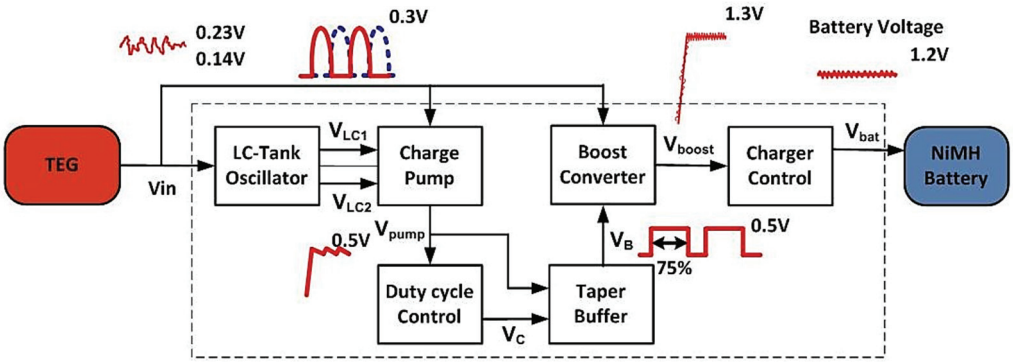


Fig. 1. Block diagram of energy harvesting system.

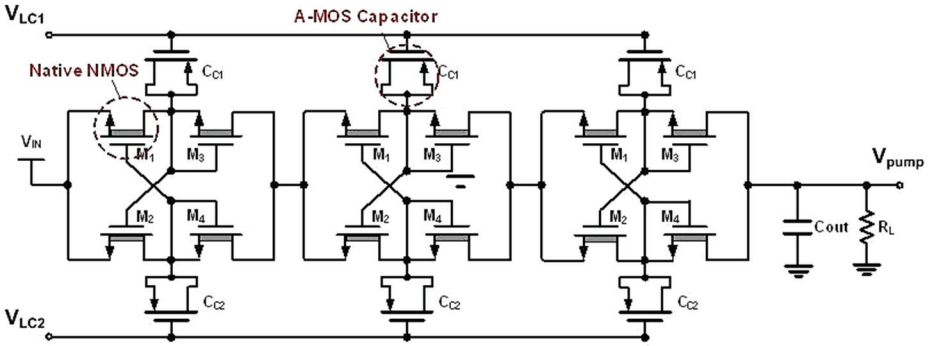


Fig. 2. All native differential drive charge pump.

2.2. Duty Cycle Control

The boost converter requires a sufficient supply voltage from the charge pump that is higher than the device threshold voltage for the control signal so as to switch the power MOS effectively. A ring oscillator implemented by odd stage of bulk-driven CMOS inverters receives supply voltage from the charge pump. An optimum efficiency of the energy harvesting system depends on the oscillator frequency. A higher frequency can provide a larger output power on the sacrifice of higher dynamic power. Fig. 3 illustrates a combined logic circuit consisting of a D Flip-Flop, a NAND gate implemented by transmission gates to produce an output frequency that is divided-by-2 with a duty cycle of 75 %.

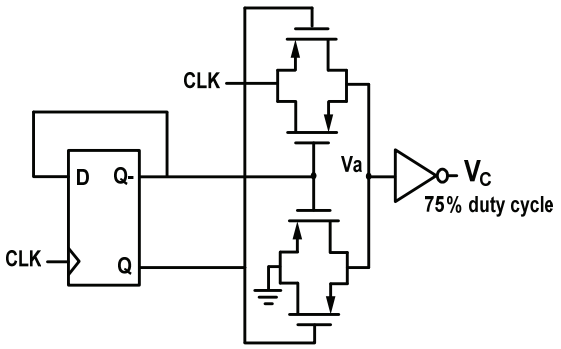


Fig. 3. 75 % duty cycle control.

2.3. Improved Boost Converter

Increasing the stage number of the differential charge pump can help to enhance the output voltage. However, the efficiency may decrease due to dynamic power consumption by the parasitic capacitances of the complicated circuit. Fig. 4 shows the improved boost converter that is employed as the main boost circuit. The 75 % duty cycle clock can ideally boost the output voltage by several times. A diode-connected NMOS M_3 connects the drain and bulk of the power MOS M_2. Then the source-bulk voltage V_{SB2} of M_2 is negative that lowers the threshold voltage. Accordingly, the efficiency can be improved.

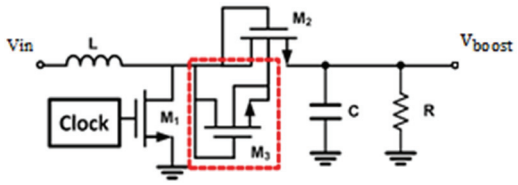


Fig. 4. Improved boost converter.

2.4. Charge Control

Fig. 5 shows the charge control with a fixed output voltage 1.2 V and supplies a constant current 120 uA for avoiding overcharge of the battery. A bandgap voltage produces a process, supply voltage and temperature insensitive voltage that is 1.2 V. A constant-gm current is applied for supplying a current source that is independent on supply voltage.

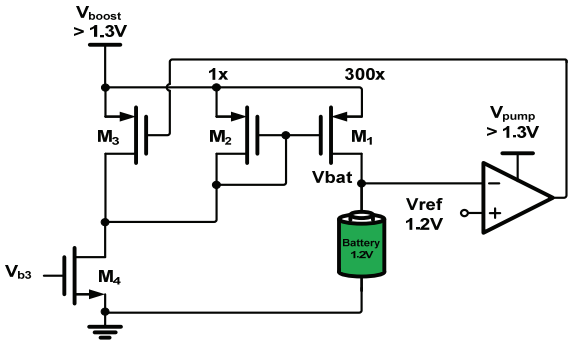


Fig. 5. Charge Control.

3. Circuit Layout and Measurement

Fig. 6 shows the test chip layout that is implemented in a 0.18 um CMOS process. Fig. 7 depicts the measurement of the control output that receives a minimum input of 140 mV and produce constant 1.2 V output. The acceptable maximum input voltage is 230 mV that produces a successful output. Table 1 summarizes the measurement results. It is observed that the proposed harvesting system can receive a lower input voltage. The conversion efficiency is better than ref [9] based upon the comparison of a similar input and output specification.

Table 1. Comparison table.

Parameters	[1]	[2]	[3]	This work 0.18-um CMOS
Min. Vin	0.18V	0.15V	0.10V	0.14V
Output Voltage	0.74V @Vin=0.12V	0.619V @Vin=0.18V	1.2V @Vin=0.12V	1.3V @Vin=0.14V
Output Current	7.5uA @Vin=0.18V Vout=0.74V	21uA @Vin=0.18V Vout=0.5V	120uA @Vin=0.12V Vout=1.2V	120uA @Vin=0.14V
Max Efficiency (Power)	-- @Vin=0.18V	72.5% @Vin=0.45V	27.0% @Vin=0.12V	30.0% @Vin=0.14V
Off-Chip Components	None	Capacitors	Inductor	Inductor

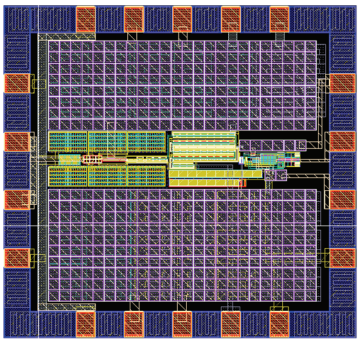


Fig. 6. Test chip layout.

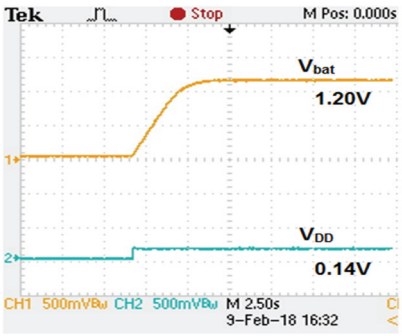


Fig. 7. Measurement of charge control output.

4. Conclusions

In this work, the proposed harvesting system combines a charge pump and a boost converter is successfully implemented. The acceptable input voltage range is 0.14~0.23 V. The output is regulated at 1.2 V with a constant supply current of 120 uA. The efficiency is 30 % at minimum input voltage while a maximum efficiency of 60 % can be successfully obtained.

References

[1]. P. Chen, K. Ishida, X. Zhang, Y. Okuma, Y. Ryu, M. Takamiya, T. Sakurai, 0.18-V input charge pump with forward body biasing in startup circuit using 65 nm CMOS, in *Proceedings of the IEEE Custom Integrated Circuits Conf. (CICC'10)*, 2010, pp. 239-242.

[2]. J. Kim, P. K. T. Mok, C. Kim, A 0.15 V Input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement, *IEEE Journal of Solid-State Circuits*, Vol. 50, February 2015, pp. 414-425.

[3]. A. Tyagi, C. Gopi, P. Baldi, A. Islam, CNFET-based 0.1 to 1.2 V DC/DC boost converter with voltage regulation for energy harvesting applications, *IEEE Trans. Circuits Syst. I*, Vol. 14, July 2015, pp.660-667.

(038)

Portable Continuous-Monitoring System Device for Monitoring the Microclimate in the Shoe-foot Interface

José de Jesús Sandoval-Palomares [1], Javier Yáñez-Mendiola [1], Alfonso Gómez-Espinosa [2] and José Martin López-Vela [1]
[1] CIATEC A.C, Omega 201, Industrial Delta, 37545 León, Gto., México
[2] Tecnológico de Monterrey, Campus Querétaro, Epigmenio González #500,
Fracc. San Pablo 76130, Querétaro, Qro., México
Tel.: + 52 4777100011
E-mail: jsando@ciatec.mx

Summary: A new continuous monitoring portable system device is presented here, it allows to reduce the complications that arise from diabetic foot ulcer, because of temperature and humidity disorders. This device monitors the microclimate of the shoe and consists of one array of 10 sensors to obtain the temperature and humidity data between the foot and the insole interface of the shoe. It has also a software interface for viewing and analyzing the data. Temperature monitoring of the participants showed an average range of 23.90 °C to 29.34 °C and 51.57 to 69.78 relative humidity.

Keywords: Temperature, Humidity, Microclimate, Ulcer, Diabetic foot.

1. Introduction

A common diabetic foot disorder located on the plantar surface of the foot is dry skin. The dry skin occurs of certain temperature and humidity conditions, adding disorders in diabetic foot [1, 2]. The development of solutions for sensor applications is an important area in healthcare monitoring [3]. It is accepted in the literature that it is important to have a quantitative way to measure temperature and humidity conditions.

A continuous-monitoring portable-system device is presented here to help preventing of complications that arise from diabetic foot [4]. The device consists in one array of 10 sensors to obtain the temperature and humidity data of the microclimate between the foot and the insole of the shoe. A software interface was developed to show graphically data from the microclimate. In order to perform an analysis of the data's behavior, a 2D plot approximation of the data was created following an exponential curve [5, 6].

1.1. System

The acquisition of temperature and humidity data is carried out in the microclimate between the plantar surface of the foot and the insole of the shoe, with a system consisting of three modules. The first one (M1) is a portable module that allows us to take direct data of temperature and humidity using 10 sensors, a second module (M2) interconnects M1 and a personal computer (PC) and the third module (M3) is a software interface that allows acquisition of the data and displaying text and graphics of the temperature and humidity results.

1.2. Hardware Architecture

The M1 architecture consists of 10 SHT15 sensors (Sensirion, Switzerland) with reading ranges of 100 % RH ±2 % for relative humidity and -40 to 123.8 ± 0.3 °C for temperature. For the connection and communication we used a microprocessor PIC18F452 (Microchip, USA), an AT24C256 memory (Atmel, USA), and a 9 V battery. The sensors were separated into two flexible segments with five sensors each one. They were connected to a screen for viewing the temperature and humidity data during capture.

1.3. User Interface

In M3 module, the obtained temperature and humidity data is stored in a database in MySQL, then the user interface can be used to select readings and plot data in a graphical form in both 2D and 3D. It allows comparison of data between different sensors and readings intervals and some basic statistics calculus can be developed.

1.4. Analysis of Curve

For an analysis of curve behavior, an algorithm was implemented to determine the least squares values for the α and β coefficients of an exponential polynomial (1). In this case, as the curve is not linear, we opted for the use of the Gauss-Newton non-lineal iterative method.

$$y = 1 - \beta\, e^{(-\alpha * t)}, \qquad (1)$$

where y is the dependent variable, e is the Euler number, t is the time and α and β coefficients are the calculated independent variables.

2. Results

2.1. Test

For the validation of the system device we proceeded with the data collection placing the sensors on calf-skin insoles; two sensors for the forefoot, two for the midfoot and one for the hindfoot then the insoles were placed inside the shoes. The system module M1 was programmed for readings with duration of 60 minutes. In our scenario, we took data from adult male participants and who declared to be without diseases or pathologies on their feet.

Temperature monitoring of the participants showed an average range of 23.90 °C to 29.34 °C, in relation to relative humidity the results were 51.57 to 69.78 RH.

2.2. Monitoring Portable-System

There were no technical problems during the 3000 temperature and humidity data readings.

Fig. 1 shows the continuous-monitoring portable-system, M1 module with the interface connected to the 10 sensors placed on the insole, the display to show temperature and humidity data, the M2 module with the interface to M1 and UBS to PC. Fig. 2 shows the corresponding experimental readings temperature graphs and the time behavior exponential graph. Fig. 3 shows the user software interface with the temperature and humidity 2D graphs of 10 sensors, and modules for selection of sensor to show, the number of reading, time range and statistical results.

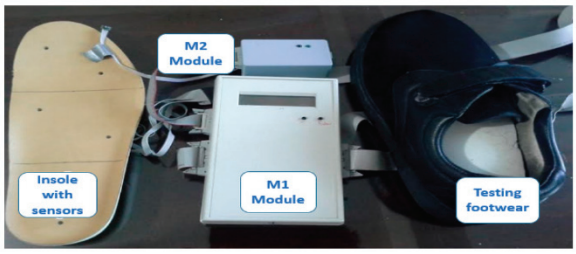


Fig. 1. Prototype of portable system for monitoring the microclimate in the interface of foot, shoes and insole with sensors.

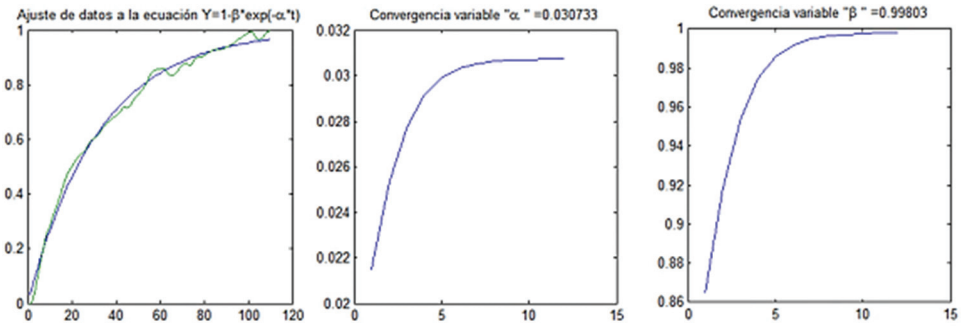


Fig. 2. Graph of experimental measurements of temperature, and curve behavior of an exponential polynomial.

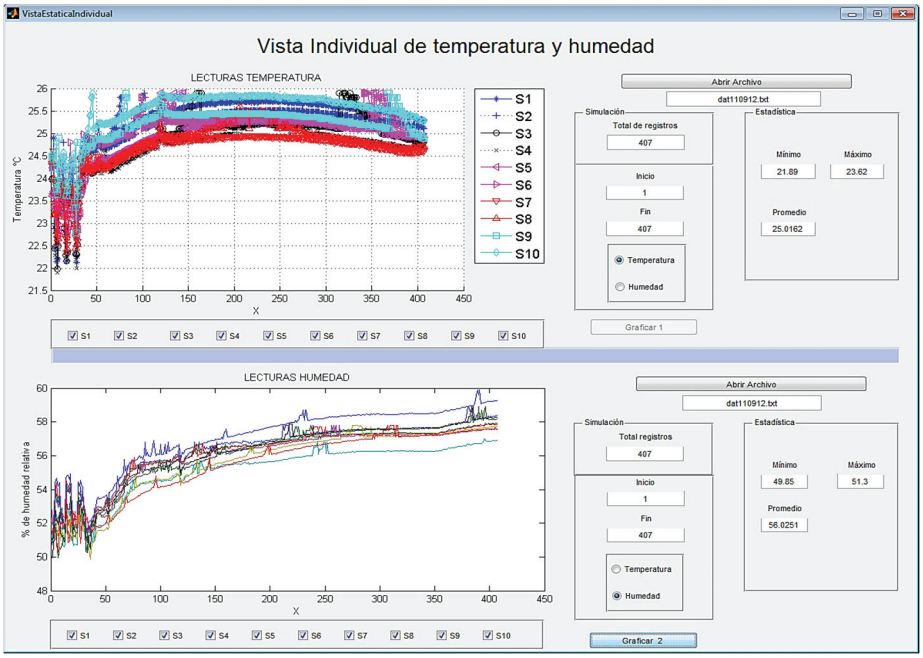


Fig. 3. Software interface to select the data range of each sensor and show its 2D graph.

3. Conclusions

We provided a portable and autonomous microclimate monitoring system for temperature and humidity readings placed into the shoes. Up to eight continuous hours of readings at one minute intervals, technically without problem.

Our results have indicated that the system for monitoring microclimates in the foot-footwear interface is a useful tool for medical applications, which may help to decrease or prevent the onset of diabetic ulcers and other diabetic foot complications.

For the future work, we are planning to perform studies using several types of footwear, as well as working with specific population groups that require specialized footwear, such as factory workers and patients with diabetes.

References

[1]. P. C. Sun, H. D. Lin, S. H. E. Jao, Y. C. Ku, R. C. Chan, C. K. Cheng, Relationship of skin temperature to sympathetic dysfunction in diabetic at-risk feet, *Diabetes Research and Clinical Practice*, Vol. 73, Issue 1, 2006, pp. 41-46.

[2]. M. Aye, E. A. Masson, Dermatological care of the diabetic foot, *American J. Clinic. Derma*., Vol. 3, 2002, pp. 463-474.

[3]. A. H. A. Razak, A. Zayegh, R. K. Begg, Y. Wahab, Foot plantar pressure measurement system: A review, *Sensors*, Vol. 12, Issue 7, 2002, pp. 9884-9912.

[4]. J. J. Sandoval-Palomares, J. Yáñez-Mendiola, A. Gómez-Espinosa, J. M. López-Vela, Portable system for monitoring the microclimate in the footwear-foot interface, *Sensors*, Vol. 16, 2016, 1059.

[5]. F. D. Foresee, M. T. Hagan, Gauss-Newton approximation to Bayesian learning, in *Proceedings of the IEEE International Conference on Neural Networks (ICNN'97),* Vol. 3, 1997, pp. 1930-1935.

[6]. J. Nocedal, S. J. Wright, Numerical Optimization, 2nd Ed., *Springer*, Berlin, 2006, pp. 259-262.

(039)

Microwave Tunable SIW Filter with Liquid Crystals

S. Missaoui [1], S. El Missaoui [1] and M. Kaddour [2]
[1] University of Tunis El Manar, Faculty of Science of Tunisia, 2092,
[2] University of Sfax, Faculty of Science of Sfax, 3029, Sfax, 2092, Tunisia
E-mail: mohsen_kaddour_tn_Fss@yahoo.fr

Summary: A new tunable rectangular substrate integrated waveguide (SIW) and its applications to band-pass filter are presented in this work. The tenability is achieved by using Liquid Crystals substrate (LCs) as a tunable dielectric. The respective design is presented for use in Wireless Communication System applications. Simulations and measurements confirm the improvement of performance by using this new structure with LCs: achieving a return loss (S_{11}) better than -35 dB and an insertion loss (S_{21}) less than -0.67 dB with a bandwidth of around 65 MHz. The anisotropic properties of LCs molecules allows to shift the central frequency from 2.33 GHz to 1.94 GHz which means a relative tuning range of 16.73 %, to decrease the return loss and insertion loss of about 44.6 % and 57.59 % respectively, when an external DC voltage is applied to the device. Good agreement is achieved between the simulated and measured results.

Keywords: Filters, Liquid crystals, Substrate integrated waveguide (SIW), Tunable devices.

1. Introduction

The current progression of wireless communication technologies has become multi-standard, having multiband coverage and multi-functionality. Hence, they require a wide variety of analog circuits containing several amplifiers, filters, oscillators, antenna, etc., for each specific application frequency. As a result of this evolution, much attention has been devoted to designing and manufacturing frequency tunable and reconfigurable devices especially the filter that constitute a key component in the radio frequency (RF) chain and microwave device. Reconfigurable filter has special significance in future smart and miniaturized wireless systems. It consists to replacing the need for multiple channels, improving overall system reliability, and reducing size, weight, complexity, and cost. it has a control circuit to adjust their characteristics such as center frequency, bandwidth, and selectivity in a predetermined and controlled manner, The present research tries to including substrate integrated waveguide (SIW) technique [1] and filters, because it has several advantage of low loss and cost, high power handling capability, easy integration [2] and compact volume size.

The SIW combines the best and complementary features of both planar transmission lines and non-planar waveguides. Some improved structures of SIW were proposed for miniaturization and enhancement of their spurious suppression characteristics [3]. Thus, it is found very appropriate in microwave and millimeter-wave tunable filter applications.

An alternative method for frequency reconfiguration is provided by material variation. Generally in this method, an applied static electric field is used to change the relative permittivity and an applied static magnetic field is used to change the relative permeability of a material embedded in the devices. The most common materials that are frequently used for frequency shifting are ferrite [4], ferroelectric [5] and more recently liquid crystal (LCs) [6].

Due to their flexibility as a liquid dielectric and because of their anisotropic characteristics [7], liquid crystals have been used widely in telecommunication and microwave devices, where they have showed promising results in terms of both tenability and performance [7-9].

Recently, a new LC mixture (GT3 series from Merck KGaA, Germany) is synthesized especially for microwave applications. This new series of LC is used, in this paper, to design a new tunable SIW pass band filter.

This work is focused on a reconfigurable rectangular SIW filter based on liquid crystal known to produce tenability thanks to the variability of their characteristics [10]. Tenability can be induced by applying an external electric field [11] to change the characteristics of the studied device.

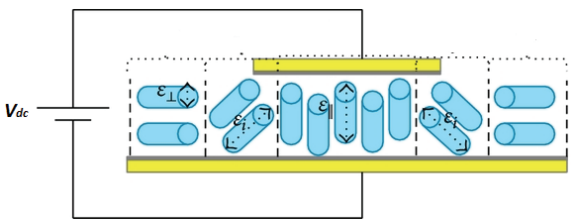


Fig. 1. Configuration parallel and perpendicular permittivity ($\varepsilon_{r\parallel}$, $\varepsilon_{r\perp}$).

To realize the concept, the reconfigurable mechanism of the filter response is analyzed, in which a holes on the top metallic surface of the SIW filter are applied for mode regulation. This new technique is used to reduce the cost, minimize the size and enhance the performance of this structure. A TE_{10} mode of

propagation is used as a dominant mode to realize a single-mode of the microwave filter witch operating at 2 GHz. The reconfigurable filter including a rectangular SIW are simulated and compared with the measured results [12] to confirm the accuracy of the proposed analysis.

2. Equations Liquid Crystal as Tunable Material for Microwave Applications

Liquid crystals are dielectric materials with anisotropic characteristics exist in a mesophase between crystalline solid and an isotropic liquid [1]. LCs can be processed around 300 °C, has excellent electrical properties, very low moisture absorption, light weight, mechanical stiffness, thermal stability (CTE = 0-30 ppm/°C), chemical resistance. The anisotropy property of LCs in the nematic phase, deduced from a permittivity tensor. It depends on the direction of the applied electric field which is created in the LC substrate by applying in addition to the microwave signal, a low frequency voltage command (Fig. 1).

As a result of applying an electric field command, the molecules of liquid crystal will gradually move parallel to the RF, thus changing the value of the permittivity and loss tangent to $\varepsilon_{r//}$ and $\tan\delta_{//}$ respectively. The saturation permittivity is related mainly to the liquid crystal permittivity $\varepsilon_{r//}$. The random distribution of the liquid crystal molecules in this case can be described by order parameter S, expressed by:

$$S = \langle \frac{3}{2} cos^2\theta - \frac{1}{2} \rangle, \quad (1)$$

where θ is the average angle between the molecular axis and the director $\vec{n}$, < > is the average orientation of all molecules.

Anisotropy is then defined as the difference between parallel and perpendicular permittivity and ensues from the following relation:

$$\Delta\varepsilon = \varepsilon_{r\parallel} - \varepsilon_{r\perp}. \quad (2)$$

The dielectric anisotropy permits the frequency agility. All of these advantages make it appealing for high frequency applications.

3. Tunable Rectangular SIW Filter Parameters and Structure

The rapid growth in wireless communication systems need the use of a new guided wave structures called substrate integrated waveguide (SIW) which can be synthesized on a planar resonator and filter with periodic arrays of metalized via holes inside the cavity.

The design rules for the rectangular SIW based upon TE_{10} are determined by the resonant frequency:

$$f_{r(10)} = \frac{c}{2\pi\sqrt{\mu_r\varepsilon_r}}\sqrt{(\frac{\pi}{w_{eff}})^2 + (\frac{\pi}{l_{eff}})^2}, \quad (3)$$

where $f_{r(10)}$ is the first resonant mode of the cavity, c is the speed of light in free space, μ_r and ε_r are the relative permeability and the dielectric constant of the substrate respectively. W_{eff} and l_{eff} are the efficient length and width of the SIW cavity.

The l_{eff} and w_{eff}, should be replaced the equivalent width (w_{SIW}) and length (l_{SIW}) of the SIW cavity because of the presence of vias side wall.

$$w_{eff} = w_{SIW} - \frac{d^2}{0.95p} \; l_{eff} = l_{SIW} - \frac{d^2}{0.95p}, \quad (4)$$

$$d > 0.2\lambda_0 \; \frac{d}{p} < 0.5, \quad (5)$$

where d is the diameter of the vias, and p is the center to center separation between the vias along the longitudinal direction as shown in Fig. 2.

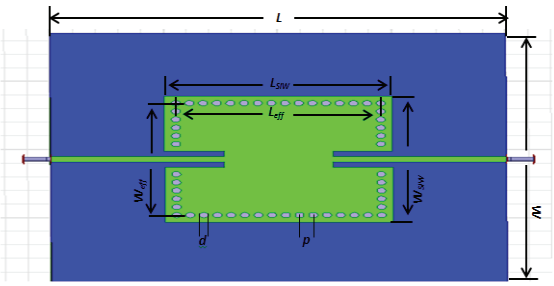


Fig. 2. Dimensions of the SIW.

The tunable rectangular SIW filter is designed and optimized through the simulation tool HFSS.13 (High frequency structure simulator) in order to evaluate the overall performance of the novel tunable structure. Parametric study for different parameters of the reconfigurable SIW filter has been performed to find the most optimum values. The structure of the rectangular SIW filter based on LCs is shown in Fig. 3.

The SIW pass band filter with vias holes has been designed on FR4 with electrical permittivity ε_r = 4.4 and thickness of 1.6 mm. the rectangular SIW is printed on LC substrate with thickness of 1.2 mm and size of 48.7×51.62 mm^2. A cavity was hollowed in the substrate to host a liquid crystal by capillarity with a low dielectric constant permittivity (from ε_r = 2.7 to ε_r = 3.3) and a loss tangent of 0.0143, whilst the via-hole diameter d = 2 mm and the distance between adjacent vias (pitch) p = 3 mm. The ground plane covers the back side of the substrate had a size of 92×100 mm^2. The tunable rectangular SIW filter is excited by a microstrip line printed on a partial grounded substrate. The microstrip feed line is designed to match 50 Ω characteristic impedance. The impedance matching of the proposed structure is enhanced by correctly adjusting the dimension of the feeding structure and the radiating patch size. The final

physical length, and width, of SIW filter are 48.75 mm and 51.62 mm respectively.

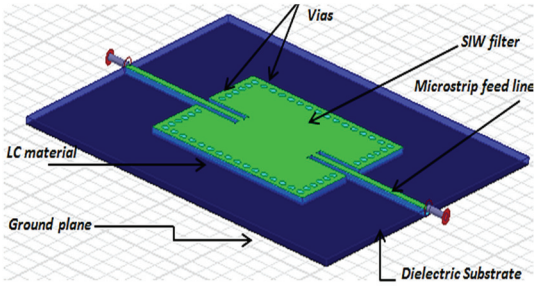


Fig. 3. Structure of tunable rectangular SIW filter.

3. Result and Discussion

Comparison of the simulated and measured return loss and insertion loss of the SIW filter without LCs is presented in Fig. 4, where it can be seen that measured and simulated return loss are in good agreement. there is nevertheless a noted frequency shift of 45 MHz (2.25 %) from the center frequency, which is due to the variations of permittivity in the substrate, i.e. 4.6 ± 0.15 (up to 3.26 %) and the inconsistencies of dielectric thickness, i.e. 1.6 ± 25 (up to 1.56 %), as well as manufacturing tolerance.

In this section, a method to improve the performance of the SIW filter and to replace the need for multiple filters is introduced. The proposed approach consists of placing LCs in the cavity of the SIW filter.

Figs. 4 and 5 show the simulated and measured S_{11} and S_{21} of the rectangular SIW filter for two different permittivity (2.55 and 2.7). We can be seen that the use of the LC material in our structure decreases the retour loss and insertion loss of the SIW filter of a value of 18.96 % and 6.33 % respectively, and confirms the potential frequency agility.

The tuning in the rectangular SIW filter is assured by varying the permittivity of the LC from $\varepsilon_{r\perp} = 2.5$ (without polarization) to $\varepsilon_{r\parallel} = 3.3$ (with polarization), as shown in Fig. 6. The variation value of the permittivity of the LC allows moving the return loss of the SIW filter, so as to cover adjacent frequency bands. The center frequency of this filter varied from 2.33 GHz to 1.94 GHz corresponds to an important frequency agility of 16.73 %. So, we can conclude that this structure with LCs and applied continuous voltage enable to decrease the return loss and insertion loss of about -16.93 dB (44.6 %) and 0.91 dB (57.59 %) respectively.

We noticed that the SIW pass band filer achieved a minimal frequency with a permittivity of 3.3 which corresponds to maximal permittivity of liquid crystals in the saturation phase.

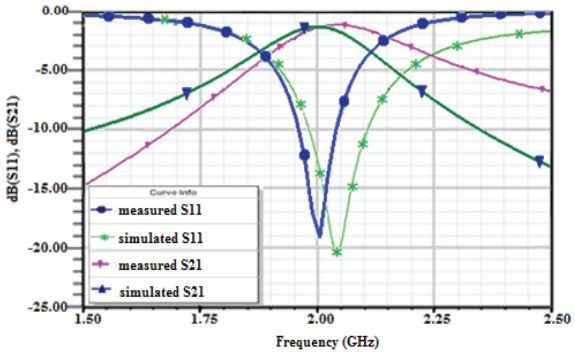


Fig. 4. Simulated and measured S_{11} without LCs.

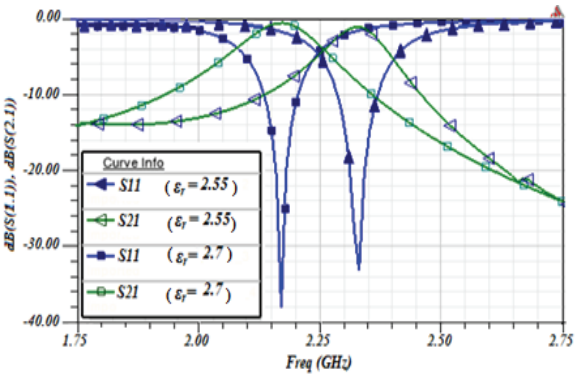


Fig. 5. Return loss and insertion loss with LCs.

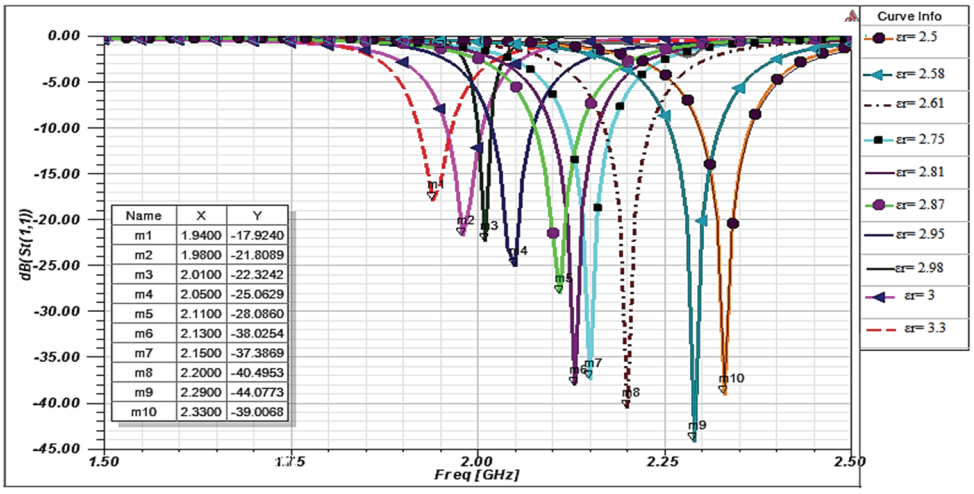


Fig. 6. Frequency agility of the SIW filter.

4. Conclusions

We have discussed the design concept as well as the performances of tunable SIW pass band filter based on Liquid Crystals substrate. In order to be applicable to the next generation mobile communication systems, there are several requirements such as tenability, miniaturization and high performances. From these results, the proposed reconfigurable SIW pass band filter is successful demonstrated, and the filter topology is simple to implement. So, the reconfigurable SIW filter can be good channelizer for multimode/multi-frequency and radio systems.

References

[1]. Y. J. Cheng, Substrate integrated waveguide frequency-agile slot antenna and its multibeam application, *Progress in Electromagnetics Research*, Vol. 130, 2012, pp. 153-168.

[2]. D. Wang, W. Che, P. Russer, Tunable substrate-integrated waveguide dual-mode square cavity filter with metal cylinders, in *Proceedings of the IEEE MTT-S International Microwave Workshop Series on Art of Miniaturizing RF and Microwave Passive Components*, December 2008, pp. 128-131.

[3]. D. Deslandes, K. Wu, Accurate modeling, wave mechanisms and design considerations of a substrate integrated waveguide, *IEEE Trans. Microw. Theiry Tech*., Vol. 54, Issue 6, June 2006, pp. 2516-2526.

[4]. E. Salahun, G. Tanne, P. Queffelec, M. le Floc'h, A.-L. Adenot, O. Acher, Application of ferromagnetic composite in different planar tunable microwave devices, *Microwave and Optical Letters*, Vol. 30, Issue 4, 2001, pp. 272-276.

[5]. H. T. Su, M. J. Lancaster, F. Wellhofer, Electrically tunable super conducting quasi lumped element resonator using thin-film ferroelectric, *Microwave and Optical Technology Letters*, Vol. 24, Issue 3, 2000, pp. 155-158.

[6]. S. Missaoui, S. El Missaoui, M. Kaddour, Tunable microstrip patch antenna based on liquid crystals for microwave applications, in *Proceedings of the XXIst International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED'16),* September 2016, pp. 88-91.

[7]. D. E. Schaub, D. R. Oliver, A circular patch resonator for the measurement of microwave permittivity of nematic liquid crystal, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 59, Issue 7, 2011, pp. 1855-1862.

[8]. S. El Missaoui, S. Missaoui, M. Kaddour, Integration of a compact circularly polarized antenna array with a reconfigurable symmetric stub phase shifter using liquid crystals substrates, *European Journal of Scientific Research*, Vol. 120, Issue 2, 2014, pp. 153-161.

[9]. S. Missaoui, M. Kaddour, Liquid crystal-reconfigurable conformal monopole antennas structures for microwave applications, *Journal of Engineering and Technology Research*, Vol. 4, Issue 3, February 2012, pp. 57-64.

[10]. J. Anderson, P. E. Watson, P. J. Bos, Liquid Crystal Display 3-D Director Simulator Software and Technology Guide, *Artech House*, Boston, MA, 2001.

[11]. N. Martin, P. Laurent, C. Person, P. Gelin, F. Huret, Size reduction of a liquid crystal-based, frequency-adjustable patch antenna, in *Proceedings of the 34th European Microwave Conference*, Vol. 2, 2004, pp. 825-828.

[12]. Z. Zakaria, W. Y. Sam, M. Z. A. Abd Aziz, K. Jusoff, M. A. Mohamad, A. Mutalib, N. Z. Haron, A novel structure of multilayer SIW filter and patch antenna, *International Journal of Engineering and Technology (IJET)*, Vol. 5, Issue 5, 2013, pp. 4400-4411.

(040)

A 16-Gbps Low-Power Transceiver for High-Speed Serial Links

Jongsun Kim and Jahyun Gu
Hongik University, Seoul, Korea
Tel.: + 82-2-320-3014
E-mail: js.kim@hongik.ac.kr

Summary: A 16-Gbps low-power transceiver for high-speed serial links is presented. The proposed transmitter utilizes a programmable-swing near-ground voltage-mode driver. The receiver adopts a multiple gain-path differential amplifier with feed-forward capacitors that boost high-frequency gain. The receiver utilizes an adaptive bias generation scheme to compensate the input common-mode variation. The small-swing and impedance matching techniques applied to the transceivers effectively improve signal integrity and power efficiency. The proposed SerDes transceiver designed in a 65-nm CMOS technology achieves a data rate of 16 Gbps/channel and 0.3 pJ/bit power efficiency over a 10-cm FR4 PCB.

Keywords: Serial link, Transceiver, SerDes, Mobile interface, Memory interface.

1. Introduction

The ever-increasing demand for higher data rates in battery-operated mobile devices, such as smart phones with multi-core application processors and low-power mobile memories, is pushing the off-chip signaling power consumption of multi-Gb/s/channel mobile I/O interfaces into the sub pJ/bit range.

In this paper, we present a low-power near-ground signaling serializer-deserializer (SerDes) transceiver which is suitable for use in point-to-point mobile I/O interfaces and memory interfaces. The proposed low-swing transceiver achieves a data rate of 13 Gb/s/pair and a power efficiency of 0.3 pJ/bit over a 10-cm FR4 printed circuit board trace. To achieve this low-power and high signal integrity, the transmitter adopts an on-chip regulated near-ground voltage-mode driver [1-3] and a simple impedance matching technique and the receiver utilizes a multiple gain-path differential amplifier with feed-forward capacitors [4] that boost high-frequency gain.

2. Proposed SerDes Transceiver Architecture

Fig. 1 shows the proposed serial-link interface architecture used in this design. It consists of a transmitter (Tx) and a receiver (Rx) at both ends on a 10-cm FR4 differential transmission line. This point-to-point serial link channel is unterminated, however, both the output impedance of the transmitter and the input impedance of the receiver are set to the channel characteristic impedance, resulting in a good signal integrity.

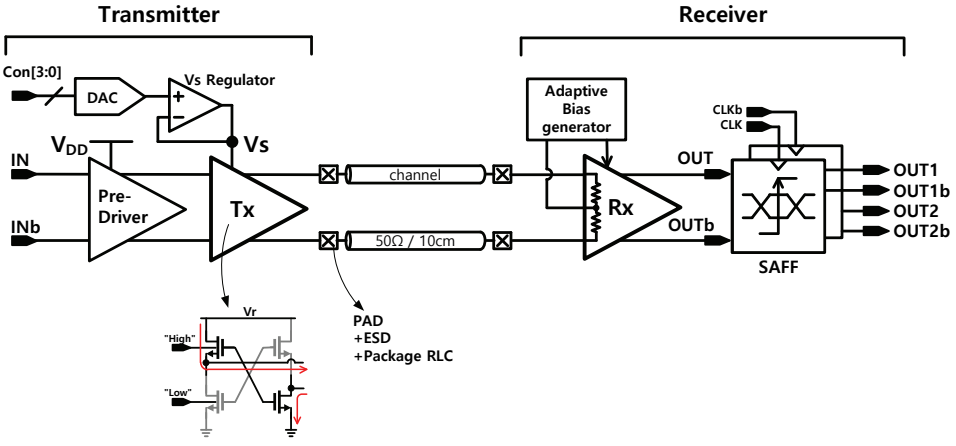


Fig. 1. Proposed serial-link interface architecture.

Fig. 2 shows the transmitter circuit, consisting of a regulated supply block, a pre-driver, and a voltage-mode output driver [1, 2]. The regulated supply block consists of a reference current generator, a digital-to-analog converter (DAC), and a Vs regulator. The regulator output can be adjusted digitally via the DAC. The Vs regulator generates a digitally adjustable supply voltage of about 200 mV, resulting in a differential peak-to-peak output swing of 100 mV.

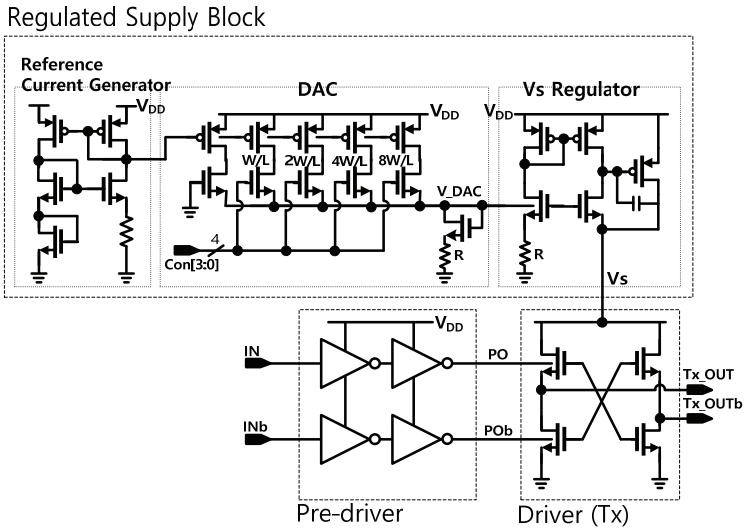


Fig. 2. Proposed transmitter architecture.

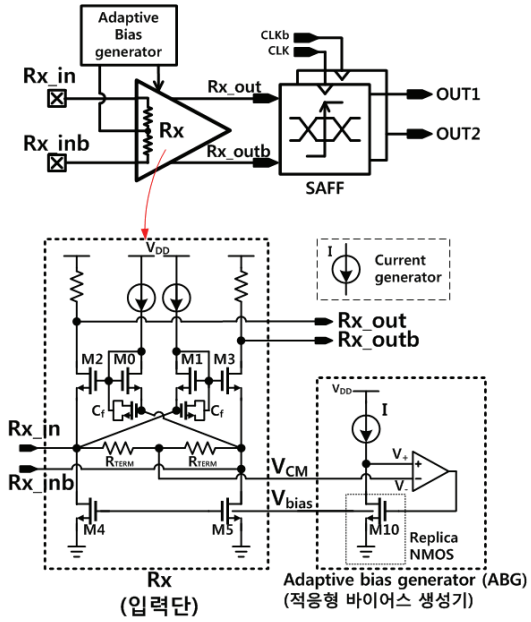


Fig. 3. Proposed receiver architecture.

Fig. 3 shows the low-power NGS receiver proposed in this paper. For high-speed operation above 10 Gb/s, this receiver consists of an input receiver (Rx), an adaptive bias generator (ABG) and a sense-amplifier based flip-flop (SAFF [7]) with a common-gate amplifier structure. In addition to the basic operation in which Rx amplifies a small differential input signal Rx_in/Rx_inb and generates an output signal Rx_out/Rx_outb suitable for SAFF driving at the next stage, the input impedance must be maintained at 50 Ω for impedance matching with the channel. In this paper, the driving voltage Vs of the transmitter output terminal Tx can be adjusted programmatically according to the state and length of the transmission line, and the swing level of the transmission signal can be adjusted through this. When the amplitude of the transmission signal changes according to the change of Vs, the common mode voltage V_{CM} of the receiver's input terminal also changes, which affects the operation characteristics of the Rx. In this paper, we present a new adaptive bias generator (ABG) using a common-mode feedback in order to correct the current mismatch problem in the receiver input stage according to this VCM changes.

3. Experimental Results

The proposed low-power NGS transceiver was designed using a 65 nm CMOS process. The proposed N-over-N structure transmitter with a programmable Vs regulator with 110-350 mV voltage level has a common mode near ground level and a programmable output swing width of 80-175 mV. The proposed receiver with differential common-gate amplifier type inputs using ABG achieves improved high-frequency characteristics using multiple gain-path structures.

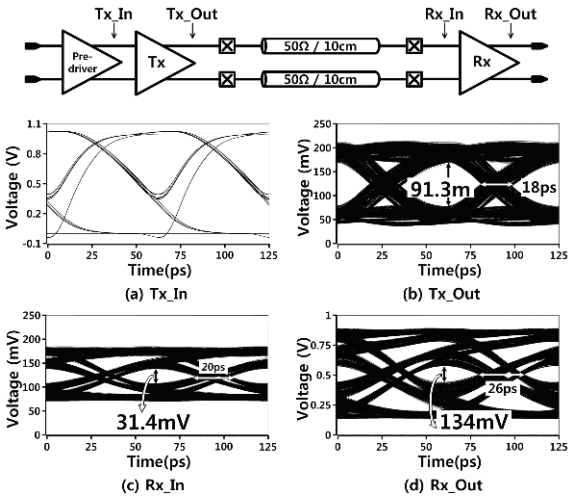


Fig. 4. Simulated eye-diagram of the NGS transceiver operation (16 Gb/s, Vs = 260 mV).

Fig. 4 shows the eye-diagram of the NGS transceiver interface operating at 16 Gb / s over a 10 cm transmission line. Fig. 4(a) shows the output of

the pre-driver. It can be seen that the asymmetric rise/fall time has an upward common mode level at high frequencies. Fig. 4 (b) shows the eye of the output stage Tx when Vs = 260 mV. It has an amplitude of about 91.3 mV, which shows that the impedance matching of the output stage and the channel is well done. Fig. 4(c) shows that the attenuated signal through the 10 cm channel enters the input of the receiver. It has a low common mode of about 125 mV and an open-eye of 31.4 mV amplitude. Fig. 4(d) shows that the signal amplified through input Rx has an eye-height of 134 mV at 16 Gb/s.

Table 1. Comparison of transceiver performance.

	[1]	[3]	[4]	**This Work**
Process	90 nm	40 nm	65 nm	**65 nm**
Supply (V)	1.0	1.0	0.6-0.8	**1.0**
Channel length (cm)	80	7.62	8.89	**10**
Tx output swing (mV)	200	400	100-200	**80-175**
Data rate/channel	6.25 Gbps	16 Gbps	4.8-8 Gbps	**16 Gbps**
Tx power (mW)	2.26	-	1.92@6.4 Gbps	**2.06@13 Gbps**
Rx power (mW)	2.3	2.69	1.07@6.4 Gbps	**1.3@13 Gbps**
Sampler(SAFF) power	0.5	-		**0.57@13 Gbps**
Total power	5.06		3@6.4 Gbps	**3.93@13 Gbps**
Power efficiency (pJ/bit)	0.81	-	0.47@6.4 Gbps	**0.3@13 Gbps (with SAFF)**

4. Conclusions

In this paper, we introduce a low-power, low-swing SerDes transceiver with a common mode close to ground level. The proposed transceiver was designed in a 65-nm 1.0-V CMOS process to achieve a data rate of 16 Gb/s and a power efficiency of 0.3 pJ/bit (= 0.3 mW/ Gb/s) on a 10-cm FR4 PCB channel.

Acknowledgements

This work was supported by the KIAT grant funded by the Korean government (MOTIE No. N0001883). The EDA tools were supported by IDEC.

References

[1]. J. Poulton, et. al, A 14-mW 6.25 Gb/s Transceiver in 90-nm CMOS, *IEEE J. Solid-State Circuits*, Vol. 42, 2007, pp. 2745-2757.

[2]. B. Leibowitz, et. al, A 4.3 GB/s memory interface with power-efficient bandwidth scaling, *IEEE J. Solid-State Circuits*, Vol. 45, April 2010, pp. 889-898.

[3]. K. Kaviani, et. al, A 0.4-mW/Gb/s near-ground receiver front-end with replica transconductance termination calibration for a 16-Gb/s source-series terminated transceiver, *IEEE J. Solid-State Circuits*, Vol. 48, Issue 3, March 2013, pp. 636-648.

[4]. Y.-H. Song, et. al, A 0.47-0.66 pJ/bit, 4.8-8 Gb/s I/O Transceiver in 65 nm CMOS, *IEEE J. Solid-State Circuits,* Vol. 5, May 2013, pp. 1276-1289.

[5]. K. Abugharbieh, et. al, An ultralow-power 10 Gbits/s LVDS output driver, *IEEE Trans, Circuits Syst. I*, Vol. 57, Issue 1, January 2010, pp. 262-269.

[6]. K. Kaviani, et al., A 6.4-Gb/s near-ground single-ended transceiver for dual-rank DIMM memory interface systems, in *Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'13)*, February 2013, pp. 306-307.

[7]. B. Nickolic, et al, Sense-amplifier based flip-flop, in *Proceedings of the IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC'13)*, February 1999, pp. 282-283.

(041)

Pt-functionalized AlGaN/GaN Heterojunction Hydrogen Gas Sensor for Extreme Environment Operation

Hyungtak Kim and Ho-Young Cha
School of Electronic and Electrical Engineering, Hongik University, Seoul, Korea
Tel.: +8223203013, fax: + 8223201193
E-mail: hkim@hongik.ac.kr

Summary: Pt-functionalized FET-type hydrogen gas sensors based on AlGaN/GaN heterojunction were fabricated and investigated for extreme environment operation. Gateless field effect transistors were fabricated on AlGaN/GaN-on Si platform and the gate area was functionalized with Pt as hydrogen catalyst. The sensor devices demonstrated hydrogen sensing performance up to 250 °C with sensitivity enhancement. In addition, the hydrogen sensitivity was not degraded by highly-energetic proton irradiation at very high fluence of 10^{15} /cm^2. These results confirm that GaN-based hydrogen sensor can be a strong candidate for extreme environment sensing application.

Keywords: Hydrogen sensor, Pt-functionalized, AlGaN/GaN heterojunction, Extreme environments, High temperature, Proton irradiation.

1. Introduction

For decades, space exploration agency has employed hydrogen gas as rocket fuel to transport crew and cargo to space and developed extensive experience in the safe and effective handling of hydrogen. With the recent focus on environment-friendly energy resource with high efficiency, hydrogen will continue to be innovatively stored, measured, processed and utilized. There is also great interest in hydrogen-fueled vehicles, aircraft, fuel cells, and industrial process [1], and hydrogen sensors have been extensively researched. In particular, wide bandgap semiconductor sensors are well-suited for extreme environment operation, due to their low intrinsic carrier concentration and high binding energy which enable them to be operated at elevated temperatures and high radiation level [2, 3]. Especially, AlGaN/GaN heterojunction has been identified as a promising candidate for gas sensors. It has a high density and mobility of carriers in two-dimensional electron gas (2DEG) channel induced by piezoelectric and spontaneous polarization. Therefore, the drain current response can be amplified through a functionalized gate electrode such as Pt or Pd catalytic metal [3-5].

In this study, we investigated Pt-functionalized FET-type AlGaN/GaN heterojunction hydrogen gas sensors for extreme environment operation. The sensor characteristics were measured at 250 °C of baseline temperature and also after 5 MeV proton irradiation with total dose of 10^{15} /cm^2.

2. Device Fabrication

The epitaxial structure consists of a 10 nm in-situ SiN_x layer, a 4 nm GaN capping layer, a 24 nm AlGaN barrier layer, and a 4.9 μm GaN buffer on a Si (111) substrate. Fig. 1 shows the cross-sectional structure of the fabricated sensor device on AlGaN/GaN-on Si platform. First, mesa isolation was performed by inductively-coupled plasma-reactive ion etching system with BCl_3/Cl_2-based discharges to define active region of sensor devices. Then drain/source ohmic contacts were formed with Ti/Al/Ni/Au (20/120/25/ 50 nm) metal layers with electron-beam evaporation followed by rapid-thermal annealing at 830 °C for 30 s in nitrogen ambient. For device passivation, the SiO_2 (200 nm) layer was deposited using a plasma-enhanced chemical vapor deposition. Ti/Au (40/600 nm) layers were used to form probing contact pad. Finally, Pt (50 nm) layer was deposited as hydrogen gas sensing catalyst on the gate area.

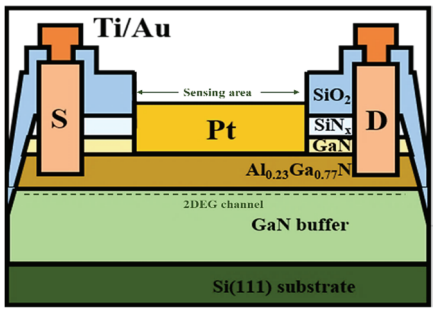


Fig. 1. Cross-sectional diagram of hydrogen gas sensor with Pt-functionalized gate area fabricated on AlGaN/GaN-on-Si platform.

3. Sensing Characteristics

3.1. High Temperature Characteristics

The fabricated sensors were submitted to five cycles of 4 % hydrogen gas for 5 s with the drain

voltage of 0.1 V in the gas chamber probing system. The current of FET-type hydrogen sensors demonstrated sensing response characteristics as shown in Fig. 2. Hydrogen-sensitivity of the sensor was 11 % at 150 °C and enhanced up to 15 % at 250 °C with a temperature-rise. This result suggests that this device can be a good candidate for hydrogen sensor operating at high temperatures.

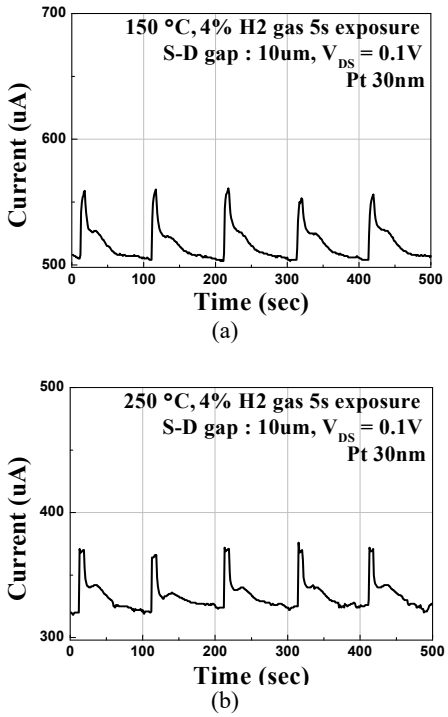


Fig. 2. The sensing response characteristics of hydrogen sensor at (a) 150 and (b) 200 °C measured with V_{DS} = 0.1 V.

3.2. Post-Irradiation Characteristics

We also performed 5 MeV proton-irradiation onto the fabricated sensor devices. Proton-irradiation was conducted with an MC-50 cyclotron at the Korea Institute of Radiological and Medical Sciences at a room temperature under low vacuum atmosphere. Total proton dose was 10^{15}/cm^2. The beam propagating direction was perpendicular to the 2DEG layer. As shown in Fig. 3, the irradiated devices exhibited the reduction of channel current from 585 to 500 μA at V_{DS}=0.1 V due to displacement damage [6, 7]. However, the sensitivity of the sensor measured at 250 °C was 12 % and 14 % before and after proton irradiation, respectively. With regard to very large amount of total dose, this result clearly demonstrates radiation hardness of hydrogen gas sensors with AlGaN/GaN heterojunction.

4. Conclusions

In summary, we investigated the operation of Pt-functionalized hydrogen gas sensors fabricated on AlGaN/GaN-on Si platform at high temperature and radiation environment. A sensitivity of hydrogen gas was enhanced with temperature-rise from 150 to 250 °C. We also observed the sensing response characteristics after proton irradiation was not degraded by 10^{15} /cm^2 proton-irradiation at 5 MeV. The ability to function in high temperature and high energy/flux radiation condition will make AlGaN/GaN heterojunctionon-based sensors very attractive in extreme environment applications.

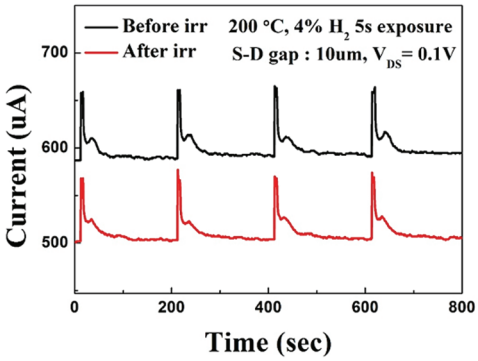


Fig. 3. The sensing response characteristics of hydrogen sensor before and after proton irradiation.

Acknowledgements

This research was supported by National Research Foundation of Korea (NRF-2016R1A1B4010474, 2017M2B2A4049495).

References

[1]. T. Hübert, et al., Developments in gas sensor technology for hydrogen safety, *International Journal of Hydrogen Energy*, Vol. 39, Issue 35, 2014, pp. 20474-20483.

[2]. J. Schalwig, et al., Group-III-Nitride based gas sensing devices, *Physica Status Solidi A*, Vol. 185, Issue 1, 2001, pp, 39-45.

[3]. Y. Xi, et al., Study of hydrogen detection response time with Pt-gated diodes fabricated on AlGaN/GaN heterostructure, *Journal of Vacuum Science and Technology*, Vol. 31, Issue 3, 2013, 232106.

[4]. H. Hasegawa, M. Akazawa, Hydrogen sensing characteristics and mechanism of Pd/AlGaN/GaN Schottky diodes subjected to oxygen gettering, *Journal of Vacuum Science Technology B*, Vol. 25, Issue 4, 2007, pp. 1495-1503.

[5]. C. F. Lo, et al., Effect of humidity on hydrogen sensitivity of Pt-gated AlGaN/GaN high electron mobility transistor based sensors, *Applied Physics Letters*, Vol. 96, Issue 23, 2010, 232106.

[6]. X. Hu, et al., The energy dependence of proton-induced degradation in AlGaN/GaN high electron mobility transistors, *IEEE Transactions on Nuclear Science*, Vol. 51, Issue 2, 2004, pp. 293-297.

[7]. B. D. Weaver, et al., Displacement damage effects in AlGaN/GaN high electron mobility transistors, *IEEE Transactions on Nuclear Science*, Vol. 59, Issue 6, 2012, pp. 3077-3080.

(042)

A PVT Insensitive Time to Digital Converter with Continuous Sampling

Hong-Yi Huang [1], Ping-Che Hsieh [1], Yung-Hsu Chen [1] and Kuo-Hsing Cheng [2]
[1] Department of Electrical Engineering, National Taipei University, Taiwan
[2] Department of Electrical Engineering, National Central University, Taiwan
Tel.: + 886-2-86741111, fax: + 886-2-26736500
E-mail: hyhuang@mail.ntpu.edu.tw

Summary: This work presents a time to digital converter (TDC) with continuous sampling, which has sufficient resolution and low power consumption. First, the time amplifier control circuit enhances the time resolution. Next, sense amplifier latch circuit measures the numbers of rise edge of input frequency within reference frequency and send the pulse wave of measurement result to next stage. Finally, the register stores the counter output data, and the reset circuit controls TDC to do continuous sampling so the system no need to enter an external signal. The layout of the test chip is realized using a 0.18 µm 1.8 V 1P6M TSMC CMOS process. The chip area is 217×169 um^2 and the power consumption is 7.2 mW.

Keywords: Time to digital converter, Continuous sampling, Time amplifier.

1. Introduction

The time to digital converter circuit is widely used in applications such as laser range-finder, ultrasonic flow meters, thermal sensor, ultrasonic thickness measurement, digital storage oscilloscopes, etc. [1, 2] This work presents process, supply voltage and temperature (PVT) insensitive TDC with continuous sampling that is applied to a capacitor sensing system for biomedical application.

2. Architecture and Circuit Design

Fig. 1 shows the function block of the time to digital converter. The architecture can produce a digital output code that is insensitive to process, supply voltage and temperature variations. A reference signal is given to sample the cycle time of the input signal (F_{in}) and converts it to a digital output code. The reset circuit is used to do continuous sampling.

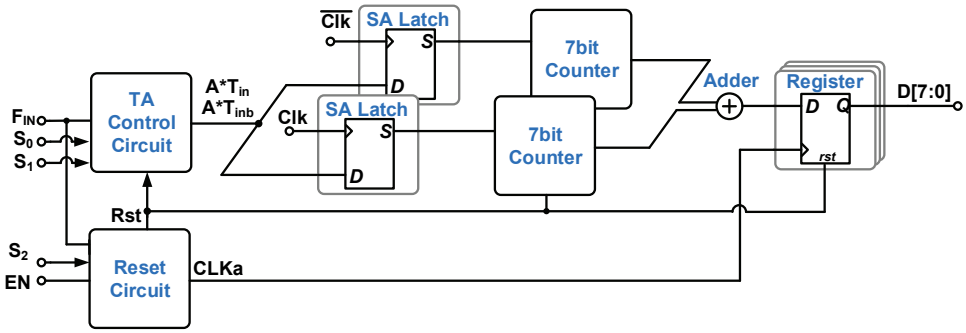


Fig. 1. Function block of time-to-digital converter.

Fig. 2 depicts the time amplifier control circuit. S1 decides the divided ratio of F_{IN} and widens the pulse width. V_{DD} is given to input of a DFF so that its output *Start* samples the first rising edge. The second rising edge is sampled by *Stop* which is output of two DFFs. Another DFF with its input connected to GND can produce *StartB* which has 180° phase difference to *Start*. The same scheme is adopted to produce *StopB* which also has 180° phase difference to *Stop*. The differential pass-transistor logic is adopted to design an XOR/XNOR function so that the rising edges of *Start* and *Stop* are combined to produce AT_{in} who has only one cycle of signal. The delay paths of all signals are carefully matched. Accordingly, the output period of time can be exactly equal to *A* times of input period of time. Accordingly, the resolution of TDC can be enhanced by ratio *A*.

The sense amplifier latch depicted in Fig. 3 is utilized to maintain high time resolution of the TDC. It is a differential circuit that contains a sense amplifier, so the operation speed can be fast. The setup time and hold time as well as delay time can be very small.

The two 7-bit counters sample the output signal of SA latch, then a 1-bit full adder accumulates the 2 outputs. The register is used to store the counter output code by the flip-flop and parallel connection. If the trigger signal CLK_a transits from "0" to "1", then the signal can be stored. To reset the signal, Rst is set to "1" and the signal is cleared.

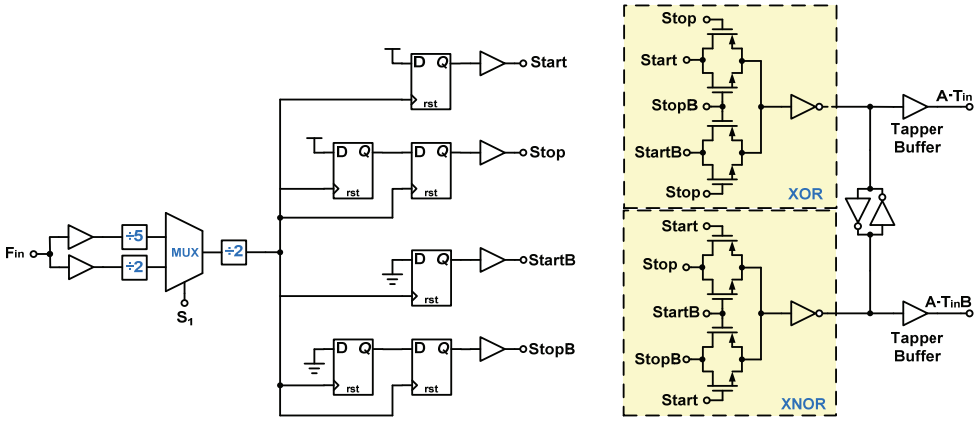


Fig. 2. Symmetrical architecture of the time amplifier control circuit.

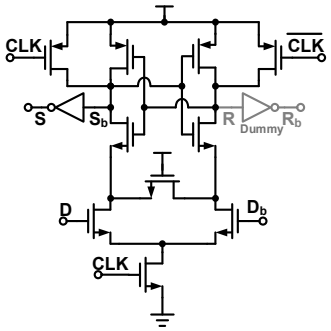


Fig. 3. Sense amplifier latch.

Fig. 4 is a reset circuit to do continuous sampling. Fig. 5 depicts the timing diagram of the reset circuit**.** If EN makes a low to high transition, then 4-bit counter begins counting. If D_0 to D_3 all pull high, then V_1 is high. The signal through a buffer triggers the register values and control signals into 2-1 multiplexer which enables the output to ground. The RST is produced, resets the circuit and begins the next sampling of F_{IN}.

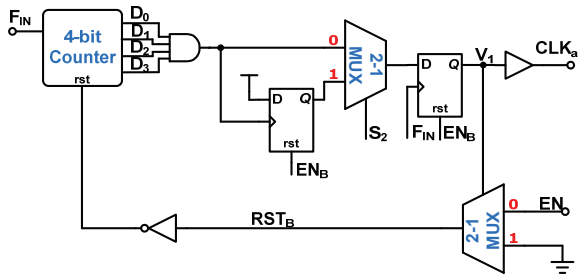


Fig. 4. Reset circuit.

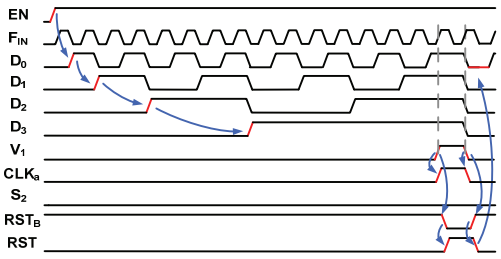


Fig. 5. Timing diagram of reset circuit.

3. Test Chip and Measurement

Fig. 5 shows the photograph of the test chip that is applied in a biomedical sensing system. The TDC is a part of the design. Fig. 6 shows measurement of the TDC with resolution of 1 MHz. The frequency range is from 190 MHz to 210 MHz. The output digital code is from 210 to 230. The data is sampled for 10 cycles.

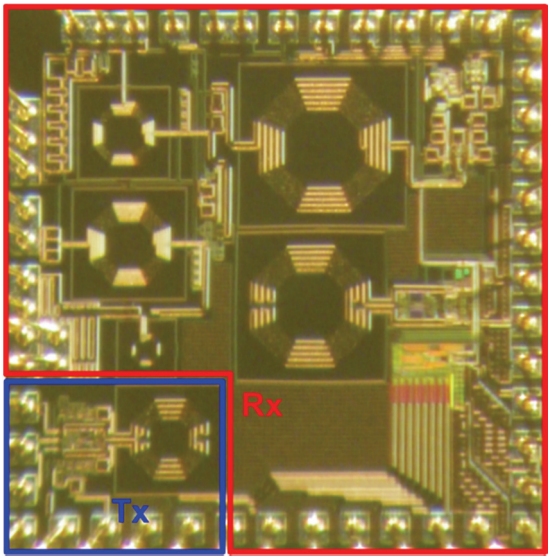


Fig. 5. Chip photograph.

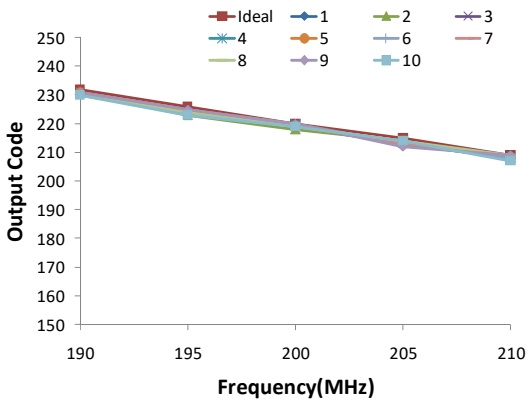


Fig. 6. Measurement results.

Table. 1. Time to digital converter comparison table.

TDC Comparison Table				
	JSSC [3]	**JSSC [4]**	**JSSC [5]**	**This Work**
Year	2012	2013	2011	2013
Tech.	0.13 um CMOS	0.18 um CMOS	0.13 um CMOS	0.18 um CMOS
Supply Voltage (V)	1.3	1.8	1.2	1.8
LSB Width$_{(min)}$(ps)	1	5	NA	43.5
Input Range (ns)$^{(*1)}$	32	NA	NA	1.53
Ref. Freq.(Hz)	100 M	52 M	NA	2.1 G 2.2 G 2.3 G
Output Bit	7	10	14	8
Continues Sampling	No	No	Yes	Yes
Sampling Rate$_{(max)}$ (MB/s)	NA	NA	3200	14.2
Power Diss.(mW)	4.3	17	7	7.2
Core Area (mm^2)	0.07	0.62	0.2	0.036

Table 1 is the comparison of the time to digital converter. The resolution is released according to the application in a biomedical system so it only requires a lower sampling rate. The chip area and power consumption is better than other references.

4. Conclusions

A time-to-digital converter is implemented in a 0.18 um CMOS process. The TDC utilized an architecture producing digital output code insensitive to process, supply voltage and temperature variations. The measurement results successfully verify that it can sample the input signal continuously. The input frequency is from 190 MHz to 210 MHz with resolution of 1 MHz.

References

[1]. J. Nissinen, P. Palojarvi, J. Kostamovaara, A CMOS receiver for a pulsed time-of-flight laser rangefinder, in *Proceedings of the European Solid-State Circuits Conference (ESSCIRC'03)*, 2003, pp. 325-328.

[2]. K. Park, J. Park, 20 ps resolution time-to-digital converter for digital storage oscilloscopes, in *Proceedings of the Nuclear Science Symposium (NSS'98)*, 1998, pp. 876-881.

[3]. Y.-H. Seo, J.-S. Kim, H.-J. Park, J.-Y. Sim, A 1.25 ps resolution 8b cyclic TDC in 0.13 um CMOS, *IEEE J. Solid-State Circuits*, Vol. 47, Issue 3, 2012, pp. 736-743.

[4]. C.-W. Yao, A. N. Willson, Jr., A 2.8–3.2-GHz fractional-N digital PLL with ADC-assisted TDC and Inductively coupled fine-tuning DCO, *IEEE J. Solid-State Circuits*, Vol. 48, Issue 3, March 2013, pp. 698-710.

[5]. W. Yin, R. Inti, A. Elshazly, M. Talegaonkar, B. Young, P. K. Hanumolu, A TDC-less 7 mW 2.5 Gb/s digital CDR with linear loop dynamics and offset-free data recovery, *IEEE J. Solid-State Circuits*, Vol. 46, Issue 12, December 2011, pp. 3163-3173.

(043)

GOx@ZIF-8(AuNPs): Synthesis and Application for Mediator Free Amperometric Glucose Sensor

Jibinlal A. [1] and Anirban Paul [2]
[1] Maulana Azad National Institute of Technology, Bhopal, India
[2] CSIR- Central Salt & Marine Chemicals Research Institute, Bhavnagar, India
Tel.: +91 8238895804
E-mail: anirbanpaul@csmcri.org

Summary: A novel method is developed for the encapsulation of gold nanoparticles and glucose oxidase combinedly into the cavity of ZIF-8 metal organic framework in aqueous media and subsequently used for amperometric glucose sensing application. ZIF-8 is highly efficient, stable (thermal and chemical) and possess large surface area with unique cavity to accommodate both the AuNPs and GOx. The as-synthesized composite is thoroughly characterized by various physico-chemical methods, confirms the uniform distribution of the AuNPs over the metal organic framework surface. The presence of highly conducting AuNPs and GOx facilitate the electrocatalytic reaction of mediator free tandem electrocatalytic reaction of both glucose oxidation and oxygen reduction. Further, the nano-composite exhibits admirable stability with low-level detection of glucose in aqueous media (50 nM of glucose) by using very low concentration of GOx (62 μg in 1 mL).

Keywords: ZIF-8, Gold nanoparticle, Amperometry, Enzymatic glucose sensor.

1. Introduction

Diabetes is the most common and widespread chronic disease affecting blood glucose levels and leads to various abnormalities as cardiac arrest, failure of kidney function, degeneration of neurons [1]. Regular monitoring of glucose level and administration of insulin shot periodically is required for the proper longterm management of blood glucose level of diabetes patients. Current monitoring methods for glucose involves painful invasive approaches and hence many patients will not follow the protocol intentionally or unintentionally [2-8]. Furthermore, insulin overdose can cause adverse effects as unconsciousness and even death. Hence, an urgent need for simple and noninvasive glucose monitoring is highly seeking.

2. Experiment

2-methlyimidazole (22.70 gm) was taken in 400 ml of ultrapure mili-Q water. 50 mg of GOx is added in the same solution. This mixture will be slightly yellow in colour due to dissolved GOx. 1.17 gm of $Zn(NO_3)_2.6H_2O$ was dissolved in another 390 ml of mili-Q water. Another 10 ml of AuNPs was taken separately. Solution of $Zn(NO_3)_2.6H_2O$ and AuNPs were added simultaneously in the mixture of 2-methylimidazole and GOx under constant stirring of 600 rpm at room temperature. The reaction mixture was stirred for 3 hours. In the very beginning of the reaction, solution was seemed transparent yellow which started to turn hazy after few minutes of stirring. The mixture was allowed to stand for overnight and then excess water was decanted. It is to be noted that the yellow colour of the mixture disappeared after the successful addition but no deep red colour of AuNPs is observed, primarily confirms encapsulation of both GOx and AuNPs respectively. The remaining solid part was centrifuged and washed with 50 ml of water for 3 times to remove any excess GOx and AuNPs (not encapsulated) if any. Further it was dried under vacuum and purple colour solid composite was obtained, refers the formation of GOx@ZIF-8(AuNPs) nanocomposite. It was further characterized by FT-IR, Powder XRD, FE-SEM, HRTEM, BET and UV-Vis spectroscopy. The crystal structure of the product was characterized by XRD (Bruker AXS X-ray diffractometer). The morphology and microstructure of the synthesized materials were investigated by FESEM (JEOL JSM-7100F, Japan) and HRTEM (JEOL JEM-2100, Japan). UV-VIS spectra were recorded with Varian spectrophotometer. FT-IR was done at Parkin-Elmer G-FTIR. For all electrochemical experiment, Plastic chip electrode of 5 mm diameter had been used. The electrode was then rinsed with ultrapure water and dried at room temperature. All the experiments were done in three electrode setups: plastic chip electrode as working, Pt wire as a counter and Ag/AgCl (sat. KCl) as a reference electrode and measured by Metrohm Autolab 203 potentiostat/ galvanostat. The GOx@ZIF8 (AuNPs) slurry was prepared by taking 1 mg of material in 200 μL of pH 7.4 buffer and further sonicated to 10 minutes. 5 μL 0.5 % nafion is added to the mixture as a binder.

3. Results

The morphology of GOx@ZIF-8(AuNPs) was examined by field-emission scanning electron microscopy (FESEM). Fig. 2(A) represents assembled star shaped morphology of ZIF-8 microstructure at low resolution. Whereas high resolution FE-SEM image

shows rod assembled star shaped morphology (Fig. 2(B)). GOx has definitely played a crucial role in controlled morphology as GOx has an affinity towards imidazole containing building block arises from intermolecular Hbonding and hydrophobic interaction.

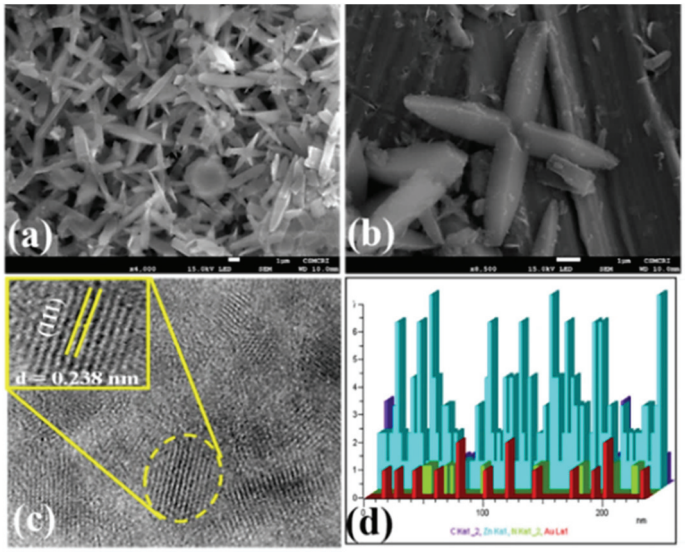


Fig. 1. FESEM image of 5 nm gold coated GO_x@ZIF-8(AuNPs) (a) Crystalline growth (b) Single particle showing large surface area (c) High magnification HRTEM image of Au lattice fringes (d) TEM-EDX line profile of Au showing almost equal distribution.

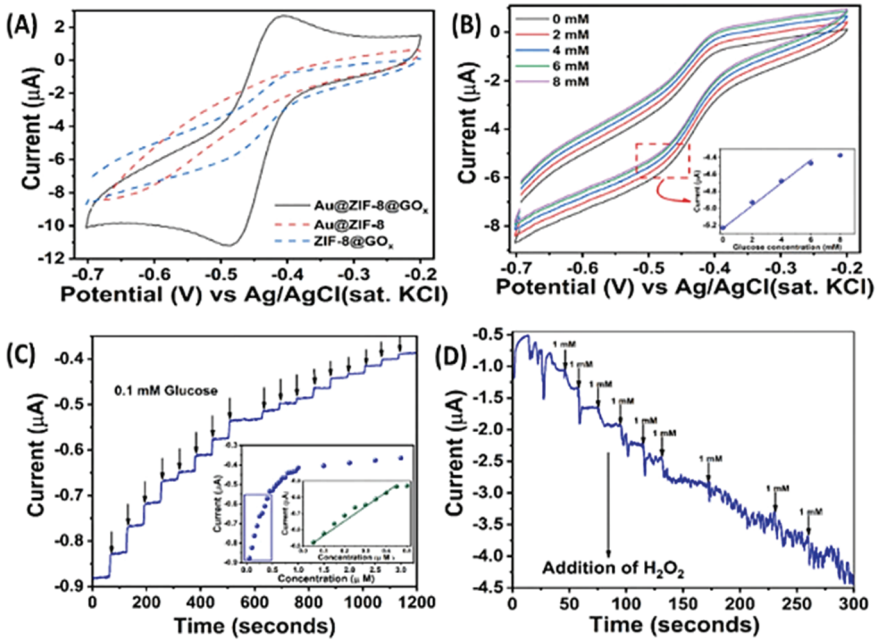


Fig. 2. (A) CV comparison of Au@ZIF-8@GOx, Au@ZIF-8, ZIF-8@GOX showing better faradaic response for Au@ZIF-8@GOx (B) glucose monitor from 0-8 mM (calibration inset) (C) Glucose amperometry with addition of 0.1 mM glucose successively (calibration inset) (D) H_2O_2 amperometry with addition of 1 mM H_2O_2 successively.

Further, HR-TEM was performed for detailed investigation of the synthesized microstructure and was depicted in Fig. 2(C). Electrochemistry of GOx@ZIF-8(AuNPs) produced sharp redox peak as a result of electron transfer of FAD/$FADH_2$ species as shown in figure 2. We had explored the electroctalytic activity of GOx@ZIF-8(AuNPs) vividly and for this purpose we had done CV vs Ag/AgCl (sat. KCl) in air saturated PBS pH 7.4 buffer and the glucose concentration is increased from 0 to 8 mM (Fig 2(B)). The increment of cathodic peak current had been correlated with the concentration of glucose and a linear increment has been found which depicts good catalytic activity of the composite towards glucose oxidation. The possible electrode reaction of glucose oxidation can be correlated by following equations:

$$\text{Glucose} + \text{GOx-FAD} \rightarrow \text{Gluconic acid} + \text{GOx-FADH}_2$$

$$\text{GOx-FADH}_2 + O_2 \rightarrow \text{GOx-FAD} + H_2O_2$$

The conventional amperometry (potentiostatic) experiment had performed by successive addition of 0.1 mM glucose to the air saturated pH 7.4 buffer solution at a characteristic potential of –0.45 V vs Ag/AgCl (sat. KCl) Detection limit of 50 nM of glucose has been achieved indicating that the glucose from sweat can also be detected. (Fig 2(C)). To get the idea about the activity of the composite towards real environment, CV was taken with air saturated 0.1 M pH 7.4 PBS buffer as electrolyte at a scan rate of 100 mV/S in the range of 0.2 to -0.7 V vs Ag/AgCl (sat. KCl) and compared with N_2 saturated 0.1 M pH 7.4 PBS buffer. The result is depicted in Fig. 2(A). The fact could be established strongly as we had repeated this experiment not by adding glucose but H_2O_2 and we found a characteristic decrease of cathodic current while the successive addition of H_2O_2 at -0.45 V vs Ag/AgCl (sat. KCl). Mechanism of this process (Fig. 2D)

$$\text{GOx-FAD} + H_2O_2 \rightarrow \text{GOx-FADH}_2 + O_2$$

Various glucometers are available in market and some of the most commonly used glucometers are mentioned in Table 1. On comparison with the commercial glucometers, the proposed sensor has better sensing capabilities and can be used for non-invasive monitoring of glucose.

Table. 1. Most commonly available commercial blood glucometers.

Company name	Mechanism	Measuring range	Invasive/ Non-invasive
CONTOUR NEXT EZ (Bayer Health Care LLC, Diabetes Care)	Quantitative amperometric assay (FAD-glucose dehydrogenase)	20 to 600 mg/dL	Invasive
ACCU-CHEK Aviva Plus Blood Glucose Monitoring System (Roche Diagnostics)	Quantitative amperometric assay, glucose dehydrogenase (mutant GDH- PQQ)	20 – 600 mg/dL	Invasive
FreeStyle Lite and FreeStyle Freedom Lite Blood Glucose Monitoring Systems (Abbott Diabetes Care, Inc.)	Quantitative coulometric assay, glucose dehydrogenase (GDH-FAD)	20-500 mg/dL.	Invasive

4. Conclusions

Thus, the detection of glucose by prepared GOx@ZIF-8(AuNPs) is a promising method for the development of next generation non-invasive point of the care glucose sensor device.

References

[1]. D. R. Whiting, L. Guariguata, C. Weil, J. Shaw, IDF diabetes atlas: global estimates of the prevalence of diabetes for 2011 and 2030, *Diabetes Research and Clinical Practice,* Vol. 94, pp. 311-321.

[2]. S. Chatterjee, K. Sengupta, S. Bandyopadhyay, A. Dey, Ammonium tetrathiomolybdate as a novel electrode material for convenient tuning of the kinetics of electrochemical O_2 reduction by using iron–porphyrin catalysts, *Journal of Materials Chemistry A,* Vol. 4, 2016, pp. 6819-6823.

[3]. S. Bharathi, M. Nogami, A glucose biosensor based on electrodeposited biocomposites of gold nanoparticles and glucose oxidase enzyme, *The Analyst*, Vol. 126, 2001, pp. 1919-1922.

[4]. W. Luo, C. Zhu, S. Su, D. Li, Y. He, Q. Huang, C. Fan, Self-catalyzed, self-limiting growth of glucose oxidase-mimicking gold nanoparticles, *ACS Nano,*, Vol. 4, 2010, pp. 7451-7458.

[5]. Z. Da Gao, J. Guo, N. K. Shrestha, R. Hahn, Y. Y. Song, P. Schmuki, Nickel hydroxide nanoparticle activated semi-metallic TiO(2) nanotube arrays for non-enzymatic glucose sensing, *Chemistry - A European Journal*, Vol. 19, 2013, pp. 15530-15534.

[6]. J. Wang, Glucose biosensors: 40 years of advances and challenges, *Eletcroanalysis, Vol. 13*, 2001, pp. 983-988.

[7]. Q. Zhao, S. Chen, H. Huang, L. Zhang, L. Wang, F. Liu, J. Chen, Y. Zeng, P. K. Chu, Colorimetric and ultra-sensitive fluorescence resonance energy transfer determination of H_2O_2 and glucose by multi-functional Au nanoclusters, *The Analyst,* Vol. 139, 2014, pp. 1498-1503.

[8]. A. J. Bandodkar, W. Jia, C. Yardimci, X. Wang, J. Ramirez, J. Wang, Tattoo-based noninvasive glucose monitoring: a proof-of-concept study, *Analytical Chemistry*, Vol. *87*, 2015, pp. 394-398.

(044)

Dynamic Threshold Compensated Organic Rectifier for RFID Applications

G. H. Ibrahim [1,3], U. Zschieschang [2], H. Klauk [2] and L. Reindl [1]
[1] University of Freiburg, Electrical Instrumentation Laboratory, Freiburg, Germany
[2] Max Blanck Institute for Solid State Research, Stuttgart, Germany
[3] Electronics Research Institute, Giza, Egypt
E-mail: ghada.ibrahim@frias.uni-freiburg.de

Summary: In this paper, experimental results of several dynamic threshold compensation rectifier circuits are shown. All rectifier circuits are built using a low voltage organic thin film transistor technology (OTFT), using only p-devices, the semiconducting organic material is a Dianapthothienothiophene (DNTT). The circuits are implemented using a low temperature process that enables using flexible Polyethelene Naphthalate (PEN) substrates. While rectifier circuits are meant for operation at 13.56 MHz, which is far beyond the extrinsic cutoff frequency of the used devices, the provided rectified voltages were up to 19 % lower than their peak rectified voltages, showing excellent Quasi-Static Regime operation.

Keywords: Rectifier, Organic TFT, Flexible electronics, RFID, Threshold compensation.

1. Introduction

Rectifiers has been a subject of continuous research because of their significant role in various applications and several waves of emerging technologies. While their traditional role was as a first block in any RFID device, they now contribute to wireless power transfer systems as key enabler to complete automation and autonomous operation of all kinds of smart devices. Flexibility, as another needed aspect in today's low cost and/or wearable wireless applications, has received a major interest. Organic Thin Film Transistors (OTFT), have provided a possible route for achieving needed flexibility. This comes from the fact that the whole OTFT device is fabricated using a low temperature process, which translates to the possibility to use polymer substrates with thickness down to 50 µm.

Nest subsections will give an overview of used OTFT technology as well as previous developments in CMOS rectifiers and organic rectifiers.

1.1. OTFT Technology

Some of the required functional specifications in the targeted OTFT technology to suit the implementation of RFID circuit blocks are the operating speed, large current drive, low leakage and low threshold voltage. The proposed OTFT technology in [1] offers better performance measures where threshold voltages as low as 1 V and supply voltages as low as 3.3 V and reduced channel lengths to 0.8 µm, leveraging device's f_T.

Targeting an organic TFT technology eliminates the possibility of using active rectifiers because they introduce higher complexity which slows down the rectifier and reduce their frequency range of operation, which is quite limited in our case. It is already known that passive solutions offer an advantage of being suitable for higher input frequencies [2].

1.2. Earlier Flexible Rectifiers

Reported flexible RFID tag [3], used a 4 stage first order, static, threshold voltage compensation scheme, to reduce threshold voltage effects, while using mostly P type transistors and a single N type transistor, due to the known superiority of P type over N type devices in all current OTFT technologies. In [4], it has been shown that static threshold compensation results into increased inverse leakage current, while dynamic threshold compensation (referred as differential drive rectifier/active Vth cancellation in [4]), dynamically changes the effective Vth of the diode connected transistors in forward/reverse bias conditions to reduce leakage current and improve power conversion efficiency.

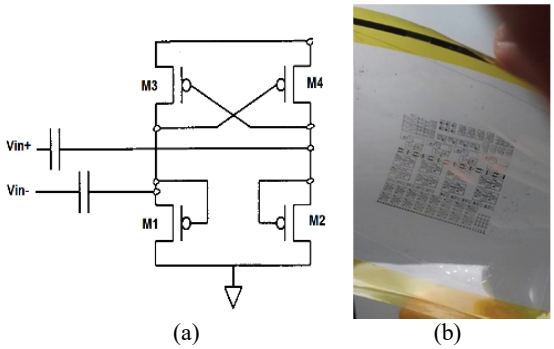
2. Rectifier Implementation

In our work we have adopted an all P type device, differential rectifier, shown in Fig. 1(a), several rectifier cells with different transistor widths from 60 µm to 200 µm and a length of 10 µm were fabricated using cheaper shadow polyimide masks, with one stage and stacked two stages for voltage multiplication. A single stage rectifier cell has an area of 2.8×2.7 mm^2, while the cascaded two stages rectifier cell has an area of 6.0×3.7 mm^2. A photo for fabricated flexible rectifiers is shown in Fig. 1(b).

3. Measurement Results

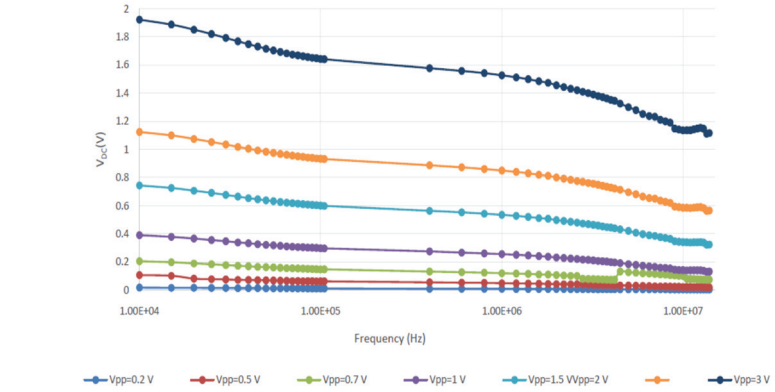
All rectifier cells we characterized over frequency range of 10 KHz up to 14 MHz, and input voltages from 200 mV to 3 V (The maximum permissible

voltage due to thin gates of OTFTs), rectified voltages are reported as open circuit voltage and under 1 MΩ loading conditions. Results of the set of rectifiers of OTFT size of 120 μm/10 μm are reported, where coupling capacitors (see Fig. 1(a)) are implemented as 120 μm × 120 μm MIM capacitors. Fig. 2(a) shows open circuit rectified voltage of a diode connected transistor, Fig. 2(b) shows open circuit rectified voltage of a single stage differential rectifier, Fig. 2(c) shows the rectified voltage of the single stage rectifier under 1 MΩ loading condition, while Fig. 2(d) shows open circuit rectified voltage of a two stages stacked rectifier.

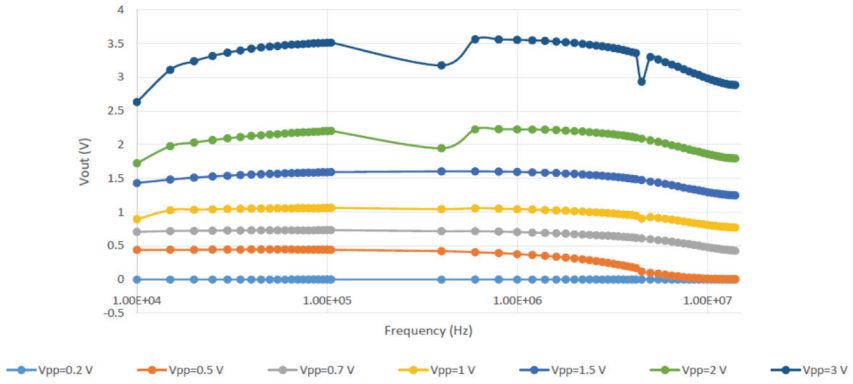


(a) (b)

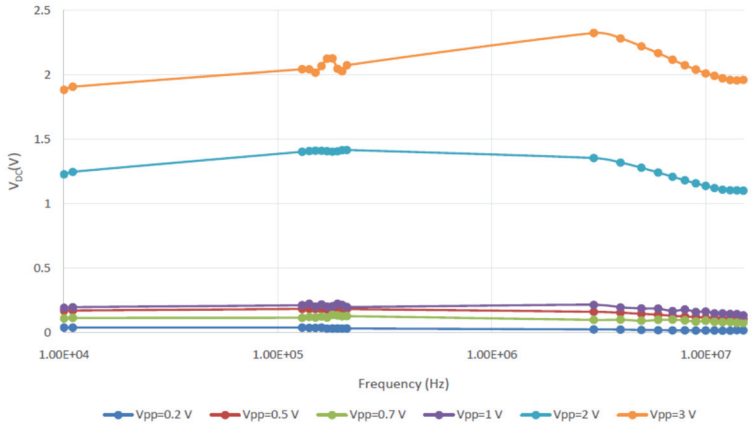
Fig. 1. (a) differential rectifier stage, (b) photo.



(a)

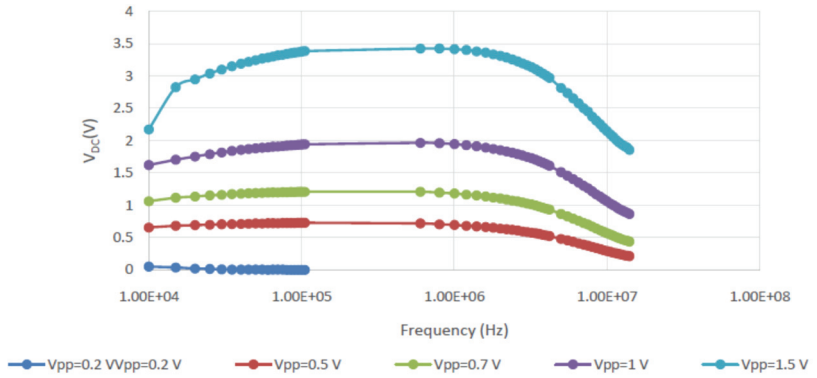


(b)



(c)

Fig. 2 (a-c). Rectified voltage (a) Diode connected device; (b) single stage; open circuit voltage, (c) single stage, 1 MOhm load,



(d)

Fig. 2 (d). Rectified voltage (d) stacked two rectifier stages, open circuit voltage.

4. Conclusions

Successful flexible rectifiers with improved frequency response has been demonstrated, while using low resolution polyimide masks of 10 μm. Targeting rectifier circuits using Si stencil masks would offer considerably improved frequency response and allowing higher complexity for better efficiency.

Acknowledgements

The research leading to this results has received funding from the People Programme (Marie Curie Actions) of the European Union's Seventh Framework Programme (FP7/2007-2013) under REA grant agreement n° [609305].

References

[1]. U. Zschieschang, et al., Dinaphtho [2,3-b:2′,3′-f] thieno [3,2-b] thiophene (DNTT) thin-film transistors with improved performance and stability, *Organic Electronics*, Vol. 12, Issue 8, August 2011, pp.1370-1375.

[2]. C. Peters, J. Handwerker, D. Maurath, Y. Manoli, A Sub-500 mV highly efficient active rectifier for energy harvesting applications, *IEEE Transactions on Circuits and Systems I*, Vol. 58, Issue 7, July 2011, pp. 1542-1550.

[3]. V. Fiore, P. Battiato, S. Abdinia, S. Jacobs, I. Chartier, R. Coppard, G. Klink, E. Cantatore, E. Ragonese, G. Palmisano, An integrated 13.56-MHz RFID tag in a printed organic complementary TFT technology on flexible substrate, *IEEE Transactions on Circuits and Systems I*, Vol. 62, Issue 6, June 2015, pp. 1668-1677.

[4]. K. Kotani, A. Sasaki, T. Ito, High-efficiency differential-drive CMOS rectifier for UHF RFIDs, *IEEE Journal of Solid-State Circuits*, Vol. 44, Issue 11, November 2009, pp. 3011-3018.

Sponsored by:





Journal of
Low Power Electronics and Applications
an Open Access Journal by MDPI



micromachines
an Open Access Journal by MDPI



sensors
an Open Access Journal by MDPI