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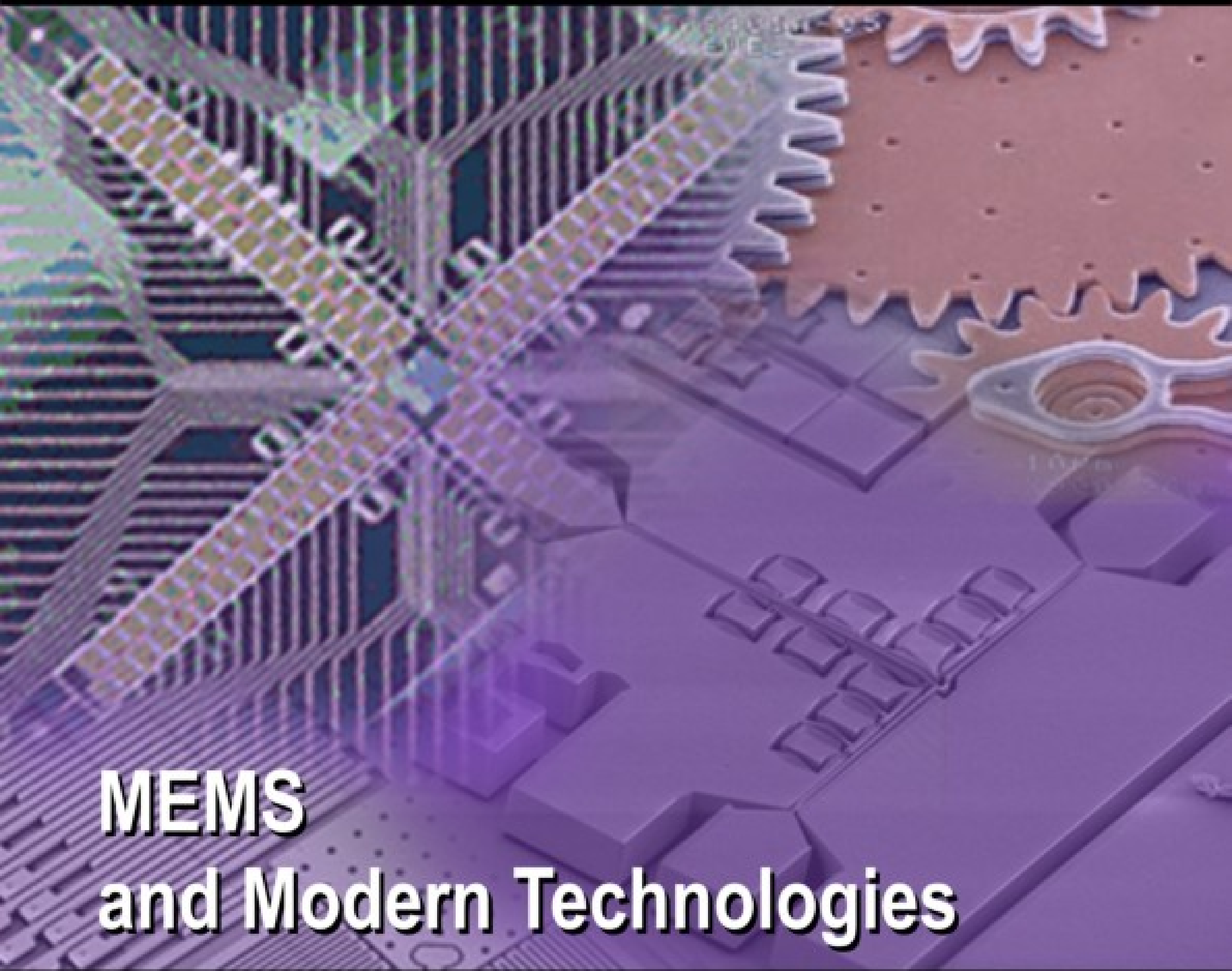

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Design and Fabrication of High Sensitive Piezoresistive MEMS Accelerometer

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Abstract: This paper addresses the design and fabrication of high sensitive single axis piezoresistive micro-accelerometer for 50 g application. MEMS based accelerometer structure comprise of flexure fixed at one end and having attached proof mass at other end. This structure is designed and simulated using Coventorware. The simulation results show the sensitivity of 4 mV/g. The structure is fabricated in N type silicon (100) substrate using Silicon bulk micromachining. This paper also discuses the use of PECVD Si_3N_4 layer as a masking material for silicon micromachining and process flow for accelerometer. *Copyright © 2008 IFSA.*

Keywords: Micro-accelerometer, Bulk micromachining

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1. Introduction

The micro-accelerometer is one of the important types of inertial sensor. The MEMS accelerometer is in extensive use in automobile, air-bag system, Crash Detection chassis dynamics, defense, aerospace and INS-GPS system [1-4]. Many transudation mechanism are available and reported for detecting the deflection of proof mass, such as piezoresistive [1], capacitive [5], piezoelectric [1] etc. Piezoresistive accelerometer is having easy fabrication process, simple signal conditioning advantages on other counterpart [4].

Roylence and Angel published first piezoresistive accelerometer. Simple cantilever based geometry was proposed by Roylence [3], which followed by different geometrical structures by researcher worldwide [6, 7]. The use of multi beam attached proof mass is demonstrated [8, 9]. The use of T shaped beam for accelerometer measurement is investigated by Hong Chen and group [2]. The use of mass attached to center of diaphragm for accelerometer measurement is also reported [10].

In this present work, we proposed a simple geometry of a cantilever fixed at one end having attached mass at other end. The sensitivity improvement is achieved by changing proof mass volume. The design is modulated using CoventorWare for sensitivity, natural frequency and resistance change.

The design structure was fabricated in Silicon (Si) n type (100) wafer using Silicon bulk micromachining. The Silicon On Insulator (SOI) is a preferred choice for such fabrication [11]. But unavailability of this substrate forces to use the Silicon substrate. The time dependant etch stop was used to create the structures in silicon. The Plasma Enhance Chemical Vapor Deposition (PECVD) Si_3N_4 layer was used as masking material for the Silicon micromachining. The masking material selection is based on low temperature processing. The Masking behavior of PECVD Si_3N_4 is discussed and results are compared with the reported data. The fabrication flow for micro accelerometer is discussed in later section.

2. Design

The microaccelerometer structure consists of a flexure fixed at a one end and having attached mass at other end. The basic mechanism of this accelerometer has a piezoresistive sensing element of value 4.5 KΩ implanted on a flexure. It is connected with three resistors of same value in Whetstone Bridge as shown in Fig. 1.2.

The dimensions of flexure and proof mass are (L x W x t) 100 x 65 x 25 μm and 2000 x 1000 x 225 μm respectively.

Piezoresistance is a phenomenon referring to a change in resistance caused by the change in bulk resistivity (ρ) of the material when subjected to mechanical stress. The resistance of a planar strip resistor as shown in Fig. 1.1 is $R = \rho\ (l /(w\ h))$; where ρ is the resistivity and l, w, and t are the length, width and thickness of the resistor respectively. The change in resistance `R' can be written in terms of strain and poison's ratio 'ρ ' as:

$$\frac{\Delta \mathrm{R}}{\mathrm{R}} = \frac{\Delta\rho}{\rho} + \varepsilon(1+2\nu) \tag{1}$$

We know that $\{\vec{E}\} = [\rho]\{\vec{J}\}$, where $\vec{E}$ and $\vec{J}$ are vectors that represent electric field and current density respectively. The relationship between the resistivity change$(\Delta\rho)$, current density and the stress components can be written as [12]

$$[\rho\ ] = \rho_o[I] + \rho_o[\Delta], \tag{2}$$

where Δ is a tensor of second rank determined by piezoresistive coefficients, as $\Delta = [\pi]\ \{\sigma\}$. Using equation (1), (2) and relationship between electric field and resistivity, change in resistivity in different directions can be written as (neglecting the effect of shear stresses)

$$\frac{\Delta\rho_{\mathrm{xx}}}{\rho} = \pi_l\sigma_{xx} + \pi_t\{\sigma_{yy} + \sigma_{zz}\} \tag{3}$$

$$\frac{\Delta\rho_{yy}}{\rho} = \pi_l\sigma_{yy} + \pi_t\{\sigma_{xx} + \sigma_{zz}\} \tag{4}$$

$$\frac{\Delta\rho_{zz}}{\rho} = \pi_l\sigma_{zz} + \pi_t\{\sigma_{yy} + \sigma_{xx}\} \tag{5}$$

Using equations (1) to (5), neglecting the resistance change due to geometry variation and if α is temperature coefficient of resistivity, we can write the relative change in resistance ($\Delta R/R$) as:

$$\frac{\Delta R}{R} = \pi_l\sigma_l + \pi_t\sigma_t + \alpha T \, , \tag{6}$$

where 'π_l' and 'π_t' are longitudinal and transverse piezoresistive coefficients and are related gauge factors as (Robert A.F et al 2000)

$$\pi_l = \frac{G_l - 2G_t\nu}{E} \text{ and } \pi_t = \frac{G_t(1-\nu) - G_l\nu}{E} \, , \tag{7}$$

where E is young's modulus and G_l, Gt are lateral and traverse gauge factors [13].

The design is simulated for maximum stress, maximum deflection, and natural frequency using MEMMech solver and for resistance change using MEMPZR solver. The design detail is published elsewhere [14]. The resistance design value is kept 4.5KΩ.

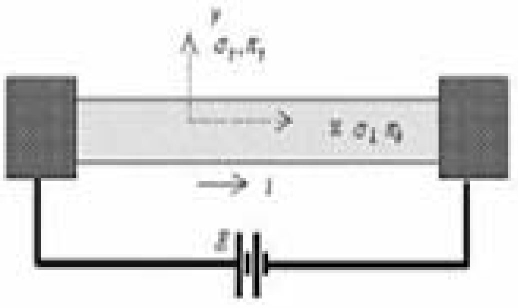


Fig. 1.1. Piezoresistor.

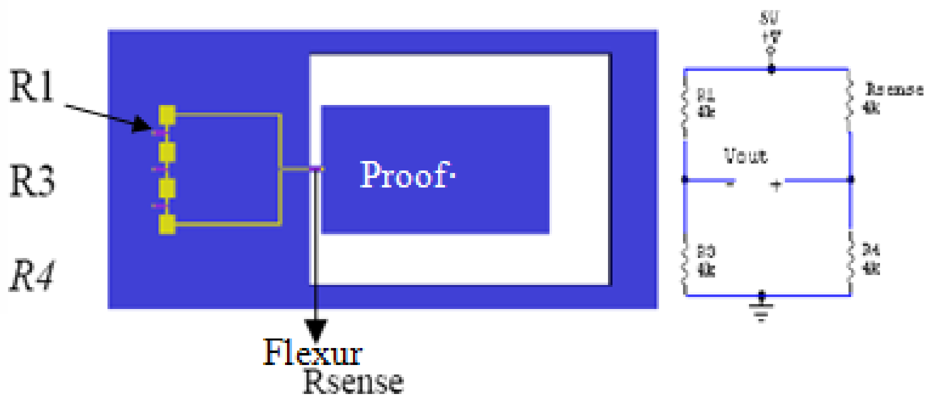


Fig. 1.2. Micro-accelerometer.

3. Fabrication

The design presented has consists of a piezoresistive sensing element implanted on flexure and a proof mass. The structure is realized using 6 masks and silicon bulk micromachining (SBM) technique. The PECVD silicon nitride is used as a masking material for SBM process.

3.1. Micro-Accelerometer Fabrication

Fabrication of accelerometer was started with N type, 3” diameter, double sided (100) silicon (225 um thick) wafer (Fig. 2). The fabrication process started with the initial oxidation of n type <100> silicon wafer for 0.55 µm step b). The SiO_2 layer on topside is patterned to open the window for P+ layer diffusion.

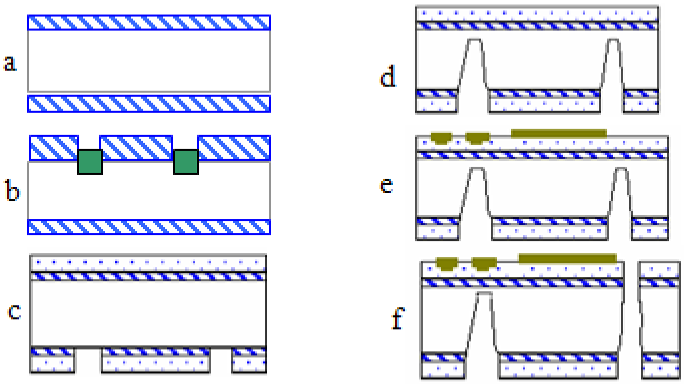


Fig. 2. The fabrication process for microaccelerometer.

The P+ layer is formed on top surface using silane and diborane gases in APCVD system. This deposited P+ layer was diffused at 1100 C, 40 min in N_2O_2 atmosphere in order to get 2.5 µm depth. The thermally re-grown SiO2 during P+ diffusion was patterned to open window for boron implantation. The four resistors windows were opened in order to fabricate for resistor on a device. The piezoresistors are formed by Boron ion implantation and diffusion. The boron dose of 5 e ^{14} ion/cm^2 is implanted d at energy of 80 KeV. The implanted boron atoms are diffused to 2 µm depth (step b). The masking layer of PECVD Si_3N_4 is deposited on both side of wafer and patterned using RIE system (step c). The Si is etched for 175 µm from back side (step d).This is discussed in detail in next section.

The implanted four resistors are connected in Wheatstone bridge using gold metallization. The Au layer is deposited by e-beam method and patterned using potassium iodide (Ki) (step e). The gold material is selected as its having etched resistance to KOH [15].

The Si_3N_4 layer was patterned form top surface to expose silicon surface. The Silicon is selectively etched from both side of silicon wafer till structure gets released (step f).

3.2. PECVD Si_3N_4 Layer Deposition

Plasma Enhanced Chemical Vapor Deposition (PECVD) deposits silicon nitride (Si_3N_4) on thermally grown SiO_2 deposited silicon wafer. The Si_3N_4 deposition condition is carried out at pressure

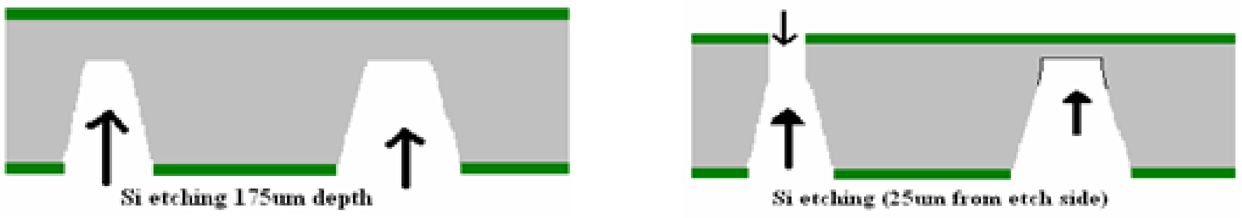
200 mtorr, with SiH_2Cl_2: NH_3 gases flow ratio of 1: 3. The deposition temperature is constant at 300 ˚C. Film deposited was carried out for thickness 100nm. The refractive index of the film was measured to be 1.96. The deposited layer is patterned using Conventional lithography and CHF_3 plasma in RIE.

3.3. Silicon Bulk Micromachining

The Silicon bulk micromachining (SBM) is carried out using Potassium Hydroxide (KOH) solution. The etchant temperature is maintained at 70 ˚C for Si etching experiment. With this set up silicon etching rate of 40 µm/hr was observed. The SBM is carried out in two steps in order to achieve different in thickness of flexure and proof mass.

In first step, the silicon wafer is etched for 175 µm from backside. During this process, PECVD Si_3N_4 is used as a masking material for silicon etching. The Fig. 3A shows the 175 µm bulk micromachined silicon wafer. During this step, proof mass is realized in structure.

During second step of micromachining, the Si selectively etched for 25 µm from both side of wafers. This step is designed in such a way that it will give a desired thickness flexure as well as accelerometer structure release. This is very crucial step in accelerometer fabrication. During this step, the sputtered gold and PECVD Si_3N_4 layers plays role of masking material. Fig. 3B shows the accelerometer after two-step micromachining.



(A) (B)

Fig. 3. (A) Si etching for 175 µm, (B) Si etching for 25 µm.

During two-step bulk micromachining, the 225 µm Si wafer is etched for depth 'd' = 200 µm from back side and 25 µm from front side. The convex corner compensation is employed to avoid the corner etching. The design for corner compensation is taken from reported data by Wei Fan et al [16].

4. Results and Discussion

4.1. Sensitivity

The structure was simulated for application of 50 g acceleration. The simulations results show that the maximum stress of 280 Mp was generating on the flexure while the maximum deflection was 200 µm. The Fig. 4.1 shows the simulated stress variation on flexure. The maximum stress on flexure was 280 Mp and it is below the value of micromachined Si fracture limit of 300 Mp [17].

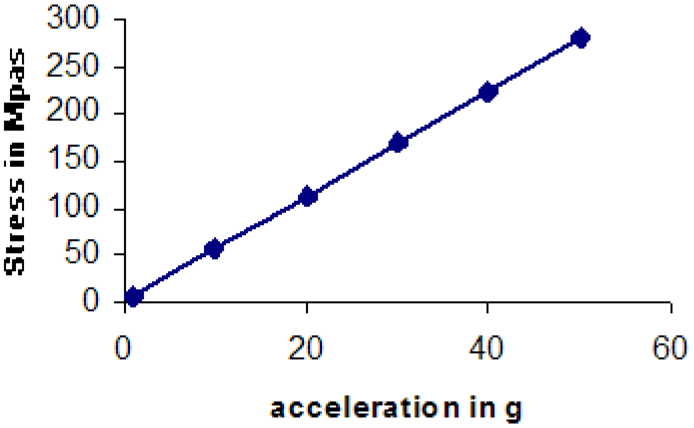


Fig. 4.1. Stress variation on flexure w.r.t applied acceleration.

Applying the 5 V dc to whetstone bridge structure did the sensitivity simulation. It shoes the device sensitivity of 4 mV/g, which is in good acceptable range.

The simulated and analytical natural frequency of structure was 485 Hz.

4.2. Masking Behavior of PECVD Si_3N_4 Layer

The PECVD Si_3N_4 layer of thickness 100 nmis deposited and patterned as discussed in previous section. This layer was subjected KOH. The trial is carried out for 330 min. The 300 min etching time is needed for making through hole in silicon wafer. Thus the masking capability is tested for more time i.e.330 min. The Si_3N_4 layer is inspected under high-magnified scope (100X). The pinhole free Si_3N_4 is observed. There is no pitting problem observed on Si_3N_4 layer. The Si_3N_4 thickness measurement is done after micromachining, which shows 68 nm thickness, there are 6 nm/ hr etching of Si_3N_4. This is in good agreement with reported data [18-20]. The Fig. 4.2 shows SEM of Si_3N_4 top surfaces after 225 µm etching. This is a promising result. It shows that the PECVD Si_3N_4 is good alternate and low temperature masking material to LPCVD Si_3N_4 for application of like 300 µm Si micromachining.

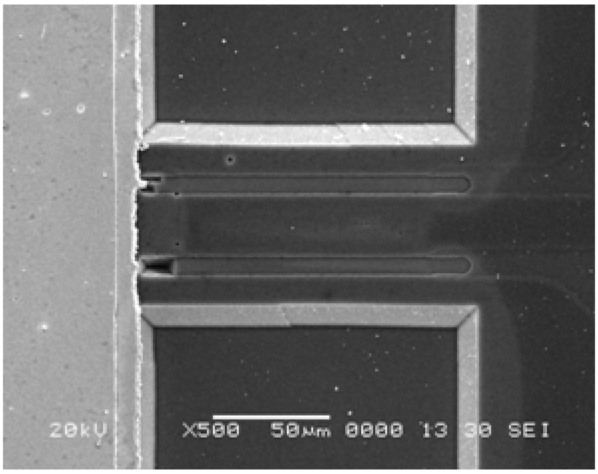


Fig. 4.2. Si_3N_4 surface after 300 min SBM.

4.3. Fabrication of Micro-Accelerometer

The sheet resistance measurement after P+ diffusion shows the resistivity of 6.7 Ω/φ. The sheet resistivity of boron-implanted silicon is 147 Ω/φ. These results are matching with expected result for resistance fabrication. But there is 5% variation in sheet resistance measurement after boron impartation over the wafer. The final resistance value is measured using the curve tracer (From Tektronix). It shows the value of 4.4 kΩ to 4.6 kΩ. This change in resistance is attributed to variation sheet resistance after boron implantation. The convex corner compensation mask is used for SMB. It is important to avoid the corner etching, which would have reduced the mass and sensitivity of device. The convex corner after 200 μm Si etching is shown in Fig. 4.3. The flexure thickness measurement is carried out using the dektak stylus measurement system. The flexure thickness is 25 μm (±1 μm). The SEM measurements taken after device fabrication .The obtained results are well matching with design value specified in section 2. This implies that the device fabrication is following the design guidelines. The SEM image of fabricated micro-accelerometer is shown in Fig. 4.4.

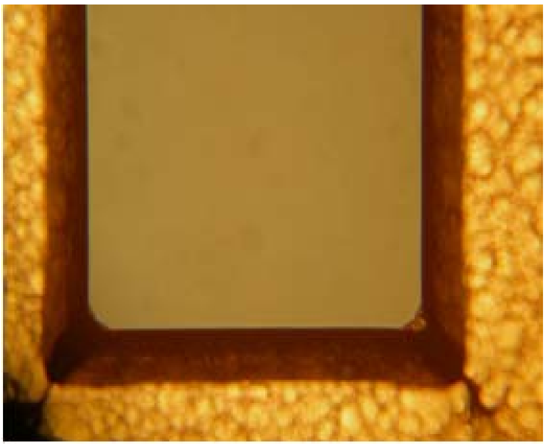


Fig. 4.3. Convex corner after 300min SBM.

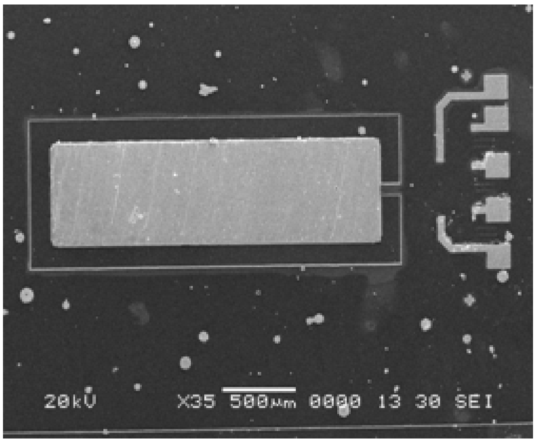


Fig. 4.4. SEM image of fabricated microaccelerometer.

Conclusion

The cantilever based simple design is presented for high sensitive acceleration sensor. The device simulation shows the sensitivity of 4 mV/g without amplification. The Silicon micromachined

Piezoresistive accelerometer fabrication is fabricated using two-step SBM. The convex corner compensation technique is employed successfully to protect the proof mass corners. The desire value of 4.5 kΩ-implanted resistances is achieved. The PECVD Si_3N_4 shows promising masking material capability for 300 min Si etching using KOH.

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Guide for Contributors

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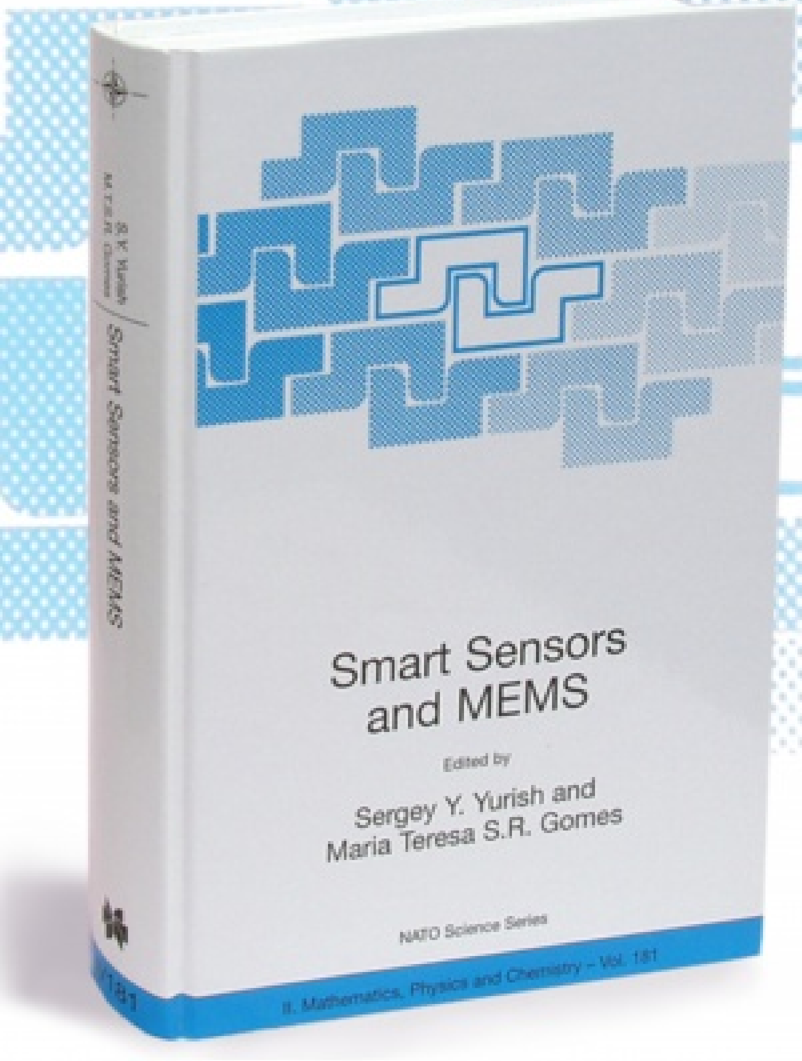
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