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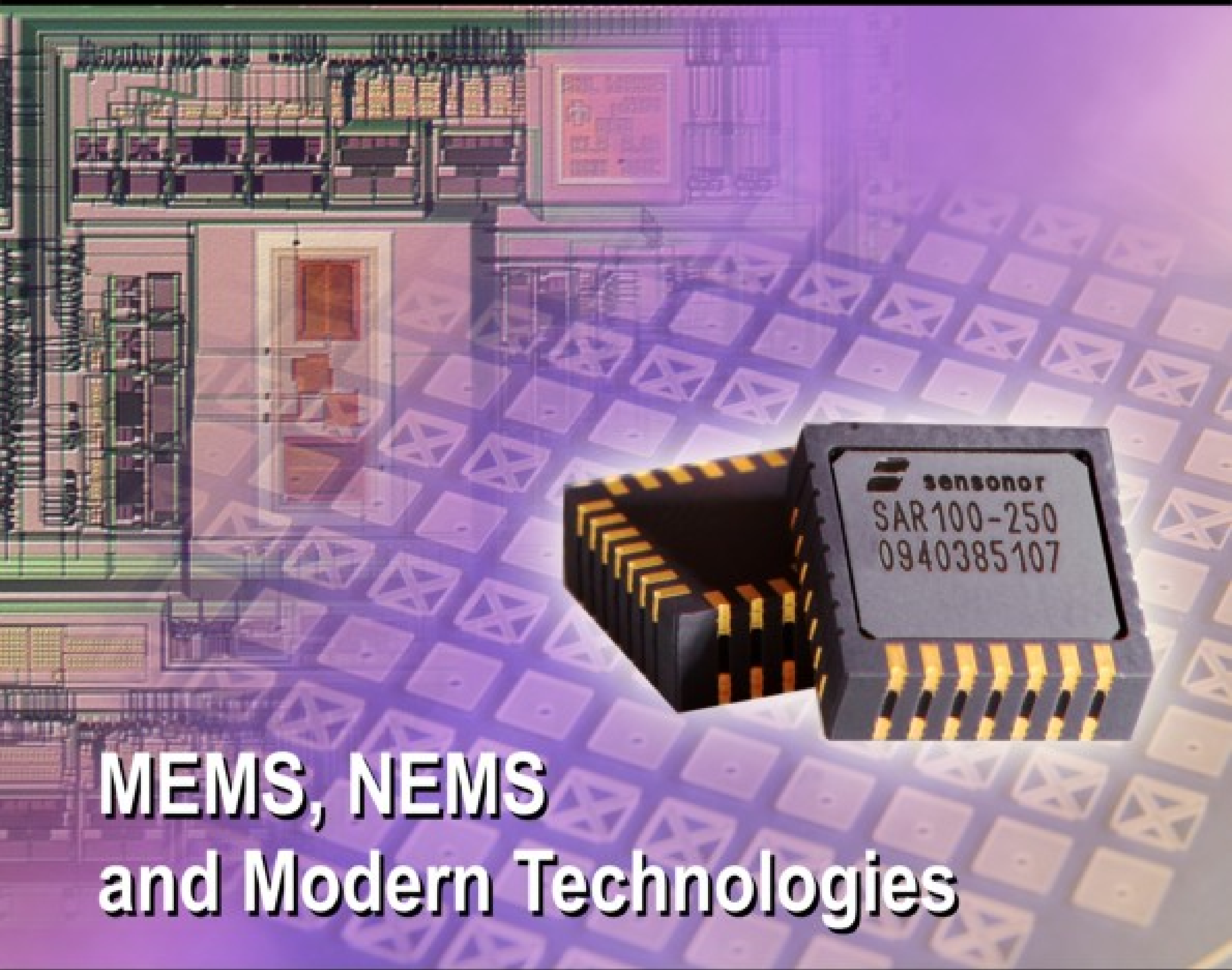

MEMS, NEMS and Modern Technologies

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Fully on-chip High Q Inductors Based on Microtechnologies

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Abstract: Wireless biosensor networks (WBSNs) collect information about biological responses and process it using scattered battery-power sensor nodes. Such nodes demand ultra low-power consumption for longer operating time. Ultra Wide Band (UWB) is a potential solution for WBSNs due to its advantage in low power consumption at reasonable data rate. However, such UBW technology requires high quality (Q) factor passive components. This paper presents detailed analysis, design and optimization of physical parameters of silicon-on-sapphire (SOS) and micro-electro-mechanical-systems (MEMS) inductors for application in UWB transceivers. Results showed that the 1.5 nH SOS inductor achieved Q factor of 111 and MEMS inductor achieved Q factor of 45 at 4 GHz frequency. The voltage controlled oscillator (VCO) designed with SOS inductor achieved more than 10 dBc/Hz reduction in phase noise and consumed half the power compared to VCO with MEMS inductor. Such low power VCO will improve battery life of a UWB wireless sensor node. *Copyright © 2010 IFSA.*

Keywords: High Q inductor, MEMS, Silicon-on-Sapphire, Voltage controlled oscillator, Phase noise

1. Introduction

Technological advancement, miniaturization of electronic devices and progress in ad-hoc network routing protocols and embedded systems have facilitated developments in the field of biosensors and biosensor networks. Biosensor networks are a collection of biosensor units that collect information about biological responses and process it in order to make a decision for a desired outcome. In today's market there is a demand for ultra low power consumption, portability and wireless connectivity from the biosensors for information exchange. Recently, there is advancement in the adaptive communication module that efficiently reconfigures its hardware components according to the changes in operating environment in order to reduce system power consumption and optimally utilize resources. Due to the intelligent wireless communication module, the biosensor unit becomes a state of the art independent system as well as part of a wireless biosensor network (WBSN) [1, 2].

With the above functionality requirements from the various components of the WBSN, ultra low power consumption is the most critical design requirement as the biosensor nodes are battery operated. Every component of the WBSN node has to be designed for low power consumption as it directly affects the system reliability, efficiency and life. In a typical intelligent biosensor node which comprises of a sensing element, signal conditioning circuits, a processing element and a transceiver for communication, more than 50 % of power is consumed by the transceiver, of which 80 % is consumed by the receiver section [3]. This makes the design of the communication module and its receiver section very critical for WBSN applications.

Ultra Wideband (UWB) communication is one of the candidate technologies to be used for WBSN because of its following features:

- Wide bandwidth of over 8 GHz; from 0-960 MHz and 3-10.6 GHz
- Unlicensed communication with limited transmit power in above bands
- Capacity to achieve low to extremely high data rates at 30 m to 2 m distances respectively
- Potential for location tracking and precision ranging

To achieve higher data rates the 3-10.6GHz band of UWB communication must be used. Receiver designs in this band have voltage controlled oscillator (VCO) as one of the highest power consuming blocks. High quality (Q) factor passive components such as inductor are the critical requirements in the design of VCO with low power consumption [4,5]. However, on chip inductors are the bottleneck in achieving the optimum performance due to their low Q factor. The low Q factor of on-chip inductors is mainly due to the substrate losses caused by the eddy currents and inductor coil series resistance. The growing research in radio frequency (RF) systems based on alternative advanced technologies such as Silicon-on-Sapphire (SOS) and micro electro mechanical systems (MEMS) indicate that these technologies have the potential to provide a on-chip high Q inductor required in such RF systems [6,7]. To explore possible solutions for this bottleneck SOS and MEMS technology are investigated in this paper.

MEMS is an enabling technology and can replace most of the off-chip components in a receiver [4]. MEMS technology achieves high performance, miniaturized passive components by performing post processing steps on standard fabrication process to reduce the losses in substrate and optimizes the layout parameters such as outer dimensions, width and spacing of the metal tracks, thickness of the metal and number of turns of an inductor [6]. However, this requires post processing steps which increase the cost of end product. Recently reported SOS technology, a variant of silicon-on-insulator technology, offers high resistivity substrate that has ability to considerably improve the quality factors of on-chip passive devices. Using the high resistivity substrate and thick top metal layer in SOS technology, it has been shown that with Q factors of more than 40 can be achieved for high Giga-Hz range of operation [7]. However, further optimizations at layout level can be performed to achieve even higher Q factors.

This paper presents design and optimization of inductors using MEMS and SOS technology. A 1.5 nH inductor is designed using both technologies and a VCO circuit operating at 4 GHz is used as a testbench to investigate the performance improvements due to high Q factor inductors. The paper is organized as follows: section 2 and 3 present modelling, simulation and analysis of MEMS and SOS inductor respectively. Section 4 presents results along with the VCO performance and conclusion are drawn in section 5.

2. MEMS Inductor

The inductor design involves understanding of effects of inductor topological parameters on the Q factor and self resonance frequency of the inductor, design and optimization of inductor topological parameters, choice of orientation and placement to reduce substrate effects and choice of material for fabrication [4]. The design process involves three major design issues namely choice of topology, reduction of substrate effects and modelling the inductor performance into an equivalent circuit that effectively models the above effects.

The modelling and simulation for the MEMS inductor has been done using the Coventorware MEMS software from Coventor Inc. The MEMS inductor is designed using copper as the material on silicon substrate. Fig. 1 shows a 3-Dimentional square spiral inductor, where OD is the outer diameter, AG is the air gap from the substrate, W is the wire width and S is the spacing between the wires of the spiral inductor.

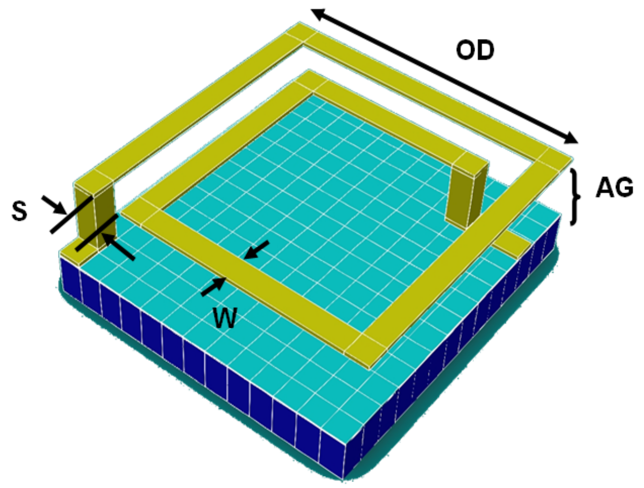

Fig. 1. Structure of the Spiral Inductor.

The inductor has been analyzed for the effect of air gap, metal width and spacing on inductance and Q. The variation of air gap has been fully analyzed, as illustrated in Fig. 2. The result revealed that inductance and Q factor increase when the spiral inductor is suspended from the silicon substrate because of the reduction in substrate losses and parasitic effects of the substrate. Fig. 3 shows the effect of metal width on Q factor and inductance. It can be seen that increasing the metal width reduces the inductance and increases the peak Q factor, this is due to the fact the series resistance decreases with increase in metal width. These effects can be combined in form of equation (1), which shows that the inductance (L) is directly proportional to the air gap (AG) and inversely proportional to the width (W). Hence, 30 µm is an optimum width for this inductor, which minimizes the series resistance and maximizes the Q-factor. From equation (2), it is observed that as for a constant thickness T as W increases, the resistance R decreases:

$$L_0 \propto \frac{AG}{W} \tag{1}$$

$$R = \frac{\rho}{(W \times T)} \quad (2)$$

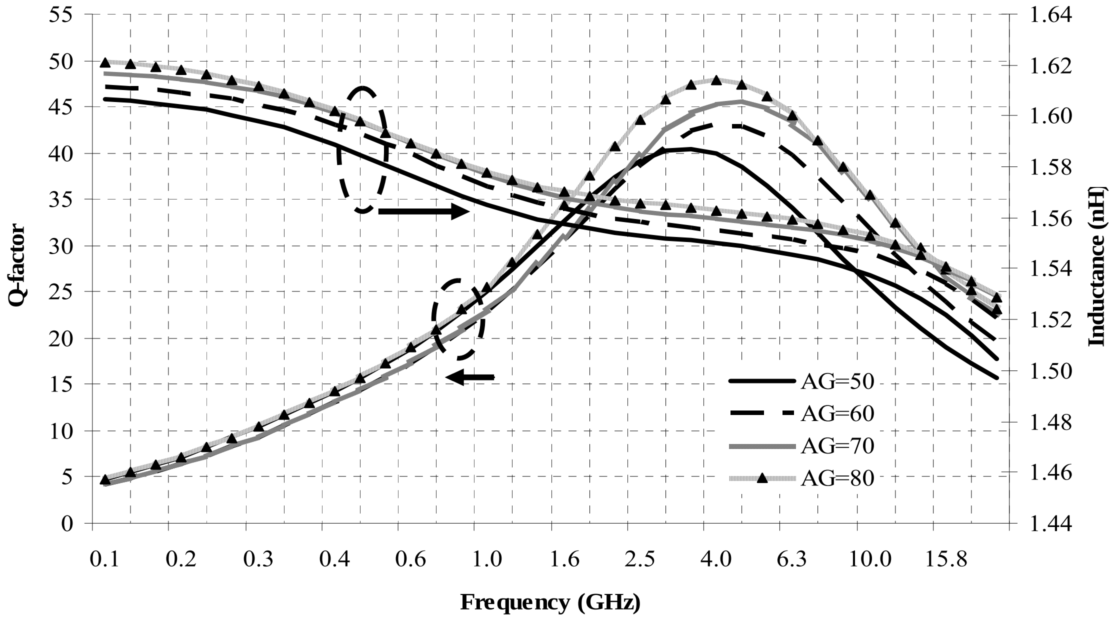

Fig. 2. Effect of Air Gap on Q Factor and Inductance
[Design Parameters: OD=400, W=30, T=5, S=40].

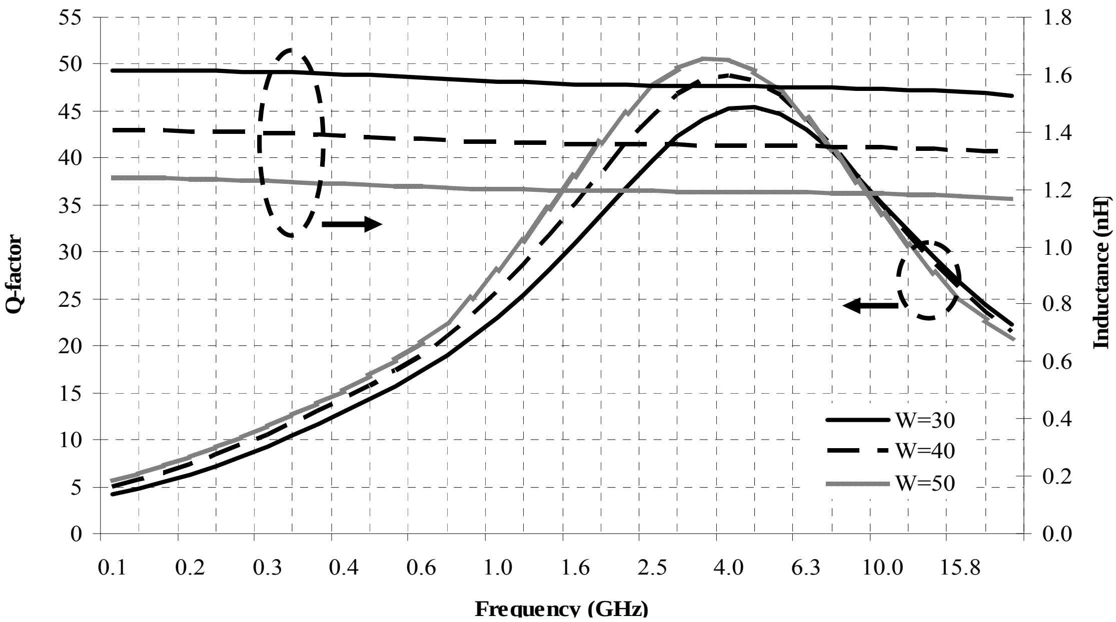

Fig. 3. Effect of Width on Q Factor and Inductance
[Design Parameters: OD=400 μm, S=40 μm, T=5 μm, AG= 70 μm].

The effect of spacing on inductance and Q factor are plotted as Fig. 4. When line spacing increases, it is observed that the inductance of the spiral coil decreases. The increase in spacing results in increase of total spiral length and hence increases the total series resistance. As a result, the Q factor decreases with increase in spacing.

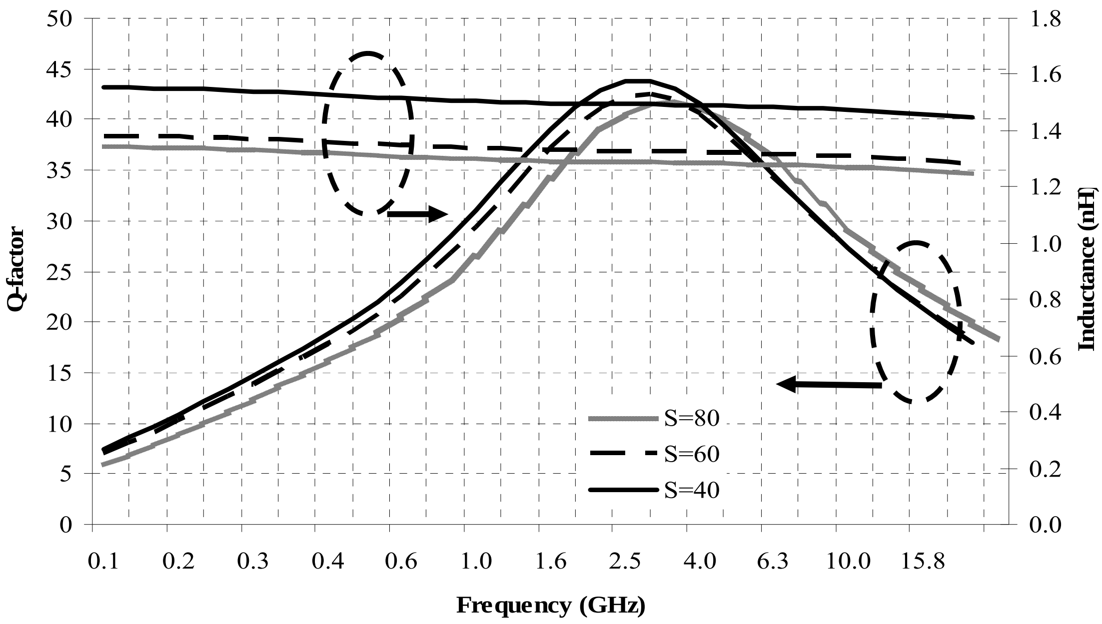

Fig. 4. Effect of Spacing on Q Factor and Inductance
[Design Parameters: OD=400 μm, W=30 μm, T=10 μm, AG=50 μm].

The primary advantage of using MEMS technology is the ability to provide air gap between the substrate and the inductor coil. The introduced air gap results in reduced substrate coupling effects like eddy current losses which has negative impact on inductance and Q factor of the inductor. However, this advantage comes at the cost of extra processing steps which increase the cost of the end product.

Silicon-on-insulator (SOI) technology can provide similar reduction in negative substrate effects due to its inherent advantage of near insulator substrate. Silicon-on-sapphire is a variant of SOI technology that enjoys the advantage of near insulator sapphire substrate while being fabricated using low cost fabrication facilities used for standard bulk CMOS. Hence, this paper also explores the possibility of designing high Q inductors in SOS technology.

3. SOS Inductor

In SOS technology, the inductor can be designed using the top thick metal later (MT). However, parasitic components that are formed in this process will alter the final inductance value and Q of the inductor. Fig. 3 presents the equivalent model of the inductor designed in SOS technology [7], where L is the inductance value, R_s is the parasitic resistance in series with the main inductance, C_P represents the capacitive coupling between the windings of the spiral inductor, L_C and R_C model the low-frequency current-crowding behaviour and R_P emulate the combined crowding and skin-effect behaviour at higher frequencies.

The Q of the inductor can also be given by equation (3), where R_{total} is its total equivalent resistance series with the inductor L at frequency ω:

$$Q = \frac{\omega L}{R_{total}} \tag{3}$$

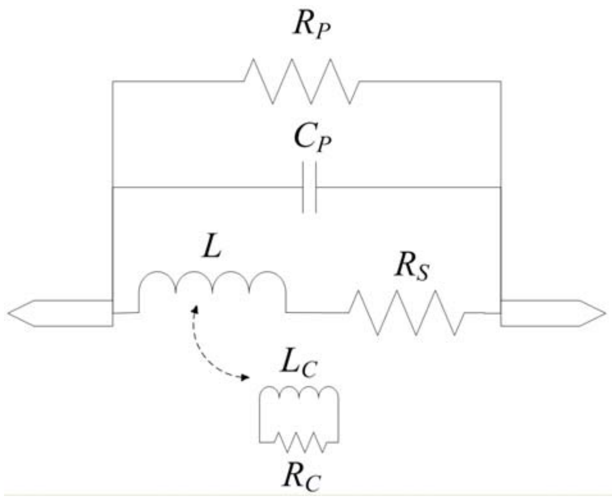

Fig. 5. SOS Inductor Model.

To achieve the highest possible Q all the parasitic components in the above model must be reduced to minimum. Fig. 6 presents the illustration of the inductor's key parameters, which are outer diameter (OD) inner radius (IR), spacing between metal tracks (TS), track width (TW), number of turns (NT) and the substrate material. For substrate material, SOS technology offers a sapphire substrate of 250 µm thickness, which has very high resistivity and is the key advantage of this technology. It is a design challenge now to achieve a significantly large inductance value with the highest Q, by optimizing the other inductor's physical parameters.

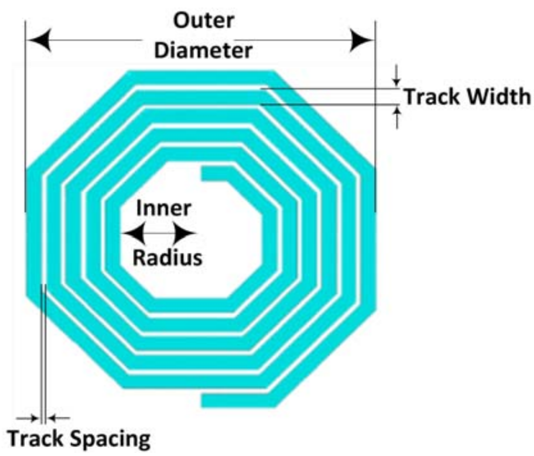

Fig. 6. Inductor Physical Parameters.

Literature describes square-spiral, octagonal-spiral and circular-spiral as some of the preferred inductor topologies [7]. Fig. 7 shows the effects of these topologies on Q factor and inductance values of a single turn inductor designed in SOS technology. It can be seen that the circular-spiral topology has highest Q factor and larger inductance value amongst these three topologies. All inductor designs use a sapphire substrate of 250 µm thickness, Metal-3 as inductor coil and a patterned ground shielding in polysilicon (POLY) layer.

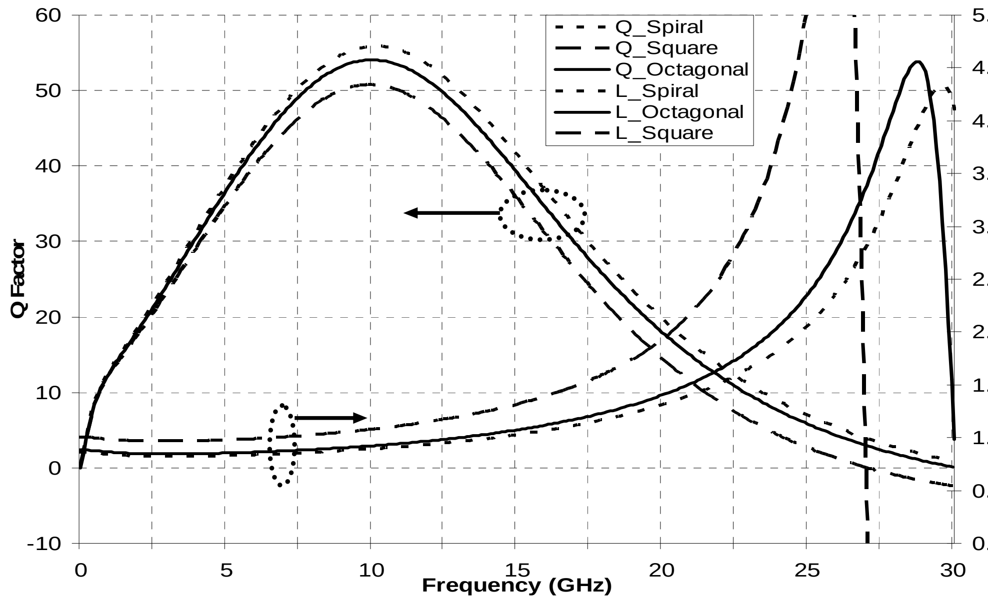

Fig. 7. Effects of inductor's Topologies on Inductance and Q Factor
[Design parameters TW=50 μm, TS=10 μm, IR=150 μm and NT=1].

One of the design challenges is to achieve large inductance value with high Q factor. Sufficiently large inductance can be achieved by increasing the number of turns of an octagonal inductor. However, increasing the number of turns reduces the Q due to the increase in series resistance and parasitic capacitance between the tracks. Increasing track spacing can reduce capacitance between the metal tracks but it will increase the total track length, thus increasing resistance resulting in lower Q. Fig. 8 and Fig. 9 show that increasing the number of turns (NTs) reduces the Q factor due to the increase in series resistance and parasitic capacitance between the tracks.

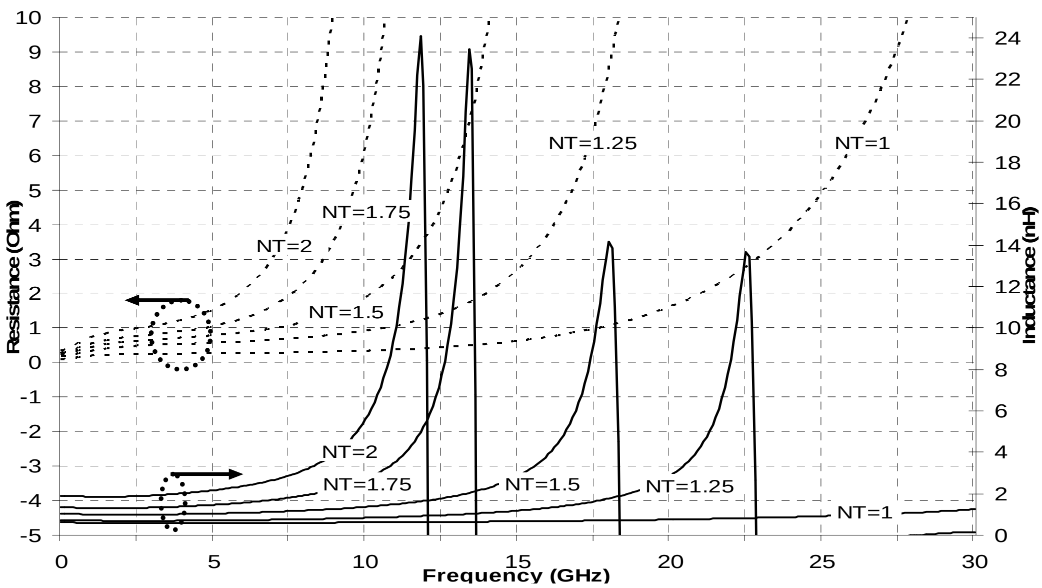

Fig. 8. Effects of NT on Inductance and Series Resistance
[Design parameters TW=100 μm, TS=10 μm and IR=35 μm].

Fig. 8 also shows that a single turn inductor can achieve maximum Q factor with the largest possible operating bandwidth. One of the major reasons for decrease in Q factor with increase in number of turns is because of the parasitic capacitance between the adjacent tracks. This can be reduced by increasing the track spacing. However, the increasing track spacing also decreases the Q factor [8].

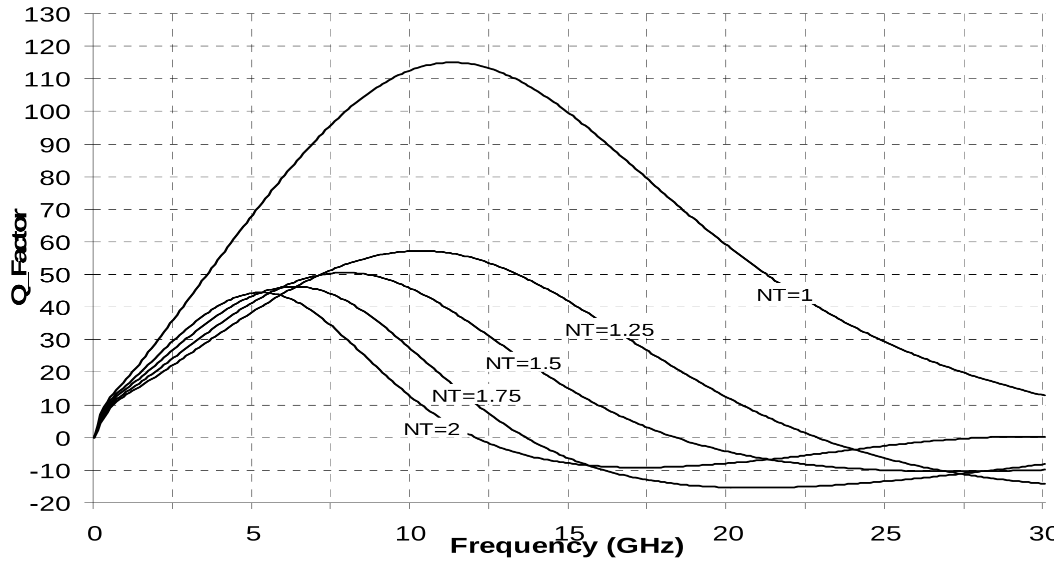

Fig. 9. Effects of NT on Q Factor [Design parameters TW=100 μm, TS=10 μm and IR=35 μm].

The series resistance of the planar coil is related to the sheet resistance of the metal strip, which is inversely proportional to the width of the strip. This shows that there is further possibility of reducing the series resistance by changing the track width. Figs. 10 & Fig. 11 show the effects of track width on series resistance, inductance and Q factor. It can be seen from Fig. 10 & Fig. 11 that larger track width increases the inductance and decreases the self-resonance frequency.

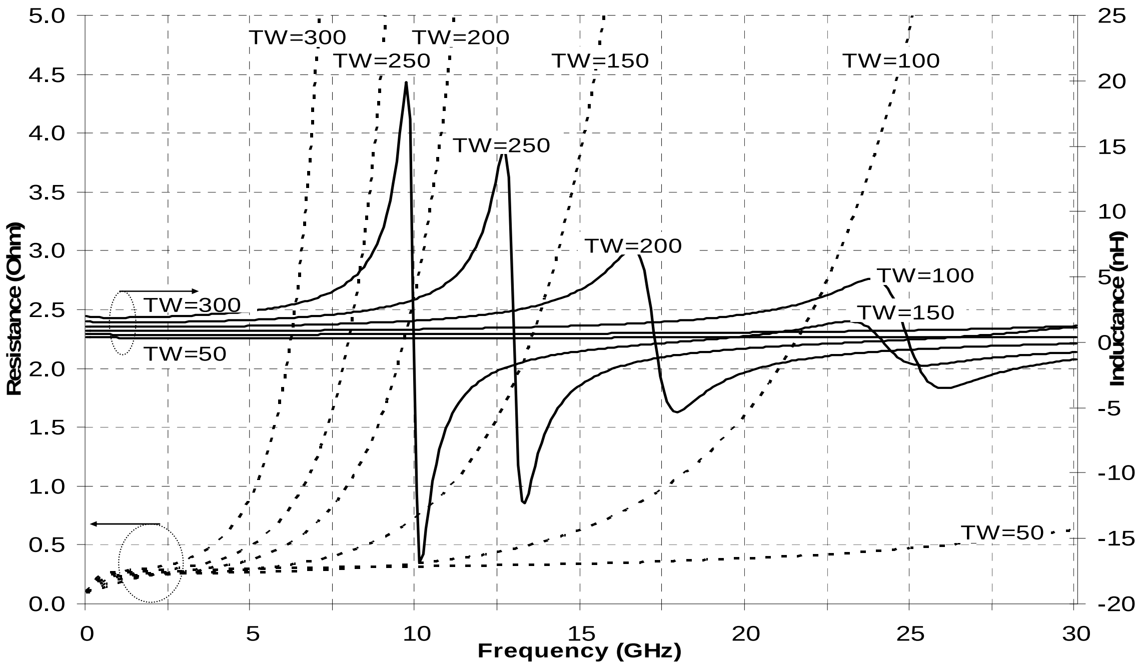

Fig. 10. Effects of Track Width on Inductance and Series Resistance
[Design parameters TS=10 μm, IR=35 μm and NT=1].

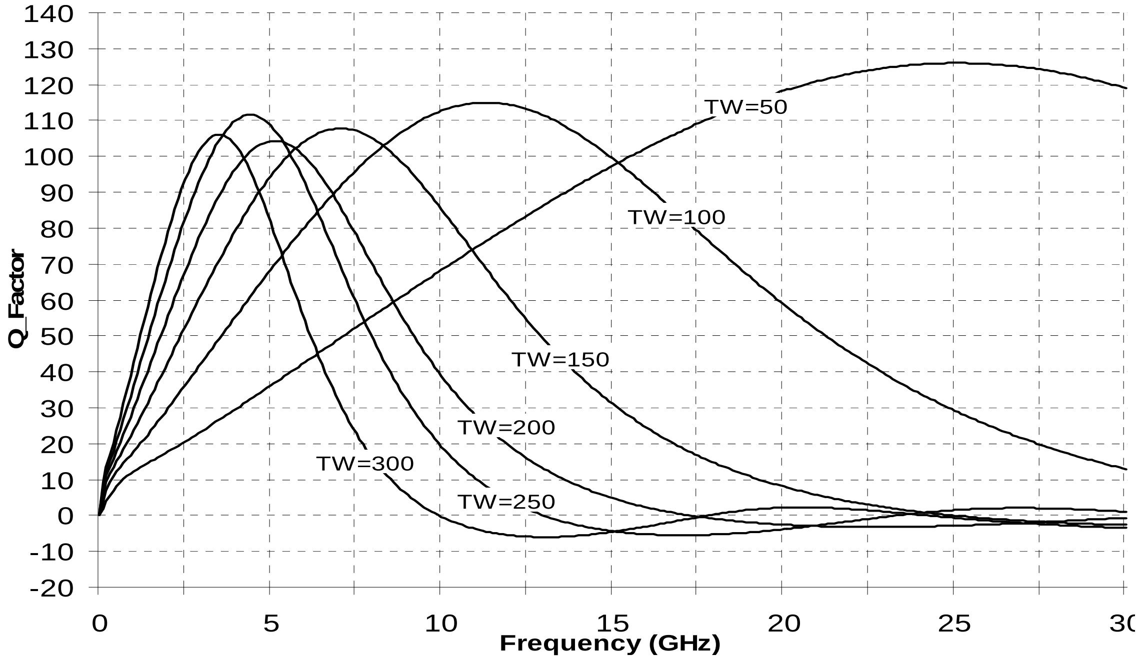

Fig. 11. Effects of Track Width on Q Factor [Design parameters TS=10 μm, IR=35 μm and NT=1].

As discussed earlier, to achieve large inductance, larger outer and inner radii are needed. It can be seen from Fig. 12 that Q factor decreases with increase in the inner radius. This is due to the increase in inner radius and the total track length. However, there was a slight increase in self-resonance frequency with decrease in inner radius. This is inline with the results obtained for effects of track spacing. It is concluded that smaller inner radius will achieve larger Q factor.

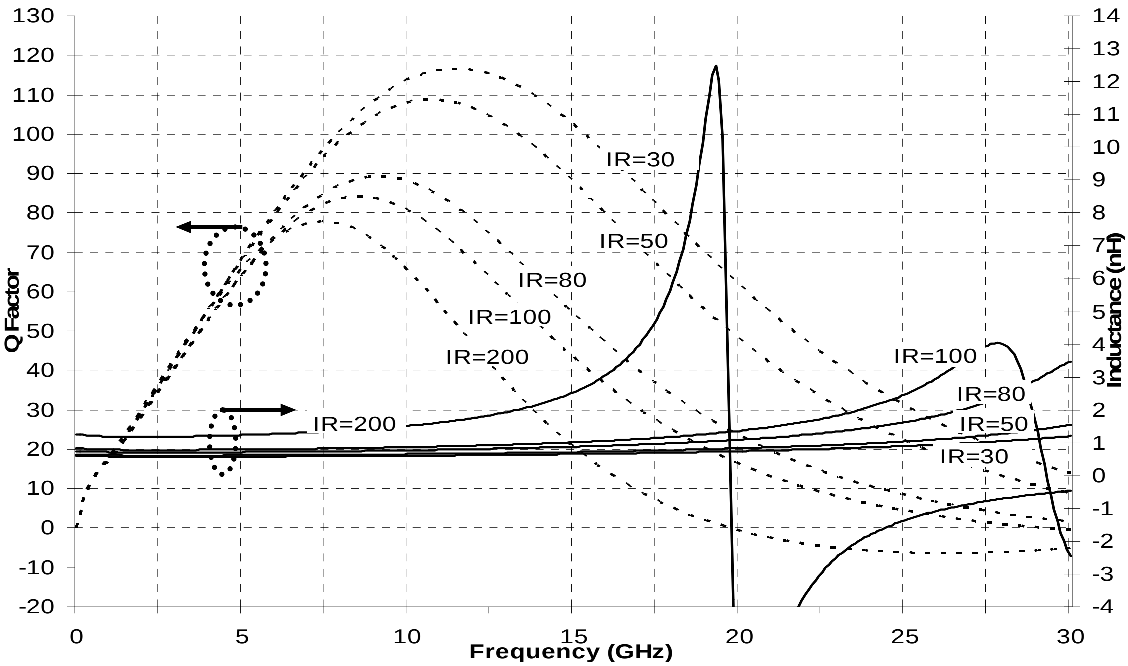

Fig. 12. Effects of Internal Radius on Inductance and Q Factor
[Design parameters TW=100 μm, TS=10 μm and NT=1].

Apart from the physical characteristics of the inductor coil, the substrate has greater effects on inductor performance. In a circular or spiral inductor the circular nature of current flowing through the inductor coil generates a magnetic field which passes through the substrate. The generated magnetic field causes a current flow in the substrate to counter act the magnetic field, and hence the net current flow in the inductor coils. This results in a reduction of the Q factor. Fig. 13 shows that the Q factor can be improved by having a patterned shielding between the substrate and inductor coil.

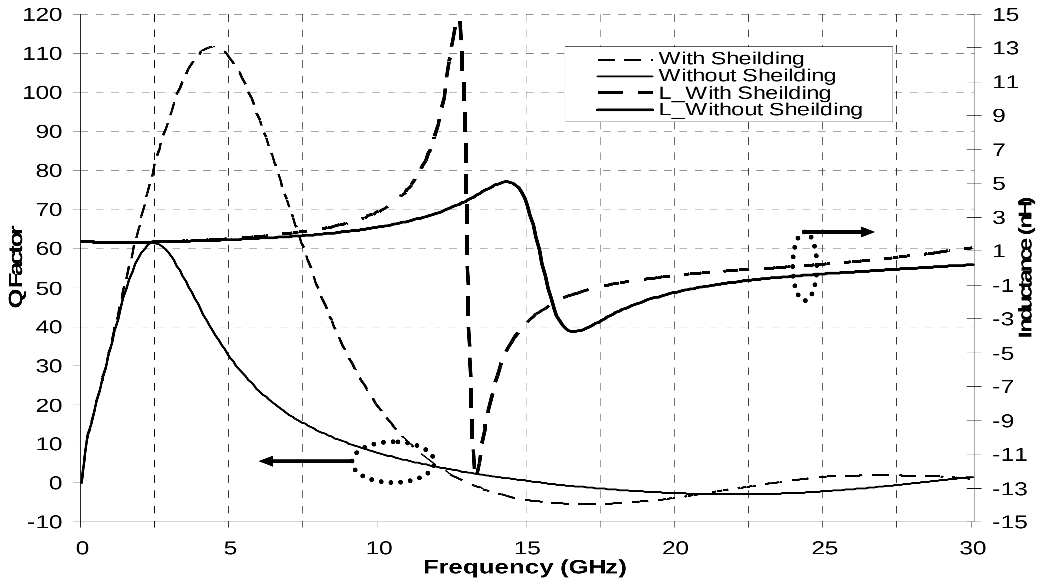

Fig. 13 Effects of Shielding on Inductance and Q Factor
[Design parameters TW=250 μm, TS=10 μm, IR=35 μm and NT=1].

Analysis of a single turn circular-spiral inductor shows that the Q factor of SOS inductor can be increased multi-fold in the desired band of operation by proper selection of inductor physical parameters and applying patterned ground shielding. Further analysis of a single turn spiral shows that the inductance depends on the width of the spiral and internal radius. To find out optimum values for track width and internal radius to achieve a 1.5nH inductor with highest Q factor a 3-D plot of inductance vs. track width and internal radius is presented in Fig. 14. Fig. 15 presents the plot of Q factor vs. the track width and internal radius.

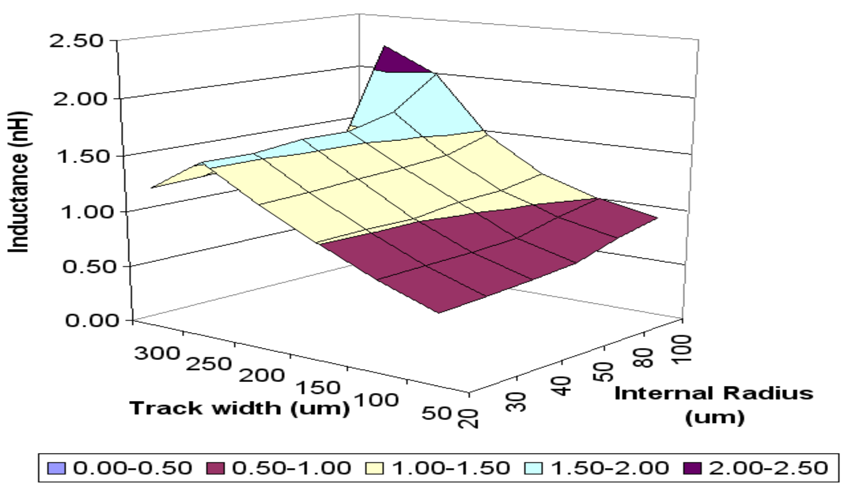

Fig. 14. Effects of Track Width and Internal Radius on Inductance.

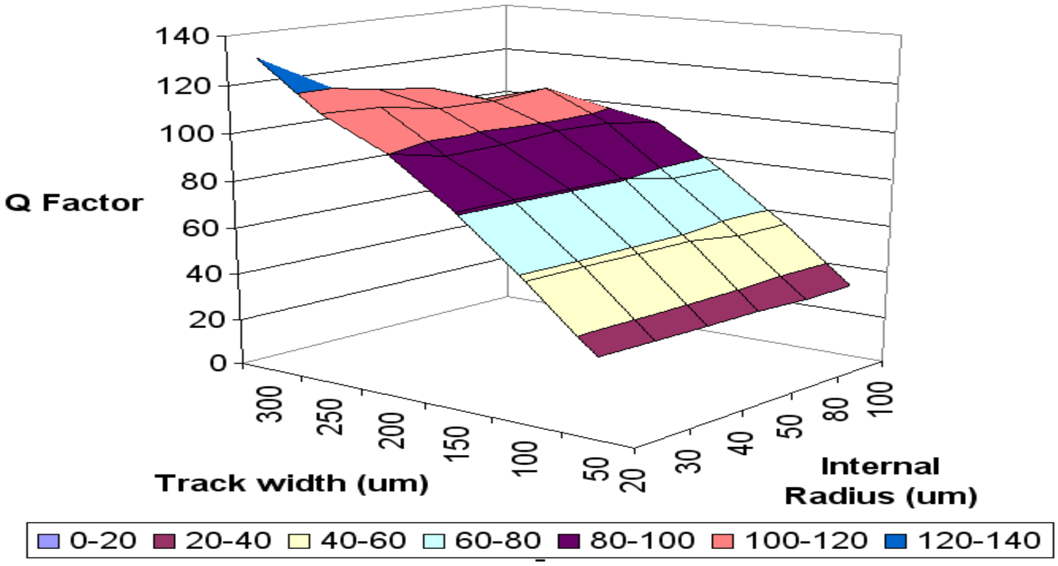

Fig. 15. Effects of Track Width and Internal Radius on Q Factor.

From Fig. 14 it can be concluded that the required inductance of 1.5 nH can be achieved with track width of 250 µm with various possible values of internal radius. However, Fig. 15 shows that the Q factor peaks at internal radius of 30 to 40 µm. Reducing the internal radius results in lower area and in this case it is advantageous as lower internal radius also improves the Q factor. After considering the effects of various parameters on inductor performance, a 1.5 nH single turn circular-spiral inductor is designed with metal-3 track width of 250 µm, track spacing of 3.2 µm and inner radius of 35.4 µm on sapphire substrate with 250 µm thickness and patterned ground shielding.

4. Results

The analysis of MEMS inductor shows that the Q factor of inductor can be improved by increasing the air gap between the substrate and the inductor coil. Results show that the required inductance of 1.5 nH can be achieved with the metal width of 30 µm with the various values of air gap. Fig. 2 shows that the highest Q factor of 45 at 4 GHz for 1.5 nH inductance is achieved at air gap of 70 µm. After considering the effects of various parameters on inductor performance, a 1.5 nH square spiral inductor is designed with metal thickness of 5µm, metal width of 30 µm, air gap of 70 µm, track spacing of 40 µm and outer diameter of 400 µm. This design achieves an inductance value of 1.5 nH with Q factor of 45 at 4 GHz operating frequency.

The inductor design using SOS technology has the advantage of near insulator substrate and added performance improvement due to use of wider metal track and patterned shielding. The final SOS inductor design achieves Q factor of 111 at 4GHz operating frequency. The performance of the Q for 1.5 nH inductors designed using MEMS and SOS technologies is compared with other literatures and is presented in Table 1. Authors in [9] had designed an inductor with 2µm metal thickness, 32.1 µm inner radius, 2.5 turns and 15 µm metal width using 0.18 µm TSMC technology. In [10] authors presented design of spiral inductor with silicon and quartz substrates. Also, suspended spiral inductors using surface micromachining technology with 40 µm and 50 µm air suspension are presented in [11] and [12] respectively.

Table 1. Inductor design parameters and performance comparison.

Reference					This work MEMS	This work SOS
Number of Turns	1.5	2.5	2.25	1.5	1.5	1
Air Gap (μm)	50	80	40	25	70	--
Metal	Cu	Al	Cu	Ni	Cu	Cu
Thickness of metal (μm)	20	2	15	30	5	3.2
Metal spacing (μm)	10	15	20	40	40	3
Metal width (μm)	--	--	30	80	30	250
Compare frequency (GHz)	4	4	4	4	4	4
Inductance (nH)	1.5	1.6	1.8	1.5	1.5	1.5
Q factor	9	12	26	42	45	111

4.1. VCO Performance Results

A cross coupled LC oscillator operating at 4GHz frequency, as presented in [13], is used as a testbench. The performance of VCO designed using the MEMS and SOS inductors are presented in Table 2.

Table 2. Comparison between VCO circuits with SOS and MEMS inductor.

Parameters	VCO with MEMS inductor	VCO with SOS inductor
Operating Voltage	2.5 V	2.5 V
Operating Frequency	4 GHz	4 GHz
Core Current (I_{core})	10 mA	4.5 mA
Phase noise @ 600 kHz	-113 dBc/Hz	-128 dBc/Hz
Phase Noise @ 1 MHz	-120 dBc/Hz	-133 dBc/Hz
Phase Noise @ 3 MHz	-132 dBc/Hz	-143 dBc/Hz
Power Consumption	25 mW	11.25 mW

Results indicate that the test-bench VCO achieve a phase noise of -113 dBc/Hz and -128 dBc/Hz at 600 kHz when employing the custom inductors designed in MEMS and SOS respectively. It can be seen that the phase noise of the VCO is reduced by 15 dB (i.e. 32 times reduction) when employing the SOS inductor instead of the MEMS custom inductor. This reduction is bases on the higher Q factor of the SOS inductor of 111 as compared to Q factor of the MEMS inductor of 45. Results also indicate that ~50 % power saving is achieved on the test-bench VCO when employing the SOS inductor as compared to the MEMS inductor.

5. Conclusion

This paper presents the design and implementation of inductors using MEMS and SOS technology. The inductor designs in MEMS and SOS achieve a Q factor of 45 and 111 respectively. The designed inductor improves the performance of the traditional cross-coupled oscillator circuit. The new improved SOS inductor result in at least 10 dB reduction of phase noise with about 50 % power reduction as compared to the oscillator designed with MEMS inductor. The reduced phase noise can be further traded for low power consumption for application in low power devices. A comparison of inductors in MEMS and SOS technologies suggest that the SOS has the potential to achieve higher Q factors needed for low-power low-cost RF applications such as UWB based wireless sensor nodes.

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Guide for Contributors

Aims and Scope

Sensors & Transducers Journal (ISSN 1726-5479) provides an advanced forum for the science and technology of physical, chemical sensors and biosensors. It publishes state-of-the-art reviews, regular research and application specific papers, short notes, letters to Editor and sensors related books reviews as well as academic, practical and commercial information of interest to its readership. Because it is an open access, peer review international journal, papers rapidly published in *Sensors & Transducers Journal* will receive a very high publicity. The journal is published monthly as twelve issues per annual by International Frequency Association (IFSA). In additional, some special sponsored and conference issues published annually. *Sensors & Transducers Journal* is indexed and abstracted very quickly by Chemical Abstracts, IndexCopernicus Journals Master List, Open J-Gate, Google Scholar, etc.

Topics Covered

Contributions are invited on all aspects of research, development and application of the science and technology of sensors, transducers and sensor instrumentations. Topics include, but are not restricted to:

- Physical, chemical and biosensors;
- Digital, frequency, period, duty-cycle, time interval, PWM, pulse number output sensors and transducers;
- Theory, principles, effects, design, standardization and modeling;
- Smart sensors and systems;
- Sensor instrumentation;
- Virtual instruments;
- Sensors interfaces, buses and networks;
- Signal processing;
- Frequency (period, duty-cycle)-to-digital converters, ADC;
- Technologies and materials;
- Nanosensors;
- Microsystems;
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