Application of New Matching Technique in Doherty Amplifier

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Abstract: According to the shortage of the traditional offset line in Doherty power amplifier, a new offset line technique is proposed to match carrier amplifier with the load and to improve the performance of the Doherty amplifier. By simulation of the computer software, a higher efficiency is obtained using the new offset line comparing the two kinds of offset lines. The new offset line technique could be applied in the system with high linearity and low power operation. *Copyright © 2013 IFSA.*

Keywords: Doherty power amplifier, Offset line, Analogous offset line.

1. Introduction

With the steady and effective process of social informatization, transmission network, content diversity, terminal mobile and commercialization operation, in recent years people have seen the fast replacement and development of high speed mobile communication system and broadband multimedia broadcast system. Along with the signal bandwidth of wireless transmission is continuously increasing, the inherent frequency selective fading of wireless channel and narrow band interference effects become the main factors of wireless transmission effect.

In the modern wireless communication system, Doherty technology [1] is one kind of amplifier design technology with best commercial prospect, because of its simple structure, low cost, is easy to implement, the influence to system linearity is relatively minor and is suitable for high efficiency transmission of modern wireless signal with Peak to Average Power Ratio.

This paper firstly introduce the fundamental principles and offset line technology of Doherty power amplifier, secondly put forward the concept

and calculation method of analogous offset line according to shortage of low power line carrier offset line, and compare the system efficiency joined the traditional offset line with the system efficiency joined class offset line by the simulation design for Doherty amplifier, the result show that the performance of the low power system can be improved after joining analogous offset line.

2. Fundamental Principles of Doherty Power Amplifier

The classical structure of Doherty power amplification circuit [2-4] is shown in Fig. 1. It's consists of two amplifier, respectively called carrier amplifier and peak amplifier, and the carrier amplifier works in class AB or class B, peak amplifier works in C. The two amplifiers connect in parallel, the cascading quarter wavelength transmission line after carrier amplifier play a role in impedance transformation and the quarter wavelength transmission line before the peak amplifier contribute in the phase compensation. The

peak amplifier begin to work when the carrier amplifier is close to saturation, so that by reducing the carrier amplifier's apparent impedance makes the carrier amplifier output more current when reaching saturation. Using this method can make the power amplifier gain high efficiency in saturated output point back within 6 dB.

Fig. 1. Structure diagram of Doherty power amplifier.

Doherty power amplifier has three working status: low power state, which only carrier amplifier works, peak amplifier output end opens, carrier amplifier output impedance value is twice than the best impedance, and the high impedance makes the output current of carrier amplifier is only half of the maximum when they close to saturation, at this time, the efficiency achieves to the first peak point; middle power state, which the peak amplifier began to work when the carrier amplifier is working in saturated state, the load traction technology make the carrier amplifier output more current with invariant output voltage constant, and the system efficiency always stay at higher level; high power state, which the two amplifier both are working in saturated state, output current reaches the maximum, and the system achieves the second efficiency peak point.

3. Analogous Offset Line Technology

The following problems of Doherty amplifier in the actual application exist [5]: peak power amplifier doesn't work in low power state, certain open circuit resistance and the parasitic capacitance exists between leakage and source, through the matching network, the load as a carrier amplifier will show a impedance value, which leads the power of the carrier amplifier leak to the peak power amplifier; in high power state, carrier amplifier's output impedance Z_{opt} matches to 50Ω , and in low power state, carrier amplifier's load impedance change into 100Ω , Z_{opt} and load do not match. In view of the above questions, the literature [6-8] mentioned the offset line method to solve the problems, namely add

a transmission line with 50Ω characteristic impedance behind the carrier power amplifier and peak power amplifier, respectively called carrier offset line and peak offset line in this paper.

For peak offset line, due to the peak amplifier's output impedance has very low resistance and strong capacity in low power status, as point A shown in Fig. 2, the output impedance can be adjusted to high resistance area by adjusting the 50Ω transmission line, and the peak amplifier is approximately open, set output impedance of peak amplifier output end point A in Fig. 3 for Z_A , reflection coefficient.

Fig. 2. Schematic diagram of offset line.

Fig. 3. Schematic diagram of analogous offset line calculation.

$$\Gamma_A = \frac{Z_A - 1}{Z_A + 1} = |\Gamma_A| \angle \phi_A \quad (1)$$

The length of peak amplifier's line offset:

$$L_{opt} = \frac{\phi_A}{4\pi} \lambda \quad (2)$$

Among them, β is the phase constant, λ is the wavelength and ϕ is phase.

For carrier offset line, suppose Z_{popt} is the best output power impedance for carrier power amplifier when load in traction, Z_{eopt} is the best efficiency impedance for carrier power amplifier when its output power is half of the saturation power, Z_{popt} and Z_{eopt} are impedance seen in the carrier power amplifier drain. The point Z_{popt} is matched to 50 Ω through the matching network in high power status, the point Z_{eopt} must be matched to 100 Ω if early saturation is going to be made to obtain greater efficiency in low power. When Z_{eopt} is matched to round 1 which is shown in Fig. 2 [9] through the same matching network, Z_{eopt} can be matched to 100 Ω by adjusting carrier offset line length.

In actual cases, the output impedance of Z_{eopt} through the matching network are not round 1 shown in Fig. 2, and adjusting the carrier offset line length cannot make Z_{eopt} matching to 100 Ω . In order to solve this problem, this paper puts forward the concept of analogous offset line, and changes the characteristic impedance and length of offset line at the same time, which making the carrier power amplifier is matched with 100 Ω loads in low power.

Suppose ABCD matrix of matching network designed by Z_{eopt} is:

$$M = \begin{pmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{pmatrix} \quad (3)$$

To the matching network, there is:

$$\begin{pmatrix} V_0 \\ I_0 \end{pmatrix} = \begin{pmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ I_1 \end{pmatrix} \quad (4)$$

When is in low power, choose $Z_{\text{opt}} = Z_{\text{eopt}}$, according to $Z_{\text{opt}} = \frac{V_0}{I_0}$, $Z_1 = \frac{V_1}{I_1}$, there is

$$Z_1 = \frac{Z_{\text{eopt}} m_{22} - m_{12}}{m_{11} - Z_{\text{eopt}} m_{21}} \quad (5)$$

$Z_1 = R_1 + jX_1$, to analogous offset line, there is

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} \cos \theta & jZ_0 \sin \theta \\ j\frac{1}{Z_0} \sin \theta & \cos \theta \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} \quad (6)$$

substitute $Z_1 = \frac{V_1}{I_1}$, $Z_2 = \frac{V_2}{I_2} = 2R_0$ ($R_0 = 50 \Omega$), the following result is got:

$$\begin{cases} Z_0 = \sqrt{\frac{2R_0 X_1^2}{R_1 - 2R_0} + 2R_0 R_1} \\ \theta = \arctan \frac{(R_1 - 2R_0) Z_0}{2R_0 X_1} \end{cases} \quad (7)$$

where Z_0 and θ are respectively the characteristic impedance and angle of analogous offset line. By

joining analogous offset line, the carrier power amplifier's best efficiency impedance Z_{eopt} and 100 Ω loads are matched in low power, and prodigious efficiency can be obtained. In high power status, because Z_{eopt} and Z_{popt} differ rarely while $\text{real}(Z_{\text{eopt}}) < \text{real}(Z_{\text{popt}})$, the calculated Z_0 will close to 50 Ω , and the influence on the system's performance is not big [13].

4. Computing Software Simulation

ADS software is chosen to do the simulation, and LDMOS tube MRF6VP3450H of Freescale, which is selected. It is a pipe, with 470-860 MHz working frequency band, 22 dB gain, 450 W maximum output power. It is easy to realize Doherty amplifier by using it [10, 11].

First of all, quiescent point is determined by dc simulation, and carrier power amplifier is working in class AB, with 2.8 V grid voltage and 48 V drain voltage. Peak power amplifier is working in class C, with 1.4 V grid voltages and 48 V drain voltage [12].

Then draw power amplifier's input impedance $Z_{\text{source}} = 2.247 - j1.5456$, the best output impedance $Z_{\text{popt}} = 2.34 + j1.981$, and the optimum efficiency impedance $Z_{\text{eopt}} = 1.517 + j2.643$ in half power output through the source traction and load traction. Using Z_{source} and Z_{popt} to design input/output matching network, and the single tube simulation performance curve is shown in Fig. 4.

The designed Doherty amplifier is shown in Fig. 5. The carrier power amplifier and the peak power amplifier use the same input/output matching network, and the input power is allocated to the carrier power amplifier and peak power amplifier through equal power allocation such as the Wilkinson power splitters [14].

According to the offset line calculation method, the peak offset line is 51.58 mm, and carrier offset line is 52.43 mm. analogous offset line $Z_0 = 40.36 \Omega$ and $\theta = 56.41^\circ$ are calculated from the formula (7), namely the width and length of transmission line is respectively 2.42 mm and 46.00 mm.

The Power Added Efficiency curve of Doherty amplifier power concluded by simulation is shown in Fig. 6. Among them, the diagram Fig. 6 (a) is simulation results where the carrier power amplifier uses 50 Ω offset line. Fig. 6 (b) is simulation results where the carrier amplifiers use analogous offset line [15].

Comparing Fig. 6 (a) and Fig. 6 (b), it can be seen that the characteristic impedance of class Z_0 offset line has better performance than 50 Ω offset line in low power. There is 3.956 % improvement in efficiency at the first peak point, and a 9.592 % improvement in efficiency when the output power is 50 dBm, and a 4.447 % improvement in efficiency when the output power is 45 dBm. In the medium power and high power the efficiency declines slightly, but the efficiency is still very high.

Fig. 4. Simulation performance of single tube.

Fig. 5. Simulation schematic diagram of Doherty power Amplifier.

Fig. 6. Power Added Efficiency of Doherty power amplifier.

5. Conclusion

By using analogous offset line technology, the efficiency performance of Doherty amplifier in low power is considerably improved. In order to obtain higher output power, combined with balanced amplifier technology, 150 W balanced Doherty power amplifier is designed in UHF frequency band. All the indexes of this system meet the requirements for power amplifier of the digital TV system, and this system is with practical application value.

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