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# Digital Back-end Based on a Low-power Listening Protocol for Wake-Up Receivers

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**Abstract:** An ultra-low-power digital baseband (DBB), based on a low power microcontroller (MCU), is presented. The DBB functions as a decoder for the Wake-up receiver (WuRx). It also implements a duty-cycle protocol meant to control the WuRx peripherals to further reduce its average energy consumption. The DBB generates very short power-on periods, during which, it has to detect the presence of a wake-up packet. This allows very low latency between a transmitted wake-up packet and its detection. The WuRx's power consumption and data rate are scalable and can be reconfigured to meet specific requirements. It emphasizes the possibility to decode more than 512-bit address pattern.

**Keywords:** DBB, Digital baseband, Wake-up receiver, Wireless Sensor Network, WSN, Low-power, Duty-cycle.

## 1. Introduction

Energy consumption is critical in WSN as batteries represent usually its only power sources. Replacing or changing batteries in WSN can be costly and difficult to realize. In practical cases, the lifetime of a WSN reaches its end when all devices (wireless sensor nodes) within the network go permanently inaccessible. A depleted battery can be one of the causes. Radio chip, in a wireless node, consumes the most energy with reference to the rest of node's components (i.e., sensors, microcontroller (MCU)). Some works proposed different approaches to solve these trade-offs. In [1], a proposed strategy, namely game-theoretic approach, suggests improving the packet reception ratio in a WSN. The presented model looks for an equilibrium point between transmission power and acts accordingly on all sensor nodes. While this improves efficiency of the WSN, it drastically

increases the complexity of the network. In addition, it may be irrelevant for implementation for numerous applications where the radio's permanent activity is often not necessary. The authors in [2] propose a specific model for sensor node deployment. It solves the coverage of the area of interest while using the least possible number of sensor nodes. Accordingly, average energy consumption of the WSN can be further reduced. In a duty-cycled radio approach, switching the radio to sleep state instead of the idle listening enhances the battery's lifetime. However, long radio sleep states affect communication latency and increase transmission energy because of the increased preamble. In on-demand application where radio communication is less frequent, a much lower power radio receiver, referred to as (WuRx), can be used to replace the idle listening of conventional transceiver. Generally, its main purpose is to continuously listen for an incoming wake-up packet

(WuPt), whilst having the rest of the devices in sleep state. It is communicated from a different node. Upon WuPt reception, the WuRx, then, issues an interrupt to the MCU, which, in return, wakes-up the main transceiver.

The WuRx should be based on simple architectures to keep the overall complexity of a sensor node to a minimum. Other characteristics are sensitivity, data rate and energy usage. In a WSN where each sensor node is embedded with a WuRx, the latter should distinguish between different WuPt. This is done by including a unique destination address in every WuPt. Fig. 1 illustrates the basic blocks found in a typical WuRx. The DBB deals with the address pattern correlation and issues a logic signal if it is addressed. This way, unnecessary MCU active/sleep toggling is avoided and more energy is saved.



Fig. 1. Simplified WuRx block diagram.

Depending on how dense is the WSN, the WuPt includes a unique pattern for every node, coded in 16, 32, 64 bits, etc. On-off keying (OOK) is often used for modulation schemes as it allows low-complex architectures. However, this can impact the overall sensitivity and power demand of a WuRx. Several DBBs are introduced in recent works to optimize the mentioned features. [3-4] use AS3932 [5] or AS3933 [6] as an off-the-shelf DBB. The chip eliminates the need of a digitizer (i.e., comparator), meaning that it is able to condition an analog representation of the

pattern bit sequence. The minimum sensitivity reaches down to 80  $\mu V_{RMS}.$  The chip consumes more than 5  $\mu W$  when listening and 24  $\mu W$  during pattern decoding. The authors in [7] used an MCU to deal with the decoding mechanism. With no RF activity, the MCU is at its lowest sleep state consuming 40 nW. It activates the core at 8 MHz upon reception of the WuPt preamble, followed by WuPt correlation, during which, it drains 300  $\mu W.$  This indicates that the more WuPt the WuRx receives the more it consumes.

In [8], another design based on flip-flops is introduced. The DBB is optimized for a specific duty-cycled WuRx, specifically DCW-MAC [9].

At 250 kbit/s, it consumes 0.9 µW. A complex programmable logic device (CPLD) and a fieldprogrammable gate array (FPGA) can be used to act as DBB for WuRx. The energy consumption, however, is still higher than most of the introduced DBB [10-11]. In this work, a DBB for duty-cycled WuRx is introduced. The detection procedure is based on lowpower listening (LPL) protocol [12]. It is safe to say that the DBB is fully flexible to implement different MAC protocols depending on the application prerequisites. The introduced DBB offers scalability in terms of address pattern length, data rate and energy consumption. This paper is organized as follows: In Section 2, details and analysis of the design process are discussed. Section 3 reports the measurements done on a fabricated WuRx with the presented DBB. Finally, Section 4 concludes the proposed work.

## 2. Energy Analysis

The digital baseband power gates the internal peripherals by following a duty-cycled schemed based on LPL protocol (Fig. 2).

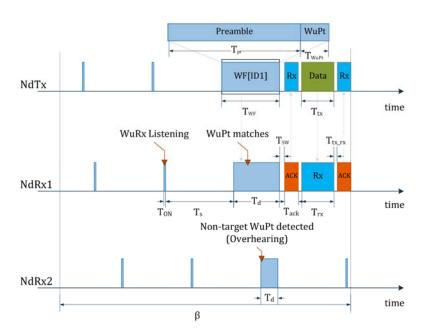


Fig. 2. LPL implementation for the WuRx.

Consider a WSN with N nodes with N WuRxs. A wake-up frame (WF) gets checked every  $T_{ON}$  by each sensor. A WF represent a preamble and a WuPt. A transmitter node NdTx sends a WF to a receiving node NdRx1. A successful preamble detection by the NdRx1 activates the corresponding MCU and the main transceiver to perform data exchange. The WuPt decoding lasts  $T_d$  and can vary depending on the WF arrival time. The value of  $T_d$  depends on the length of the WF. It is expressed as in Eq. (1).

$$T_{WF} \ge T_d \ge T_{WuPt} + T_p,\tag{1}$$

where  $T_p$  is the preamble length,  $T_p$  is the time needed to detect a preamble and  $T_{WuPt}$  is the WuPt length. A second non-target node NdRx2 can also detect the WF. After address checking of the WuPt, NdRx2 ignores it and turns back to WF checking. This overhearing wastes energy consumption. Let  $\beta$  be the mean interval between two transmitted WFs.

The introduced DBB allows to detect the preamble  $T_{ON}$  to be short enough, thus reducing the latency and energy consumption. In On-demand scenarios, data exchange is unpredictable and less frequent. This means that the interval  $\beta$  is long enough when  $\beta > T_{WF}$ . By following the described communication protocol, the energy consumptions,  $E_{NdTx}$  for NdTx,  $E_{NdRxI}$  for NdRx1 and  $E_{NdRxn}$  for NdRx2 in an interval  $\beta$ , are expressed in (2), (3) and (4).

$$E_{NdTx} = \beta P_{SLEEP} + E_{l tx} + E_{tx}, \qquad (2)$$

$$E_{NdRxI} = \beta P_{SLEEP} + E_{l rx} + E_{rx}, \qquad (3)$$

$$E_{NdRxn} = \beta P_{SLEEP} + E_{l nrx}, \tag{4}$$

where  $P_{SLEEP}$  is the power demand of the node at sleep state,  $E_{l\_tx}$ ,  $E_{l\_tx}$  and  $E_{l\_mx}$  are the WuRx's average energy consumption during idle listening for the transmitter, receiver and non-target receiver, respectively.  $E_{tx}$  is the energy consumed by NdTx1 during WuPt and data transmission.  $E_{tx}$  represents the energy required for data reception.

During  $\beta$ , the WuRx's average energy consumptions of every node  $E_{l\_tx}$ ,  $E_{l\_rx}$  and  $E_{l\_mrx}$  depend on  $T_{\rm ON}$  and the decoding time  $T_d$ . Assuming that the WuRx is deactivated right after finishing decoding process, the energy models are express as follows:

$$E_{l\_tx} = P_{WuRx} \frac{T_{ON}(\beta - \Delta_{tx})}{T_{ON} + T_S},$$
 (5)

$$\mathbf{E}_{l_{rx}} = P_{WuRx} \frac{T_{ON}(\beta - \Delta_{rx}) + T_{s}(T_{d} - T_{ON})}{T_{ON} + T_{s}},$$
(6)

$$E_{l\_nrx} = P_{WuRx} \frac{\beta T_{ON} + T_s (T_d - T_{ON})}{T_{ON} + T_s},$$
 (7)

where

$$\Delta_{tx} = T_{SW} + T_{WF} + 2 T_{ack} + 3 T_{tx} r_x + T_{tx}$$

and

$$\Delta_{rx} = T_{SW} + 2 T_{ack} + 3 T_{tx} r_x + T_{rx}$$

denote the sum of activity and transition durations performed by the main transceiver and the MCU.  $T_{tx\_rx}$  is the transition delay of the transceiver from TX to RX mode and vice versa.  $T_{ack}$  is the time required to receive an ACK.  $T_{SW}$  represents the time slot required for the MCU and the radio to switch from sleep to active state. Furthermore, the energy consumptions related to data exchange or packets transmission are given by:

$$E_{tx} = E_{SW} + P_{tx}T_{WF} + 2P_{rx}T_{ack} + 3E_{tx} + P_{tx}T_{tx}$$
, (8)

$$E_{rx} = E_{SW} + 2P_{tx}T_{ack} + 2E_{tx} r_x + P_{rx}T_{rx},$$
 (9)

where  $E_{SW}$  is the energy consumption during the MCU's transition from sleep to active.  $E_H$  corresponds to the energy consumed during  $T_H$ .  $E_{tx\_rx}$  denotes the energy needed from the transceiver to switch from TX to RX mode or vice versa.  $P_{tx}$  and  $P_{rx}$  are the power needed for packet transmission and reception, respectively. Hence, for a WSN with N nodes the total energy consumption during  $\beta$  is expressed in Eq. (10).

$$E = E_{NdTx} + E_{NdRx1} + (N-2)E_{NdRxn}$$
 (10)

The above analysis takes into account the radio transceiver, the MCU and the WuRx energy consumptions. However, this work focuses only on the analysis of the DBB's energy consumptions, where  $P_{ON}$  and  $P_{WDT}$  are the power consumption of the MCU at active state and sleep with watchdog enabled, respectively. The detection is performed in a purely asynchronous scheme. OOK is employed for a low-power front-end architecture.

## 3. System Description

The proposed solution relies on maximizing WuRx's sleep time instead of constantly monitoring the channel. It allows the adjustment of several parameters such as destination address length, data rate and WuPt detection latency. This scalability makes the WuRx suitable for a wide range of applications. Alowpower MCU PIC12LF1572 [13] is used to design the back-end of WuRx. The MCU periodically wakes- up then enables the rest of WuRx components. If any RF signal is fed through the front-end during this brief time duration  $T_{ON}$ , the MCU waits for a corresponding WuPt preamble. If it is the case, it keeps the active components active to receive the rest of WuPt. A decision is made depending on the correlation results followed by switching off all active components. The MCU switches to sleep state for TS until the next wake-up period. The MCU waits for preamble detection during  $T_{ON}$ . In the case where there is no WuPt, all

components are turned off and the MCU turns back to sleep. Fig. 3 illustrates the timing diagram where the MCU successfully detects/misses a WuPt. The illustrated arrival time of the WuPt is considered the best case scenario as the MCU activates for the minimum necessary time  $T_d$ . The opposite case is when the preamble is detected at the very beginning of the WuPt. Then, the MCU has to process the entire

WuPt, wasting more energy. From Eq. (10) and Eq. (6) the DBB's average power consumption is calculated as follows:

$$P_{avg} = P_{WDT} + \frac{P_{ON}(T_{ON}(\beta - \Delta_{rx}) + T_S(T_d - T_{ON}))}{\beta(T_{ON} + T_S)}$$
(11)

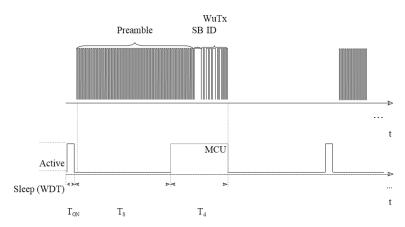


Fig. 3. Simplified timing diagram of WuPt and duty-cycled MCU in channel listening.

#### A. WuPt Structure

The WuPt contains a preamble, separation bits (SB) and destination address pattern (ID). The preamble  $\{p0 \dots p_{i-1}, i \in \mathbb{N}\}$ , consisting of i-bit, helps the MCU detect the presence of WuPt. SB  $\{s0 \dots s_{j-1}, j \in \mathbb{N}\}$  are composed of j-bit. The sequence separates preamble and the ID.

Let k N. The ID consists of k times 10-bit sequence (Fig. 4) where  $\{d0...d7\}$  are the 8-bit ID and 2 bits for a start and stop bits. k=2 and k=4 represent 16-bit and 32-bit IDs, respectively.



Fig. 4. 8-bit ID sequence diagram.

Depending on the memory of the MCU, the latter can decode more than 512-bit. The start and the stop bits help the MCU localize the pattern.

### B. Back-End Architecture

Instead of continuously waiting for an incoming WuPt, the self-duty cycled MCU wakes-up periodically to monitor the channel. When the MCU enters sleep state, all its internal peripherals are automatically disabled except for the watchdog timer (WDT). By enabling the latter, the MCU can toggle between active/sleep state without the need for an external timer. The more interesting characteristic of the WDT lies in its energy consumption with only 260 nA at 1.8 V. When WDT overflows, the MCU is interrupted

and switches to active state. The WDT's time-out represents also the sleeping period TS of the WuRx. This can be configured between 1 ms and 256 s [13]. In [14], the WDT is considered deactivated during the  $T_{ON}$ . For the sake of the protocol's simplicity the WDT is left continuously on. When the MCU enables all active elements of the WuRx, it holds waiting for a WuPt preamble (i.e., '010101...') till an elapsed duration of  $T_{ON}$ . Upon the reception of the preamble, the MCU counts the positive edges of each single  $p_{i-1}$  bit for  $i_c$  times. The counting stops if it reaches n ( $i_c = n$ ), where n is a user-defined number of positive edges the MCU has to detect. If  $i_c < n$ , the detection is considered erroneous, then the MCU turns-off all external peripherals and switches back to sleep.

Any interfering signal, that has a baseband frequency higher or lower than  $f_c$ , is rejected by the MCU by means of digital filtering. This is done by continuously polling an input pin for a certain period of time  $t_p$ , in a way that if the positive edge comes sooner or later than expected the preamble is rejected. Let  $f_c$  be the modulated signal frequency. The choice  $t_p$  is done by the following equation.

$$\frac{1}{f_c} < t_p < \frac{2}{f_c} \tag{12}$$

The choice of  $T_{ON}$  depends on  $t_p$  and the power- on time tPOWER of all peripherals including the MCU's core. The minimum  $T_{ON}$  should obey the Eq. (13).

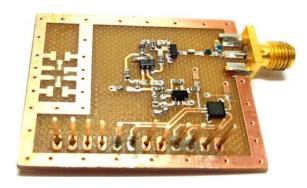
$$t_{POWER} + t_p < T_{ON} \tag{13}$$

In the different case of successful preamble detection, the MCU remains active and waits for  $s_{j-1}$ -bit. The SB structure is a successive j of '1' bits.

If SB sequence is received, the MCU enables the enhanced universal synchronous asynchronous receiver transmitter (EUSART). The latter is a peripheral within the MCU dedicated for serial communication. The usage of EUSART excludes the need of a software implementation for serial data reception. The correlation process starts upon reception of the first '0' bit (start bit) after SB. The EUSART stores the  $\{d0...d7\}$  in a byte register to be read later on. The process is repeated k times until the processing of all ID frame takes place. The MCU, then, compares the received byte(s) to the stored value(s). The comparison brings the decision to either issue an interrupt or not to an external unit. In the end, the MCU disables the EUSART and all WuRx's peripherals. The decoding process takes time  $T_d$  and affects dynamically the average power consumption of DBB. In the following section, we configure the MCU the required parameters to evaluate its performance.

## 4. System Evaluation

The front-end published in [15] is used to implement and evaluate the DBB. It consists of an envelope detector that performs an RF to DC conversion. Then an amplifier boosts the signal and forward it to an analog to digital convertor. In the end, the logic signal is fed to the DBB. Only the electrical characteristics of the MCU are taken into account for the final measurements. Fig. 5 shows all the assembled components on a PCB.  $T_S$  represents the latency of WuPt detection since at that time the DBB is at sleep state. It is configured by acting on the watchdog timer.

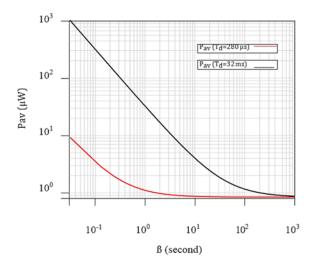


**Fig. 5.** Assembled wake-up receiver with the presented DBB on 1.55 mm thick printed circuit board (PCB).

For the sake of the complete system evaluation, the DBB it is set to perform preamble detection every  $T_S = 32$  ms. Moreover, when exiting sleep mode, the high frequency internal oscillator (HFINTOSC) is activated, which requires a certain time to stabilize.

For the PIC12LF1572, the HFINTOSC warm-up time  $t_{POWER}$  =5 µs. 16 MHz is chosen for the core frequency to allow maximum processing speed at which, the MCU demands a power  $P_{ON}$  =1 mW. 32 MHz requires a phase locked loop (PLL) and needs

more than 2 ms to settle. The WuPt modulated frequency is chosen  $f_c$  =128 kHz. From Eq. (12),  $t_p$  is calculated  $t_p$ =8  $\mu$ s. Hence, from Eq. (13),  $T_{ON}$ =13  $\mu$ s. Using these parameters on the Eq. (11),  $P_{av}$  can be simulated against the mean average interval  $\beta$  for minimum and maximum durations of  $T_d$ . The latter depends on the WuPt arrival time and when it coincides with the MCU's preamble polling. Fig. 6 shows the obtained results. For  $\beta$ >1000 s the average power is  $P_{av}$  <0.9  $\mu$ W for  $T_S$  =32 ms.



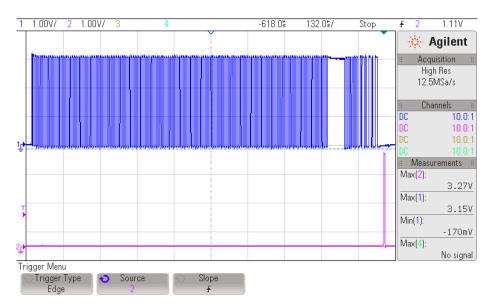
**Fig. 6.** The MCU's average power consumption against the mean interval time  $\beta$  for different decoding durations  $T_d$ .

The MCU is configured to correlate a 24-bit ID {0x55, 0x69, 0x96}. Fig. 7 shows a successful decoding process finished by issuing a pulse at an output pin.

The duty-cycle obeys the LPL protocol. This can cause overhearing issues in a dense WSN, thus increasing energy consumption. The DBB allows flexible implementation of different MAC protocols as to address specific applications demands.

## 5. Conclusion

An MCU-based back-end for duty-cycled wake-up receivers is introduced. It operates as a DBB with addressing capabilities and also controls the activity of WuRx peripherals to reduce the overall energy consumption. The MCU is fully configurable either by an external unit or by acting on its firmware. Main configuration parameters including latency, data rate and ID length allow a wide range of input values. A prototype is realized as to evaluate the intended features. For a latency of  $T_S = 32$  ms, the DBB consumes less than 1 µW. The power consumption depends on timing parameters, which can be configured depending on the application requirements. Additionally, several MAC protocols can be implemented to improve different performance measures, including energy consumption, overhearing issues and latency.



**Fig. 7.** Oscilloscope screen capture of a correlated WuPt's ID (blue). A generated pulse (pink) indicates a matching ID with the register values.

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