

## Description

The PDI-LNL2048S has a pixel size of  $7\mu\text{m}\times 7\mu\text{m}$  optical area,  $7\mu\text{m}$  center-to-center spacing, and 85% fill factor. The PDI-LNL2048S is ideal for line scan applications, such as fluorescent imaging or optical inspection, which require low-noise, high sensitivity and wide dynamic range. The four *acquisition* modes include Read After Integration for applications requiring high quality signals, buffered Single Read During Integration of the next line for higher-speed operation, Read On Integration for the highest speed at a cost of higher noise, and a mode which permits sampling during integration (non-destructive read-out): Multiple Read During Integration. The multiple read mode permits oversampling for demanding low-light applications. A JTAG-based *programmed mode* is available to meet a wide range of specialized imaging requirements. In this mode, external signals control the read-out cycle.

Packaging options include CLCC, and TE cooled package. Evaluation kits are available for prompt evaluation of the sensor, and display of either the analog outputs or digital samples for capture in a PC.

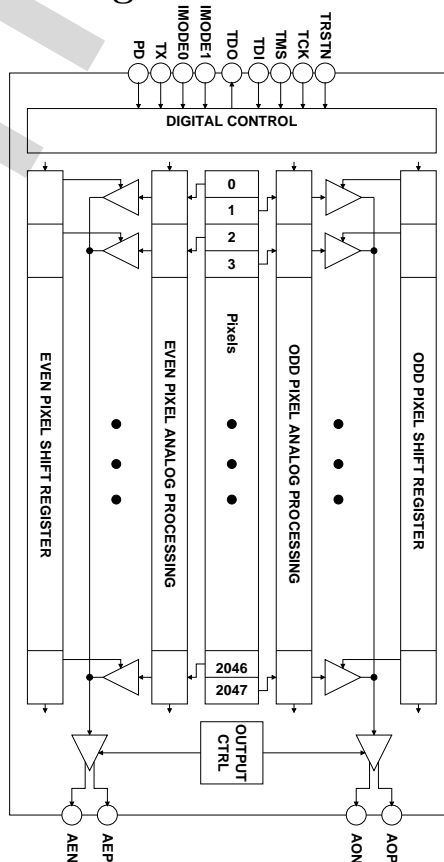
## Key Feature Summary

- Package size:  $22.35\text{mm}\times 6.35\text{mm}\times 2.85$  (l×w×h)
- Maximum output rate: 40Mpixel/sec
- 1 or 2 output ports
- Wide dynamic range: 52000:1 (94dB)
- Very low read-out noise: 1 electron
- Low dark current
- Excellent linearity
- 3.3V 200mW operation plus power-down
- Two independent gain settings per pixel
- Electronic shutter and anti-blooming drain
- Non-destructive read-out mode for Fowler sampling

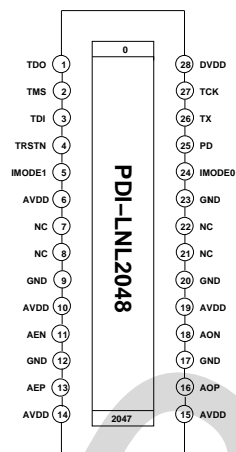
## Applications

- Microscopy
- Photon Counting
- Fluorescent imaging

## Block Diagram



## Pinout Diagram



(See Table 1 for pinout definitions)

Information furnished by Pixel Devices Intl is believed to be accurate and reliable. However, no responsibility is assumed by Pixel Devices for its use, nor for any infringements of patents of third parties which may result from its use.

Table 1: Electrical Specifications **PDI-LNL2048S**, RAI acquisition,  $T_{int} = 5\text{ms}$ ,  $V_{DD} = 3.3\text{V}$ ,  $T = 25^\circ\text{C}$ 

Parameter	Min	Nom	Max	Units
Supply current per active output		15	20	mA
Supply current (outputs inactive during integration)		15	20	mA
Supply current (power-down)		10	20	$\mu\text{A}$
Output swing	1.0	1.5		volts
Output capacitive load	10	30	50	pF
Output resistive load	1	2.2	$\infty$	k $\Omega$
RIR	99.75			%
RIL			0.25	%
Sensitivity (high gain)		25		V/lux-sec
Sensitivity (high gain)		169		V/ $\mu\text{J}/\text{cm}^2$
Sensitivity (low gain)		2.5		V/lux-sec
Sensitivity (low gain)		16.9		V/ $\mu\text{J}/\text{cm}^2$
Pixel response nonuniformity			$\pm 5$	%
Pixel differential nonuniformity			$\pm 2.5$	%
Dark signal nonuniformity			5	mV
Dark signal response			5	mV
Conversion gain (high gain)		270		$\mu\text{V}/\text{electron}$
Conversion gain (low gain)		27		$\mu\text{V}/\text{electron}$
Usable full well capacity (high gain)		5200		electrons
Usable full well capacity (low gain)		52000		electrons
Saturation exposure (high gain)		60		mlux-sec
Saturation exposure (high gain)		9		nJ/ $\text{cm}^2$
Saturation exposure (low gain)		607		mlux-sec
Saturation exposure (low gain)		90		nJ/ $\text{cm}^2$
Nonlinearity			1	%
Pixel rate per port	0.1	8.0	32.0	MHz
Logic clock	0.1		40.0	MHz
Pixel count		2048		
Pixel size		$7 \times 7$		$\mu\text{m}^2$
Fill Factor		85		%

Table 2: Electrical Specifications **PDI-LNL2048S**,  $T_{int} = 100\mu\text{s}$ ,  $V_{DD} = 3.3\text{V}$ ,  $T = 25^\circ\text{C}$ 

Parameter	Com	Ind	Sci	CSci	Units
Dark current	12.0	2.0			e-/pixel/msec
RAI read noise (high gain)	5	5			electrons
RAI read noise (low gain)	10	10			electrons
MRDI read noise 16x oversampling (high gain)	1	1			electrons
RAI noise equivalent exposure (high gain)	46	46			$\mu\text{lux-sec}$
RAI noise equivalent exposure (high gain)	6.6	6.6			pJ/ $\text{cm}^2$
RAI noise equivalent exposure (low gain)	116	116			$\mu\text{lux-sec}$
RAI noise equivalent exposure (low gain)	16.6	16.6			pJ/ $\text{cm}^2$
MRDI noise equivalent exposure 16x oversampling (high pixel gain)	11.6	11.6			$\mu\text{lux-sec}$
MRDI noise equivalent exposure 16x oversampling (high pixel gain)	1.7	1.7			pJ/ $\text{cm}^2$
Dynamic range in MRDI mode	52K 94	52K 94			dB
Non-functional pixels	5	0			

# 1 Operation

The operation of the pixel array contained in PDI-LNL2048 is shown in Figure 1. Each pixel has a photodiode, a pixel amplifier, and a sample and hold circuit. Each pixel also contains one bit of the gain register and noise suppression circuitry which are not shown in the Figure. The S1 and S2 signals shown in the Figure are internally generated depending on the selected acquisition mode. The amplifiers and other pixel circuitry are organized into two halves, even (lower) and odd (upper), as shown in the block diagram on the first page.

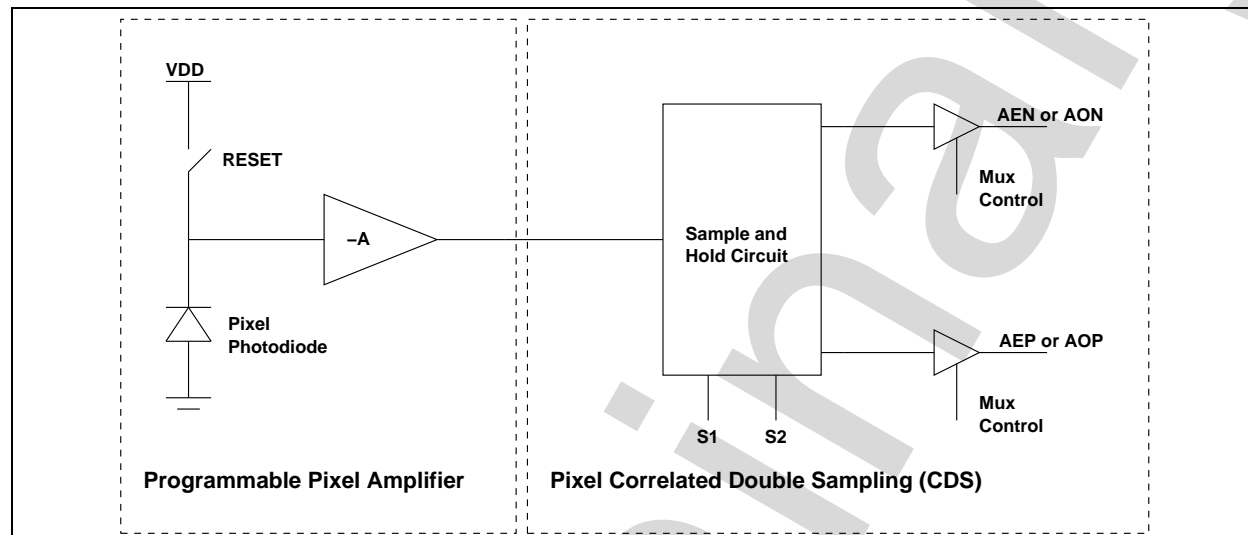


Figure 1: Pixel Schematic

Pixel transfer and/or reset is initiated when TX is pulsed for one clock cycle. All input signals are sampled on the rising edge of TCK. When a single-clock-cycle pulse is applied to TDI, it is serially shifted, on the rising edge of each TCK, through a 2052-bit pixel output enable shift register. The first two and last two bits are dummy pixels and the middle 2048 bits each act as an enable for the shift register bit's respective pixel output buffer. The output buffers are multiplexed (2048-to-1) onto the AEP and AEN pins, and/or the AOP and AON pins, depending on the interface mode. The pixel output enable shift register is clocked on the rising edge of TCK.

## 1.1 Acquisition Modes

The pixel circuits can be operated in four different data acquisition modes: RAI, SRDI, MRDI, and ROI. These modes select between different speed/noise tradeoffs to support a wide range of applications. In each mode, TX and TDI control sequencing.

The acquisition modes are selected by sampling the TX and PD pins on the first rising edge of TCK after TRSTN rises. Note that the normal functions of TX and PD are suppressed after TRSTN falls until one clock after TRSTN rises, i.e. after they have been sampled to determine the acquisition mode.

- **RAI — Read-out After Integration**

Differential pixel data is available for destructive read-out (current pixel value is destroyed by read-out) after photocharge integration is complete. This is the simplest mode. It achieves relatively low read noise and FPN, but it has a slower scan rate than other modes. TX starts and ends pixel reset and starts integration, and TDI ends integration and starts pixel read-out. Fixed pattern noise (FPN) may be removed by using the output signal processing described for the SRDI acquisition mode.

- **SRDI — Single Read-out During Integration**

Differential pixel data from the previous line is available for destructive read-out while the current line is integrating. SRDI mode can be faster than RAI mode since pixel data from the previous line is buffered for read-out while the sensor is integrating the current line. TX captures the integrated data, starts and ends pixel reset, and starts a new integration, and TDI starts pixel read-out of the previously-captured data.

In RAI and SRDI acquisition modes, the fixed pattern noise (FPN) in the differential output path can be removed by performing external chip level CDS on the pixel and calibration data. Therefore, each pixel value can be determined by calculating

$$S_{out} = (AEP_p - AEN_p) - (AEP_c - AEN_c), \quad (1)$$

where  $AEP_p$  and  $AEN_p$  are the pixel values on AEP and AEN respectively, and  $AEP_c$  and  $AEN_c$  are the calibration values on AEP and AEN respectively. In dual-port output mode, the odd pixel data will appear on AOP and AON instead.

- **MRDI — Multiple Read-out During Integration**

Single-ended pixel data can be read out multiple times during photocharge integration. MRDI mode provides the lowest noise through the use of oversampling. This mode is intended for applications that require very low read noise. Since the read-out is non-destructive, each pixel can be read out multiple times and averaging/oversampling techniques such as Fowler sampling can be applied to effectively reduce the read-out noise. TX starts and ends pixel reset and starts integration, and TDI starts pixel read-out.

- **ROI — Read-out On Integration**

Single-ended pixel data from the previously-scanned line is available on one of the differential output pins while the current scan line data is being integrated. ROI mode produces the highest line scan rate, sacrificing FPN and read noise. Similar to SRDI, ROI mode allows for a single read of each pixel after each integration period. The difference is in the operation of the pixel and output circuitry. In ROI mode, the CDS circuit is disabled and analog pixel data is single-ended. AEP and AEN, and AOP and AON, must be shorted together since pixel data toggles between the two every line. TX ends integration, captures the integrated data, starts and ends pixel reset, and starts a new integration, and TDI starts pixel read-out of the previously-captured data.

In MRDI and ROI acquisition modes, no calibration data is generated. Therefore data is read out single-ended and is available during the entire pixel read-out cycle. This allows the sensor to be read out twice as fast as RAI and SRDI acquisition modes.

- **Programmed mode —**

Data acquisition is performed using the sensor input pins only, i.e. no internal counters are used.

## 1.2 Pixel-Level Gain Control

Each pixel amplifier has bi-level digitally programmable gain and an anti-blooming drain. The pixel-level gain can be set either high,  $270\mu V/e$  sensitivity, or low,  $27\mu V/e$  sensitivity. The gain of each pixel amplifier is set by shifting in a string of 2052 bits into the pixel gain register using clock (TCK) and data input (TDI) while the interface mode pins select the GAIN register (IMODE[0:1] = 11). As in the pixel data enable shift register, the first two and last two bits in the gain shift register are for dummy pixels. High gain is selected with a logical low, and low gain is selected with a logical high. The initial condition of each bit in the gain register is logical low, i.e. high gain.

## 1.3 Interface Modes

The PDI-LNL2048 can be operated in four different interface modes: single-port output, dual-port output, gain register control, and JTAG programming. JTAG programming is presently supported only for use of programmed mode. These interface modes are controlled by pins IMODE0 and IMODE1. Interface modes are determined by sampling the IMODE0 and IMODE1 pins during the rising edge of TCK. Of the four possible combinations, two are used to access the pixel data enable shift register and thus send pixel data to the AEP and AEN and/or AOP and AON pins, one is to access the pixel gain register, and the last allows JTAG access to internal timing and operation registers.

In single-port output mode (IMODE[0:1] = 10), all pixel data is read from the AEP and AEN analog output port. In dual-port output mode, data from odd and even pixels are read from two output ports. AEP and AEN generate even pixel data, and AOP and AON generate odd pixel data. Dual-port output mode achieves twice the pixel throughput of the single-port output mode if the output ports are at their maximum bandwidth. While in either dual-port or single-port output mode, read-out of the sensor is always

initiated by pulsing TDI for one clock cycle. During each clock cycle one pixel is read out. The first two and last two pixels in the 2052 bit pixel data enable shift register are dummy pixels. In dual-port output mode (IMODE[0:1] = 01), both analog output ports are active for 2052 clock cycles.

## 1.4 Quantum Efficiency

100% fill factor is assumed when quantum efficiency is estimated.

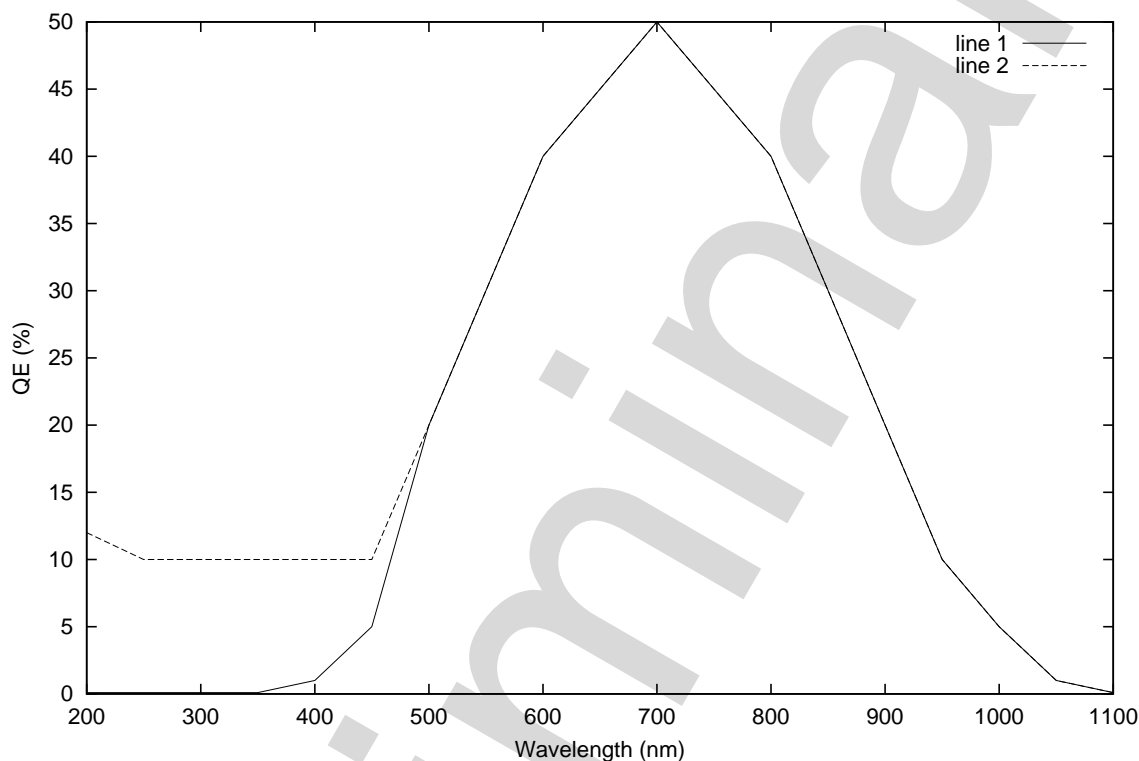


Figure 2: Quantum Efficiency

Note 1. Line 1 is for a front-illuminated sensor and line 2 is for a UV-enhanced sensor.

The User Chooses Either of Two Output Modes			
Single-Port Output Mode "Even" port is used. "Odd" port is not used		Dual-Port Output Mode Both "Even" and "Odd" ports are used	
Pixel data available ~30nSec after rising edge of each clock cycle.  External CDS calibration data available ~30Sec after falling edge of clock.  16MHz maximum data output rate.  The maximum data rate is determined by the sum of these two 30nSec analog output delays above.	this is config <b>1</b> RAI single output port	On the Even port, data for Pixel "N" becomes available ~30nSec after the falling edge of each clock cycle. Calibration data for that pixel becomes available ~30nSec after the falling edge of the next clock cycle.  On the Odd port, data for Pixel "N+1" becomes available one clock cycle after data for Pixel "N" became available in the Even port.  32MHz maximum data output rate.  The maximum data rate is determined by one analog output delay (1/30nSec), as opposed to two analog output delays for the single-output-port case to the left.	this is config <b>2</b> RAI dual output port
	this is config <b>3</b> SRDI single output port		this is config <b>4</b> SRDI dual output port
	this is config <b>5</b> ROI single output port		this is config <b>6</b> ROI dual output port
	this is config <b>7</b> MRDI single output port		this is config <b>8</b> MRDI dual output port

The User Chooses Any of Four Pixel Readout Modes		
Readout Mode Name	What It Is	Output Signal Type
<u>RAI</u>  Single Destructive Readout  Readout Occurs After Integration, Before the Next Integration Cycle Can Begin	Readout does not start until integration is complete. Integration does not resume until readout is complete.  On-chip control circuitry is off during pixel integration so as to minimize noise picked up by the pixels.  RAI is slower than some of the other modes because integration and readout occur sequentially rather than simultaneously.	Differential Output Signal
<u>SRDI</u>  Single Destructive Readout  Readout of an Integration Occurs During Next Integration Cycle	While a line is being integrated, the previous line is being read out.  This speeds up operation as compared to RAI.  As with RAI, readout of a given line does not start until integration of that line is complete.  Fixed pattern noise (FPN) is the same as in RAI mode, because external CDS is used just as with RAI.  Read noise, however, is degraded compared to RAI mode because clocking is performed on-chip during pixel integration.	
<u>ROI</u>  Single Destructive Readout  Readout of an Integration Occurs During the Next Integration Cycle	This is a single-ended-output version of SRDI.  Faster operation is achieved than is possible with SRDI, because the calibration circuit is disabled so as to devote internal circuitry solely to rapidly clocking out data.  Read noise & fixed pattern noise are degraded as compared to SRDI.  Reset in ROI mode requires 680 single-port clock cycles which is 21uSec at 32 MHz clock rate.  The resulting maximum line rate, as integration time approaches zero, is 47 KHz.	Single-Ended Output Signal
<u>MRDI</u>  Multiple Non-Destructive Readouts  Readouts are performed while the pixel is integrating	Pixels can be sampled multiple times during integration.  Read Noise and Fixed Pattern Noise can be averaged and further suppressed as compared to the other modes.  Read noise as low as 1 electron is achievable with high pixel gain setting and 16X oversampling on the "S" pixels (7umx7um), and 3 electrons on the "R" pixels (7umx200um).	The calibration circuit for external CDS is disabled

Figure 3: Summary of Standard Configurations