T-FinFET Mobility Enhancement from Process-Induced Stress and Compact Model Development

Wanjun Wang, * Jin He, Bing Xie, Guangjin Ma, Guoqing Hu, Chunlai Li, Daye Lin, Jingjing Liu, Ying Yu, Zhangyuan Chen and Zhiping Zhou

Peking University Shenzhen SoC Key Laboratory, PKU-HKUST Shenzhen-Hong Kong Institution, Shenzhen 518057, China
Tel: 15013563293
E-mail: frankhe@pku.edu.cn

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Abstract: In the advanced CMOS process lines, the process-induced stress is often used to increase carrier mobility so as to improve MOSFET performance. It also strongly affects the carrier mobility of T-FinFET as long as it is fabricated with the CMOS process as always done in experiment tunneling FET device. Here we report the effect of process-induced stress on mobility enhancement and a corresponding compact model. The layout dependence of T-FinFET’s carrier mobility due to process-induced stress is efficiently captured. The mobility model is verified for different layout dimensions for several stress-inducing process technologies through both process simulations and experimental data.

Keywords: nanometer T-FinFET, process technology, strain effect, performance enhancement, modeling

1. Introduction

The continued scaling of bulk MOSFETs for higher current drive is approaching the physical limit due to strong short-channel effect, low threshold voltage controllability and high leakage. Thus new process technology, new devices are being investigated to extend the Moore’s Law.

Among the new process technology, the process-induced stress is promising in enhancing the carrier transport and achieving higher current drives. Last few years have seen numerous efforts on introducing both biaxial and uniaxial stress in transistor to enhance the electron and hole mobility [1, 2]. However, there has been very little work to date on modeling layout dependent mobility enhancement due to process-induced stress. In addition, the efforts were focused mainly on the modeling of mobility change due to STI process [3]. On the other hand, among the proposed non-classical device structures, the double-gate MOSFET and FinFET, with very thin film body are strong contenders to the bulk MOSFETs due to superior short-channel-effect immunity, near-ideal sub-threshold slope, and low parasitic resistance and capacitance [4-6]. Following the ITRS prediction, the CMOS integrated circuit will approach 10 nm technology generation in two or three years [7], and Tunneling-FinFET (T-FinFET) structure is highly required for the IC production scaling from 10 nm down to 5 nm. It is well known that the combination of the strain effect and T-FinFET structure results in high performance match between N-type and P-type devices. Also, the traditional modeling approach is generally believed to be outdated due to the regional characteristics, a compact modeling for stress effect on T-FinFET mobility enhancement is highly required by engineers and circuit designers to optimize process control and device structure parameters.

In this paper, the stress induced mobility enhancement for the T-FinFET is studied and a
compact model for process-induced stress is developed. The model is non-process specific and can work for any stress-inducing process. Process simulations in this work are performed on T-FinFET using the process simulator TAURUS to develop the mobility model. The new model is then incorporated into the ULTRAS-T-FinFET mobility model. The model is finally verified with experimental data from various stress-inducing process technologies [8].

2. Channel Stress Analysis

It is well known that stress in silicon leads to band splitting and change of effective mass, resulting in mobility change. The fractional change in the local resistivity is linearly related to the local stress through the Piezoresistive Coefficients.

\[ \frac{\Delta \rho}{\rho} \propto S \quad \text{where } S \text{ is local stress} \quad (1) \]

Fig. 1 highlights the possible ways through which stress can be introduced into the channel in a regular T-FinFET process. Depending on the materials and the process conditions, the resulting stress in channel can be either compressive or tensile. In almost all these methods, the stress in the channel is non-uniform and varies along the channel length. Using Eq. 1, the change in channel mobility, taking into account the non-uniformity of stress in the channel, can be written as (L represents the set of layout variables)

\[ \frac{\Delta \mu}{\mu} \propto - \int_0^L S(x, L) \, dx \quad = S_{AVG}(L) \quad (2) \]

The four possible directions through which the stress can be transferred to the channel are S/D side, Gate-stack side, Spacer side of T-FinFET. Channel middle part stress (ex. SiGe buffer) is mostly uniform through the channel and independent of the transistor layout. Hence, it can be modeled simply via a constant. The other three directions need to be modeled individually. The total channel stress will be the sum of these four components.

2.1. S/D Side Stress

S/D side stress refers to the stress transferred from S/D region (Fig. 2). The stressor can be on top of S/D (ex. Capping layer), inside the S/D (ex. SiGe S/D), or adjacent to S/D region (ex. STI). To analyze this component, a 75 nm thick stressed nitride layer, with an internal stress of 1800 MPa, is deposited on the S/D area (Fig. 3a) for different transistor lengths (L), only showing the upper half part of the T-FinFET. A tensile nitride layer transfers tensile stress to the channel. As L increases, the stressor moves away from center of channel, which decreases the average stress $S_{AVG}$.

The channel length dependence of $S_{AVG}$ for S/D side stress can be semi-empirically modeled through (Fig. 3b)

\[ S_{AVG}(L) = A_1 + \frac{A_2}{A_3 + L}, \quad (2) \]
where $A_1$ denotes the long channel stress, while $A_2$ and $A_3$ control the increase rate of stress as $L$ decreases. To verify the S/D side stress model, SiGe S/D structure was simulated. 17% Ge was used in the S/D region. Compressive stress gets transferred to the channel. The $L$ dependence of $S_{AVG}$ for SiGe S/D can also be captured using Eq. 3 (Fig. 3c). The stressor in this case is inside the S/D region, unlike in Fig. 3a where it was on the top, indicating that Eq. 3 works for all S/D side stressors.

### 2.2. Gate-stack Side Stress

Stress can also get transferred from gate-stack into channel (Fig. 2). The stressor can be a layer on top of gate electrode (ex. Capping layer), the gate electrode itself, or the gate-stack. In order to study this stress transfer component, a gate electrode comprising of a stressed layer (SL) and an unstressed Poly-Si is used. Fig. 4a shows a simulated structure with 150 nm SL (with intrinsic stress of 1800 MPa) and 30 nm unstressed Poly-Si. Process simulations were repeated with different SL thickness. The results showed that the stressor has to be very close to channel to generate significant $S_{AVG}$ (Fig. 4b). The channel length dependence of Gate-stack side stress is captured through (Fig. 4b).

$$S_{AVG}(L) = B_1 + \frac{B_2}{B_3 + L} - \frac{B_4}{B_5 + L}$$

Fig. 3a. Process simulation to analyze S/D side stress in the upper half part of the T-FinFET.

Fig. 3b. Simulated average channel stress due to S/D side stress and model fitting in the T-FinFET.

Fig. 3c. Simulated average channel stress for SiGe S/D process and model fitting (stress here is compressive) in the T-FinFET.

Fig. 4a. Partially stressed gate electrode to analyze stress getting transferred from Gate-stack side in the upper half part of the T-FinFET.

Fig. 4b. Simulated average channel stress due to Gate-stack side stress and model fitting in the T-FinFET.

The non-monotonic behavior for Gate-stack side stress can be explained as follows. The volume of stressor is proportional to gate length. For very short $L$, stressor volume is small, making $S_{AVG}$ small. As $L$ increases, the increasing stressor volume enhances the channel stress. At longer $L$, the stress in the center of gate is relaxed. The maximum $S_{AVG}$ is observed at an intermediate $L$ where the relaxation effect begins to

dominate the stressor volume increase. S/D stress analysis showed that the stress decreases rapidly as channel length decreases. Hence, a combination of S/D side and Gate-stack side stress can provide stress (mobility) enhancements over a wider range of channel lengths.

2.3. Spacer Side Stress

A stressed sidewall spacer or any stressed film outlining the spacer can transfer stress to channel from spacer side (Fig. 2). Maximum stress transfer occurs when the spacer itself is stressed. Simulations showed that 2GPa stressed spacer transfers only 80 MPa stress (Fig. 5).

Any stressed film outlining the spacer will transfer even smaller stress to the channel, since it is further away from channel. This implies that this stress transfer component is negligible and can be excluded from the model.

3. Source/drain Length Dependent Model

In the previous section, stress dependence on the layout variable channel length (L) was studied. Using a similar approach, a model for Source/Drain length (LSD) dependence is now developed. LSD controls the length of S/D side stressor or/and the distance of S/D side stressor from the center of channel. Thus, the S/D side stress changes significantly with LSD. Other stress transfer components remain unchanged with LSD variation.

S/D side stress is sufficient to capture LSD dependence. Nitride stressor is deposited (same as in Fig. 3a) over a variable LSD. As LSD increases, SAVG increases and gradually saturates when the farther edge of stressor has no more impact on channel stress. LSD dependence can be captured by (Fig. 6)

\[ S_{AVG}(LSD) = \frac{C2}{C3 + LSD} \quad (5) \]

Fig. 5. Stressed spacer structure and simulated average stress for Spacer-side stress in a T-FinFET.

4. Mobility Enhancement Model and Verification

From the stress analysis, S/D side stress and Gate-stack side stress are needed to capture channel length dependence while only S/D side stress is needed to capture LSD dependence. Using Eq. 1-5, we can express the holistic mobility enhancement model for any stress-inducing process as

\[
\mu = \mu_0 \left( 1 + A1 + \frac{A2}{A3 + L} - \frac{A4}{A5 + L} \right) \left( 1 + B1 + \frac{B2}{B3 + LSD} \right)
\]

where \( \mu_0 \) represents any mobility model with no stress, A1-A5 model \( L \) dependence and B1-B3 model the LSD dependence. Substrate side stress can be modeled by A1, a constant correction term. A1-A3 can model S/D side stress. A1-A5 can represent either Gate-stack side stress or a combination of Gate-stack and S/D side stresses. All the parameters can be extracted by measuring the mobility enhancement as a function of channel length and S/D length. The proposed model was added to BSIM mobility model to enable further verification.

The complete model is verified against the capping layer process since it has all three layout-dependent stress components. The model (Eq. 6) agrees well with the capping layer process simulations for both L and LSD variation (Fig. 7a). Experimental data for capping layer process is obtained from [1], which reports mobility reduction for PMOS devices with a tensile capping layer. BSIM mobility model is first matched to the control wafer. The holistic mobility model (Eq. 6) was then added to BSIM model to capture the mobility change due to capping layer. Good fit was obtained to the measured mobility with capping layer using the holistic mobility model (Fig. 7b).
SiGe S/D process is very promising for PMOS mobility enhancement. Unlike the capping layer process, the stressor here is inside S/D region. Gain in the linear drain current was reported in [2] after correcting for Vg-Vt. The holistic model is able to match the measured gain in linear ID for different channel lengths (Fig. 8) through change of hole mobility.

5. Conclusions

The mobility enhancement through process-induced stress is studied and a compact model is developed and then verified for the T-FinFET. The developed model lends itself to an easy incorporation into any compact model through a simple modification of the mobility term. Channel length and Source/Drain length dependencies have been modeled. The approach used in this work can be extended to add other layout variables when need arises. The model has been verified against both process simulations and experimental data for a wide range of stress-inducing processes like Capping layer process, SiGe S/D process and STI process.

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