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The Design of Multi-channel Signals Source with High-speed and High-precision Based on FPGA

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Abstract: The multi-channel signals source that the structure is simple and flexible control is proposed in the article, with FPGA and high-speed D/A as its core. The choice of parts of apparatus, hardware constitution and design of software of the signals source are recommended here. Before the hardware designed, detailed theoretical analyses and quantitative description for the key factors on effecting the precision of signal source are given, and when debugging in hardware circuit is completed, on the base of analysis, errors estimation were verified with experimental results. It has provided high-precision signal related to the static and dynamic characteristics test accuracy of measured system for encoder and memory. By experiment and application it can meet the system requirements and has some theoretic and practical value. *Copyright © 2013 IFSA.*

Keywords: Multi-channel, Signals source, FPGA, High-speed, High-precision.

1. Introduction

There are more requirements to the output amplitude accuracy of the source signal, to the frequency accuracy and stability, to the number outputs and controllability of signals in modern electronic measurement. So we must design a signals source with producing large amounts of the standard signal and guarantee the high accuracy, high stability, maneuverability and operability of signals. The signals, with continuous phase transformation and frequency stability, can be controlled real-time in frequency, phase and amplitude.

The traditional signals source is an independent source, depending on hardware mainly, without computer participating in. It has complex hardware design and hasn't played software functional fully. In the system, the signals source is programmed by software. By that, these Standard signals' waveform are quantified and the quantitative data are preset in memory. The Communications between the system and computer rely on USB2.0.

2. Analysis of Accuracy of the Signals Source

Provided high-precision signals, it related to the static and dynamic characteristics test accuracy of measured system. Generally, the factors that affect

the accuracy of the sources are in the following mainly: a variety of circuit noise, static and dynamic parameters of DA converter, Operational Amplifier's zero-drift and static and dynamic accuracy, resistance deviation and resistance drift in resistor network, shut-off and conduction delay of electronic switch, no synchronization between electronic switch and DA conversion and so on.

2.1. The Electronic Switch's Effect in Accuracy

Signal output accuracy is required to reach 0.01 % in the system. So signal amplitude of capacitance C in a channel after t1charging should be greater than full range of 99.99 %.And in other channel switching process, the leakage voltage in the channel after t2 discharging should be less than full range of 0.01 %.

In the design we use ADG506 as electronic switch. It's contact resistance is about 400 Ω in the working and is more than 1kM in the else. We can Use the capacitance for polypropylene capacitor, their leakage resistance is greater than 1 kM. LM324, the input impedance is greater than 250 M, is adopted as Operational amplifier in the design. Therefore, the whole leakage resistance of the total device is about 250 M. The equivalent circuit is shown Fig. 1.

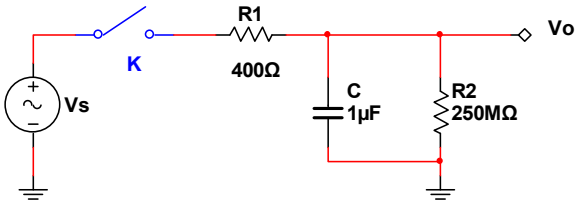

Fig. 1. The equivalent circuit.

From the Fig. 1, we can know that capacitance C can be charged through R_1 when the switch is turn-on; otherwise, capacitance C will discharge through Leakage resistance R_2. The charging process is:

$$U_O = (U_S - U_O^{'})(1 - e^{-\frac{t_1}{\tau_1}}) + U_O^{'}, \quad (1)$$

When Corrugated coefficient is 1‰, there is $1 - e^{-\frac{t_1}{\tau_1}} \geq 0.999$. In ADG506, Not synchronized and the switching delay time should be less than 400ns. So $t_S \approx 0.4\mu s$, Then there is:

$$C \geq \frac{-4\mu s}{R_1 \times \ln 0.001} = \frac{-4\mu s}{400 \times 6.9} = 1449\,pF$$

and

$$C \geq \frac{-64 \times 4\mu s}{R_2 \times \ln 0.999} = \frac{-256\mu s}{10^{13} \times \ln 0.999} = 2.56\,pF$$

To meet the design requirements, we choose 102 capacitance.

2.2. The PCB's Effect in Accuracy

Crosstalk is a Noise voltage signal that is brought owing to electromagnetic coupling between adjacent signals line, namely, the energy is coupled by a line to another line. To the higher signal accuracy system, crosstalk noise can further reduce signal quality and margin to other transmission line, taking into account accuracy, this paper focuses on the peak output voltage of crosstalk noise.

$$V_{FE} = \frac{1}{2} L_S (Z_0 C_m - \frac{L_m}{Z_0}) \frac{d\upsilon_s}{dt} \quad (2)$$

$$V_{NE} = K_{EN} \upsilon_0 \quad (3)$$

Young-Soo Sohn has brought out experience formula of C_S, L_S, C_m and L_m and approximate impedance formula of single line in PCB. As follows formula (4), (5), (6), (7), (8).

$$\frac{C_t}{\varepsilon} = [1.15(\frac{W}{H})^{0.963} + 1.07(\frac{T}{H})^{0.049}] + exp(-3.52\frac{S}{H})[0.75(\frac{W}{H})^{0.25} + 2.7(\frac{T}{H})^{1.34}], \quad (4)$$

$$\frac{C_m}{\varepsilon} = 1.17(\frac{W}{H})^{0.083}(\frac{S}{H} + 0.402)^{-0.78} + (\frac{S}{H} + 1.32)^{-0.8}[-1.36(\frac{W}{H})^{0.037} + 0.227(\frac{T}{H})^{0.98}], \quad (5)$$

$$\frac{L_s}{\mu_0} = 3.71(\frac{H}{W})^{0.041} + 0.018(\frac{H}{W})^{-0.73} - 3.39(\frac{H}{T})^{-0.0006} + exp(-1.89\frac{S}{H})[0.75(\frac{H}{W})^{-0.0052} - 0.84(\frac{H}{T})^{-0.0026}], \quad (6)$$

$$\frac{L_m}{\mu_0} = [-0.415(\frac{H}{W})^{-0.16} - 2.38(\frac{T}{W})^{1.18}] + (\frac{S}{H} + 1.07)^{-2.6} + (\frac{S}{H} + 0.89)^{-2.03}[0.418(\frac{H}{W})^{0.13} + 1.37(\frac{T}{W})^{1.09}], \quad (7)$$

$$Z_0 = \sqrt{L_s / C_t} \quad (8)$$

Therefore, from the formula (4), (5), (6), (7), (8), we can see distal crosstalk interference will be eliminated when $Z_0 C_m - L_m / Z_0 = 0$ and $Z_0 = \sqrt{L_s / C_t}$ or $L_m / C_m = L_s / C_t$. So we are not layout line between the pin of integrated chip in the PCB and should add earth wire or use wide wire around in easy interference parts. Do not forms a loop in any signal, if inevitable, must be allowed to loop area as small as possible. To improve anti-interference ability of the system we use 4 layer boards in PCB in the design.

2.3. The DA Effect in Accuracy

Based on high-precision, we must select a high-resolution, high-precision D/A Converter in the design. As is known to all, D/A converter the analog output rely ultimately on voltage reference source Predictably, voltage references of the output voltage is directly influence to the precision and stability.

We use A/D768AR, a high-speed 16-bit digital-to-analog converter, as AD In the system. The AD768 may be used in either current-output mode with the output connected to a virtual ground, or voltage-output mode with the output connected to a resistive load.

In current output mode:

$$I_{out} = (DACCODE / 65536) \times (I_{REFIN} \times 4), \quad (9)$$

In voltage output mode:

$$V_{out} = I_{out} \times R_{LOAD} // R_{LAD}, \quad (10)$$

I_{REFIN} is the current applied at the I_{REFIN} pin, determined by V_{REF} / R_{REF}. Substituting for $\boldsymbol{I_{out}}$ and I_{REFIN},

$$V_{out} = -V_{REF} \times (DACCODE / 65536) \times 4 \times [(R_{LOAD} // R_{LAD}) / R_{REF}] \quad (11)$$

For application flexibility and multiplying capabilities, the reference amplifier is design to offer adjustable bandwidth that can be reduced by connecting an external capacitor from the NR node to the negative supply pin, $\boldsymbol{V_{EE}}$. This capacitor lim it's the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier. The voltage output is then a function of the ratio of $(R_{LOAD} // R_{LAD}) / R_{REF}$, allowing for cancellation of resistor drift by selection of resistors with matched characteristics.

3. The Programmer of System and Hardware Constitution

This system has put forward a new method of signal source realization. Using the principle of DDS, computer technology is been into the signal source implementations Through the USB bus. The hardware design will be softened using the power of computer. FPGA is used as center logic control. Hardware circuit principle diagram Fig. 2.

The basic principle for the signal source: Computers send forth Commands and waveform number to FPGA by the USB interface module. Then the FPGA receive computer orders and accomplish the following two tasks according to different command. The first, in the controlling of FPGA the waveforms are read form FIFO and are stored to SRAM. The second is to control the waveform read an SRAM data to the D/A converter, and control the D/A converter finishes conversion.

In the D/A conversion process, the advancement of the memory address pointer should be synchronized with the multi-switch forward address pointer. AD824 is chosen in the design, the AD824 is a quad, FET input, single supply amplifier, featuring rail-to-rail outputs. Its slew rate is $2V / \mu s$, the ability of the output to swing rail-to-rail enables designs to build multistage filters in single supply systems and maintain high signal-to-noise ratios. When peak-to-peak value occurs in adjacent two channels signal to overact next channel stable output demands $(8V / 2V) / \mu s = 4\mu s$, so electronic switch must be opened after $4\mu s$ in the D/A conversion ending, otherwise channel interference will arise.

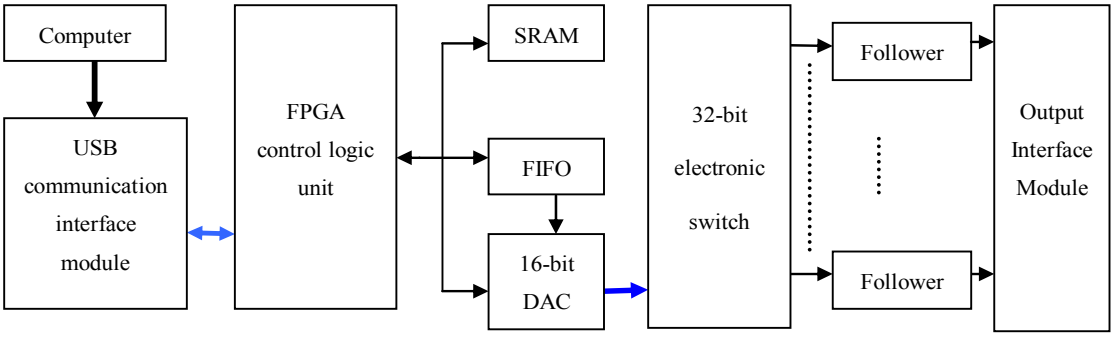

Fig. 2. Source hardware principle diagram.

4. The Design of Logical Control Unit in FPGA

As the center logic control devices of the signal source, FPGA has the following functions: to analyze Communication Protocol between the system and PC; to control storage and read of waveform data; to control DA conversion and electronic switch address propulsion; to control signal generator; to control impedance test and so on. The program control flow chart is as shown in Fig. 3.

Limited by the USB data transfer, each received 18 valid data which is truly effective data bits $D_7 \sim D_0$. Because there are 16 bit waveforms data in the signals source, the device must receive two effective data to synthesize a 16-bit waveform data which is sent in accordance with the first low 8 bits, then the high order 8 bits. The PC issue data in accordance with the address-Command-Data. So, when the system is working, to determine whether the received address matches the address for the system, if it is , then to judge the specific order form of the second 18-bit data. If the data are download command flag, to set write signal of FIFO is valid, the valid data has been received at this time is the waveform data. And, a 16-bit waveform data, integrating the before low 8-bit data and the after low 8-bit data, will be written into FIFO.

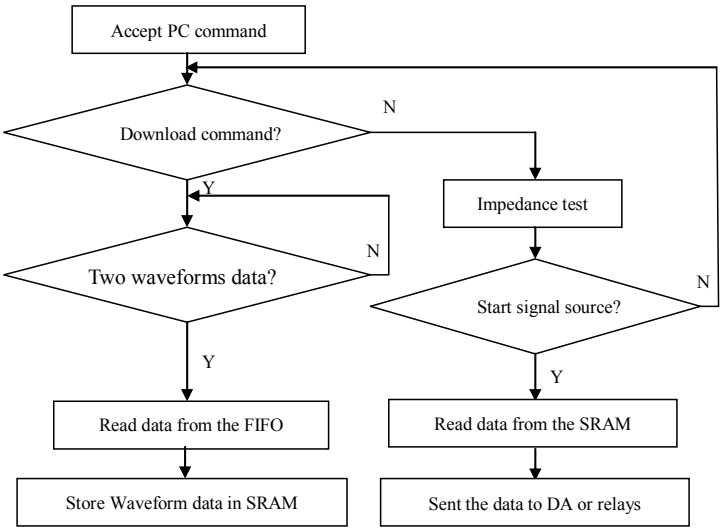

Fig. 3. Program flow chart of FPGA.

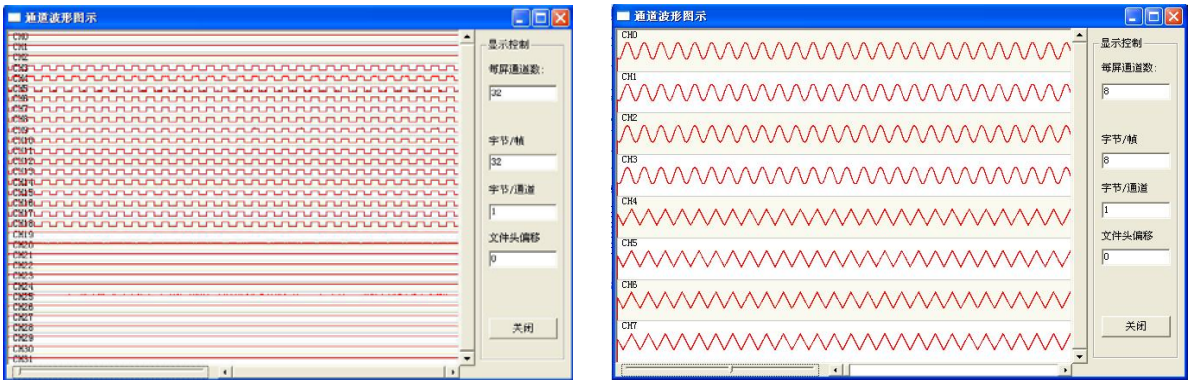

Fig. 4. Self-test wave of signal source.

5. Conclusion

The system has been put into use, and is involved in some large test. In the experimental process, it has provided high-precision signal for encoder and memory. It provides the basis for developing high-accuracy encoder and memory. Fig. 4 is self-test wave of signal source; we can be seen the design can conform to the system requirements.

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