

2D Numerical Analysis of Metal/Insulator/Thin Film Silicon Systems for TFT's Applications: Investigation of Active Layer Properties on Quasi-Static Capacitance

¹ Hadjira TAYOUB, ¹ Asmaa BENSMAIN, ¹ Baya ZEBENTOUT,
¹ Fatima MAACHOU, ¹ Zineb BENAMARA
and ² Tayeb MOHAMMED-BRAHIM

¹Applied Microelectronic Laboratory, Faculty of Engineering, University of Sidi Bel Abbes,
22000, Algeria

² IETR-Microelectronics Group, UMR6164, University of Rennes I, 35042, Rennes, France

¹ Tel.: 00213 48 55 12 84, fax: 00213 48 55 12 84

E-mail: Hadjira.tayoub@gmail.com

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Abstract: Thin Film Transistors (TFTs) are used as pixel switching and driving elements in active matrix liquid crystal displays. High quality of active layer on glass substrates associated with low temperatures is necessary for fabricating high performances and long-term reliable TFTs. According to the deposition conditions at low temperatures, the thin silicon layer presents an inhomogeneous structure that consist of a random superposition of grains of different sizes, where grains boundaries parallels and perpendiculars appear containing a high density of states in the energy forbidden gap. The purpose of this work is to study the impact of granular structure of active layer on the electrical behavior of Metal/Insulator/TFS systems. We have developed a 2D-numerical code based on the resolution of Poisson's equation. The application of gate bias allows to simulate the quasi-static capacitance characteristic $C(V_G)$. The effect of intergranular DOS, interface states and grain size on the quasi-static capacitance is investigated. Copyright © 2014 IFSA Publishing, S. L.

Keywords: Quasi-static capacitance, DOS, 2D-numerical simulation, Grain boundary, Grain size.

1. Introduction

Recently polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have emerged as the device of choice for many applications with desirable electrical characteristics. These include, the integrating driver circuits and pixel transistors on the same glass panel, active matrix liquid crystal displays (AMLCDs) in notebook computers and high definition televisions (HDTVs), printer heads, scanners, synchronous random access memories (SRAMs), image sensors,

high performance electrically erasable programmable read only memories (EEPROMs), three-dimensional large scale integrated (LSI) circuits and system-on-panel applications [1]. This is because the field effect mobility in polycrystalline silicon is significantly higher (by two orders of magnitude) than that in amorphous silicon [2]. However, issue of poly-Si TFT is the main constraints toward the applications due to the granular structure of poly-Si which degrades performance and reliability. The polycrystalline layer consists of several

crystallites separated by grain boundaries. Crystallites are made of monocrystalline silicon, and have the classical properties generally attributed to this material. The small grains polycrystalline silicon has grain boundaries randomly distributed in the entire polycrystalline layer.

The main objective of this paper is to use a program based on the two-dimensional numerical solution of Poisson's equation using finite-difference method with non-uniform mesh sizes for simulate The response of quasi-static capacitance versus gate voltage $C(V_G)$ of Metal/Insulator/TSF. The investigation is performed according to intergranular DOS, number of grain boundaries, grain size as well as the interface states. In this paper, we first describe the physical and numerical method based on 2D-geometric model of thin silicon film. Next, we present the results of numerical simulation with comments.

2. Main Equations for Computation of Quasi-Static Capacitance $C(V)$

2.1. 2D-Domain Simulation of Al/SiO₂/pc-Si Capacitance

The structure of thin silicon film is dependent on the technology used to form the material. To model our structure, we take into account the LPCVD technique followed by the solid-phase crystallization (SPC). When the polycrystalline film is obtained after SPC of amorphous silicon film, its structure is columnar. Indeed, the SPC phenomenon of growth begins by the formation of very small grains with different crystalline orientations. Then these grains compete during the growth so that a columnar structure occurs. A possible model is to consider the pc-Si film formed by 2 regions separated by a horizontal grain boundary. The bottom region is formed by grains with small size and the structure of the up-region is columnar (Fig. 1 a). Since the parallel grain boundary is away from the Insulator/pc-Si interface where the variations of surface potential

occur, it will not impact on the calculated capacitance of our structure. Therefore, two-dimensional geometry is used to model well the columnar grain structure of pc-Si.

The pc-Si layer is described by introducing equally single-crystalline grains, L_G sized spaced by grain boundaries, depicted as thin amorphous silicon layer with a width of 1 nm [3], which are perpendicular to the growth surface. Because of the complexity of the structure model and the limited number of points in programming language, the number of perpendicular grain boundaries is ranging from 1 to 15. Therefore, the computed capacitance is confronted to that realized at low temperatures consisting of aluminum gate/SiO₂ insulator/ pc-Si deposited on a monocrystalline silicon (c-Si) substrate highly doped. The manufacture of this device is crucial to optimize the quality of the active layer and the interface before launching complete process of TFT transistor intended for a certain application. The Fig. (1.b) illustrates a description of the structure with dimensions and doping concentration for each region.

2.2. Numerical Method

In order to simulate the variation of the quasi-static capacitance characteristic $C(V_G)$ of pc-Si TFT's, Poisson's equation (1) is numerically solved in two dimensions:

$$\nabla(\varepsilon \text{grad} \Phi(x, y)) = -q(p(x, y) - n(x, y) + N_D^+ - N_A^- + \sum N_T(x, y)) \quad (1)$$

where:

ε : The permittivity of each material;

$n(p)$: The free electrons (holes) density;

Φ : The electrostatic potential;

$N_D^+(N_A^-)$: The ionized donor (acceptor) density;

$\sum N_T$: The sum of the different ionized trap centers present in the material.

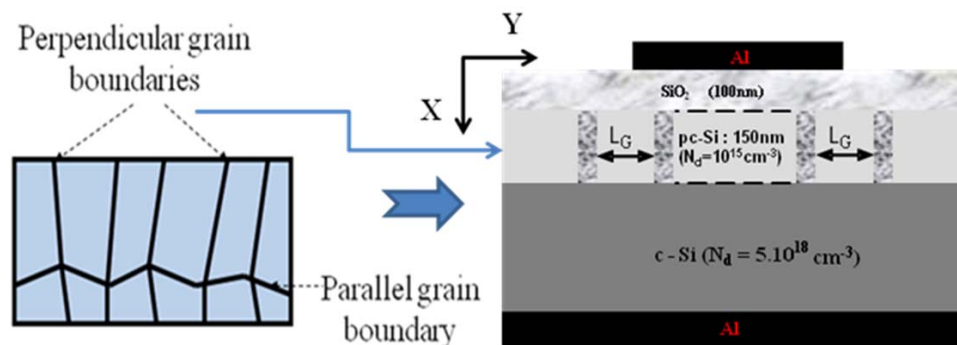


Fig. 1. (a) Schematic cross section of low temperature polycrystalline silicon (LTPS); (b) 2D-geometrical of the simulated structure.

The total capacitance of Al/Oxide/pc-Si structure is defined by:

$$C = \frac{dQ_m}{dV_G} = -\frac{dQ_{sc}}{dV_G}, \quad (2)$$

where Q_m and Q_{sc} are the electrical charges developed at the gate and pc-Si respectively.

The resulting charge capacitance value is expressed as a function of the electrostatic potential Φ which is deduced from a numerical integration of Poisson's equation:

$$Q_m = \varepsilon_{ox} \iint_{\Sigma} \overrightarrow{grad\Phi} \big|_{x=0} \cdot \vec{n}.ds, \quad (3)$$

$$C = \varepsilon_{ox} \cdot L \cdot \frac{\left(\sum_{j=1}^N \left\{ \left(\left[\frac{d\Phi}{dx} \right]_{x=0} \right)_j + \left(\left[\frac{d\Phi}{dx} \right]_{x=0} \right)_{j+1} \right\} \times \frac{pas(j)}{2} \right)_{V_G} - \left(\sum_{j=1}^N \left\{ \left(\left[\frac{d\Phi}{dx} \right]_{x=0} \right)_j + \left(\left[\frac{d\Phi}{dx} \right]_{x=0} \right)_{j+1} \right\} \times \frac{pas(j)}{2} \right)_{V_G + \delta V_G}}{\delta V_G}, \quad (4)$$

$\frac{d\phi}{dx}$: The slope of the potential between points 1 and 2;

δV_G : Increment of gate bias taken at 20 mV.

Partial differential equation (1) is solved by using the finite differences defined by Gummel's decoupling method.

For this, the equation is discretized on a variable mesh (strongly refined at interface and grain boundaries) then linearized to first order. The numerical resolution is based on the method of relaxation by line and by column. The tridiagonal character of the matrix leads us to use the Gauss's elimination method.

This allows the plot of the normalized capacitance as a function of gate bias, illustrating the three regions: accumulation, depletion and inversion of the structure. The quasi-static capacity is given by the following equation:

these states are considering in term N_T of the volumic charge concentration in Poisson's equation. More details including the hypotheses and parameters values of the density of states are reported in reference [5].

2.3. Density of States at the Grain Boundaries

The usual density of states (DOS) model in the amorphous silicon [4] is used to describe the distribution of the states inside the forbidden band-gap of grain boundaries and at the Oxide/pc-Si interface.

It is consisted of two decreasing exponential distributions for the valence N_{TBV} and the conduction N_{TBC} band tail and two correlated Gaussian distributions for deep defects introduced by dangling bonds N_{DB} as well as the discrete states due to uncontrolled impurities with single level trap N_{SLT} for donor and acceptor type (Fig. 2). The total charge of

3. Results and Comments of Numerical Simulation

Numerical values for the physical parameters as the permittivity, the electron affinity, the densities of states in the conduction and valence band edge, the gap energies in the crystallites and in the grain boundary are taken from the literature.

The first result allowed us to verify the 2D plot of the electrostatic potential (Fig. 3a) and the energy band diagram at thermodynamic equilibrium in the X and Y direction (Fig. 3b).

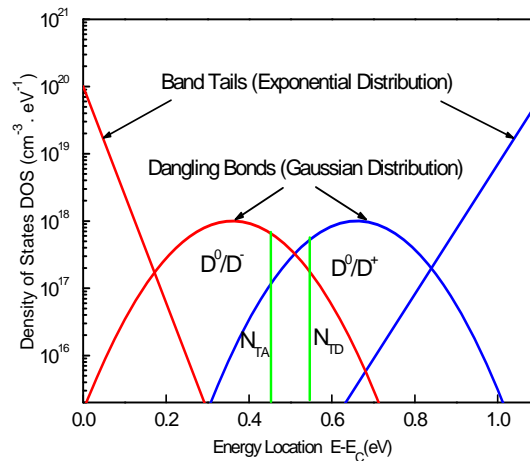


Fig. 2. Density of States (DOS) in the gap of the amorphous grain boundaries regions.

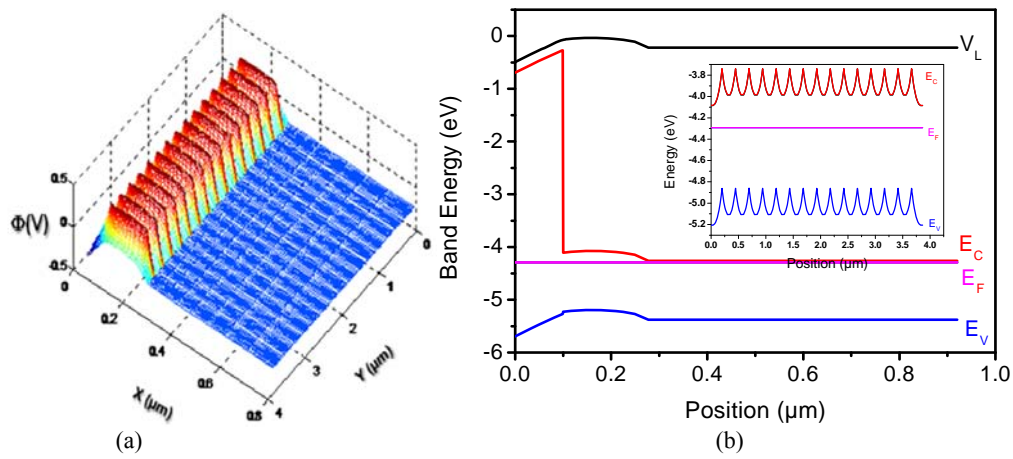


Fig. 3. (a) Distribution of electrostatic potential; (b) Energy band diagram of Al/SiO₂/pc-Si structure.

These figures demonstrate the appearance of a height of potential barrier at the grain boundaries with crystallites partially depleted due to the presence of a localized DOS at grain boundaries. In this case many electrons will be trapped at grain boundaries leading to increase the distance between conduction band and Fermi level except for extreme areas. The effect of granular structure, DOS inside grain boundaries and interface on the quasi-capacitance is given in the following sections.

3.1. Effect of Granular Structure

Fig. 4 shows the effect of grain boundaries' number on the quasi-static capacitance of pc-Si active layer, increasing the number of grain boundaries allows to find the $C(V_G)$ curves usually measured on Al/SiO₂/pc-Si structure where the capacitance is lifted upwards and remains insensitive to the applied voltage in inversion mode. A similar behavior of the quasi-static capacitance was noted when the grain size L_G decreases. In fact, a structure with wider grain size has a higher normalized capacitance and a same than with crystalline silicon(c-Si). This

phenomenon was largely explained by SETO model which stipulates that the decrease in grain size implies a great trapping efficiency of free carriers making a total desertion of grains.

3.2. Effect of Density of State (DOS)

Now, we analyze the effect of the single-level traps, the dangling bonds and the interface states on the quasi-static capacitance. Let us notice that, traps due to band tail states are less effective than the dangling bonds and the discrete levels. This can be explained by the fact that for doping $<10^{17} \text{ cm}^{-3}$, the Fermi level will be constantly away from the maximum of the acceptors and donors exponential distributions then it will be blocked by the Gaussian associated with dangling bonds which are located adjacent the middle of the band gap and the same for the discrete levels so we have not observed any effect of the band tail states on the curve of quasi-static capacitance. In the following, we present only the results of the other parameters.

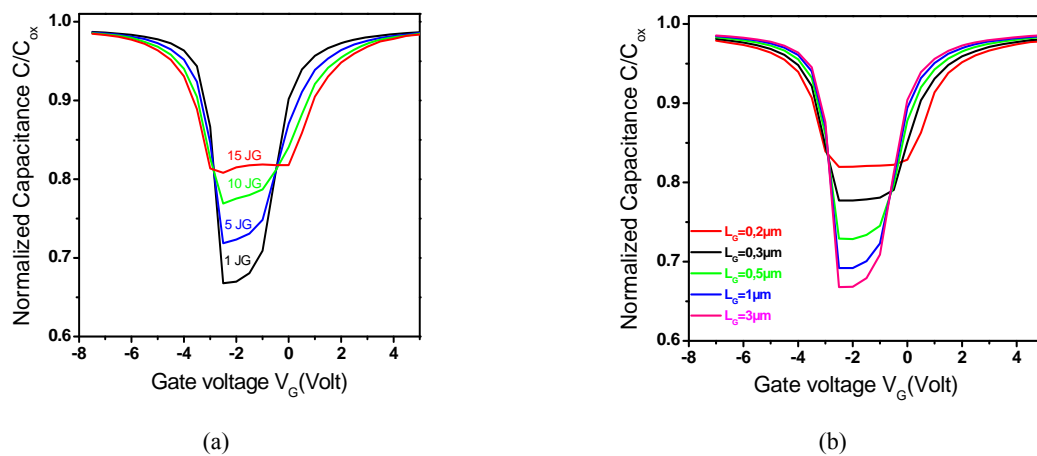


Fig. 4. The variation of quasi-static capacitance with the gate voltage for different number of grain boundaries (a), and grain size L_G (b).

3.2.1. Influence of Dangling Bond Parameters

The following figure shows that the increase in dangling bonds density N_{DB} (donor and acceptor) enhances the trapping of free carriers so the accumulation and the inversion becomes more difficult which implies the enlargement of $C(V)$ curve that will be pushed upward. We may note also that the increase in the standard deviation σ_{DB} makes the Gaussian overlap inevitable and trapping greater.

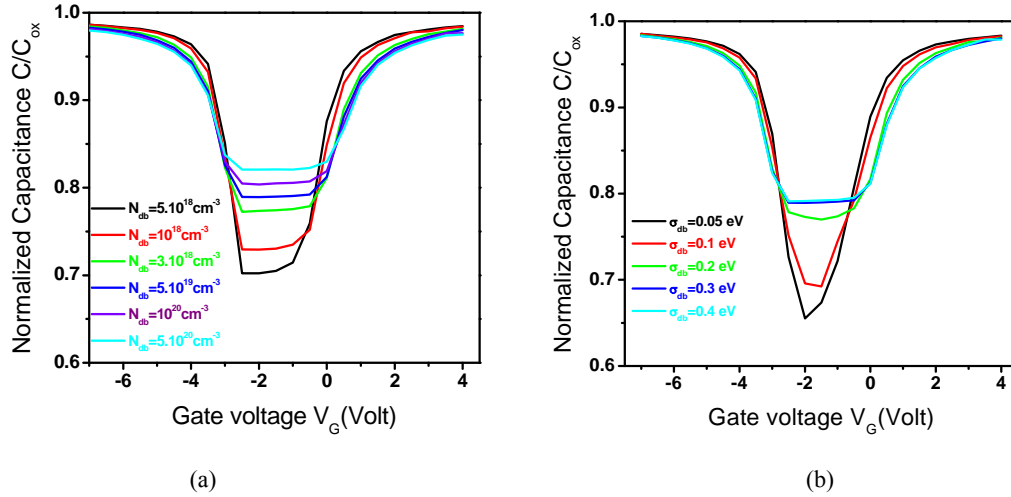


Fig. 5. The variation of quasi-static capacitance with the gate voltage for different N_{DB} (a) and σ_{DB} (b).

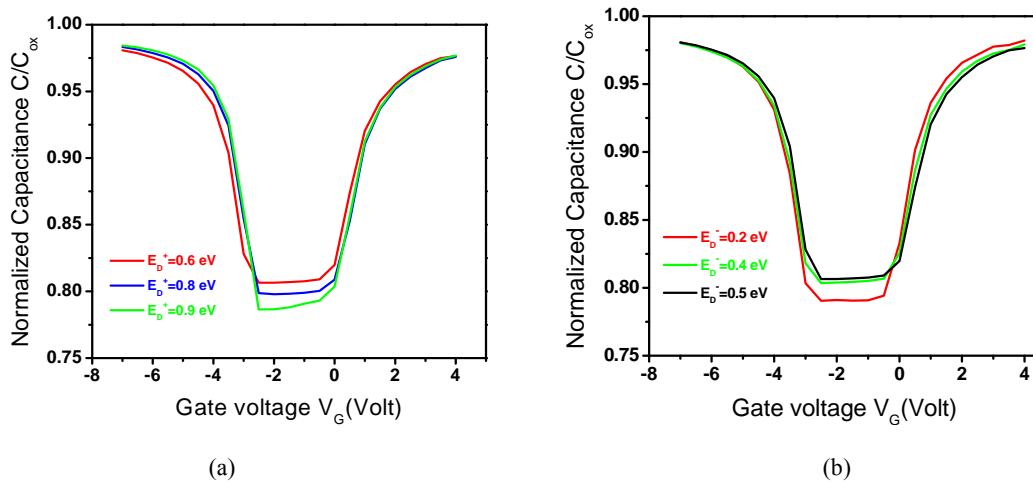


Fig. 6. The variation of quasi-static capacitance with the gate voltage for different E_{dp} (a) and E_{dm} (b).

3.2.2. Effect of Discrete Level Parameters

The shape of the $C(V)$ curves in Fig. 7 represents the effect of the density of acceptor and donor discrete traps on the quasi-static capacitance, these curves are superposed in accumulation mode for acceptor level trap and inversion mode for donor level trap. The consideration of the two types of traps reflects the experimental $C(V)$ curves based on the pc-Si.

In general, experimental curves of pc-Si quasi-static capacitance show a curve pushed upward but these curves do not reflect the experimental curves

found. Fig. 6 shows the influence of the effective energy levels on the quasi-static capacitance. When the gap energy between the two Gaussian centers increases the traps density move away from the midgap and the probability of capturing an electron or hole decreases. When E_{dp} fixed to 0.6 eV , we note that the trapping efficiency increases when E_{dm} approaches to the midgap and vice versa.

The defects have an amphoteric nature this is why taking into account simultaneous simulation of these states meet well the experimental curves.

Fig. 8 shows the variation of quasi-static capacitance with the gate voltage for different value of the density of discrete traps acceptor and donor simultaneously and the influence of acceptor and donor discrete traps energy on the quasi-static capacitance. The remoteness of these traps density of discrete traps N_{TA} and N_{TD} promotes trapping of free carriers. We may obviously show that the remoteness of these states from the midgap facilitates the transport of free carriers.

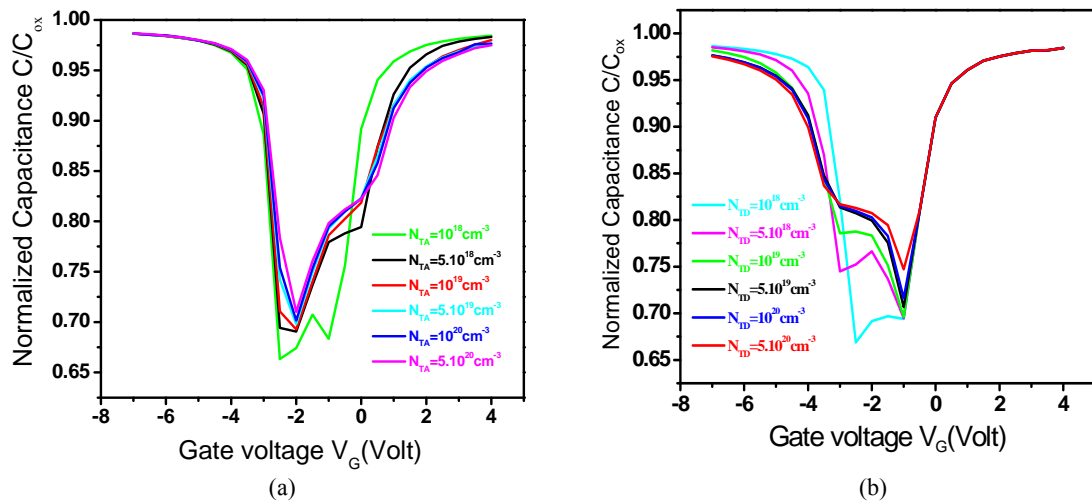


Fig. 7. The variation of quasi-static capacitance with the gate voltage for different N_{TA} (a) and N_{TD} (b).

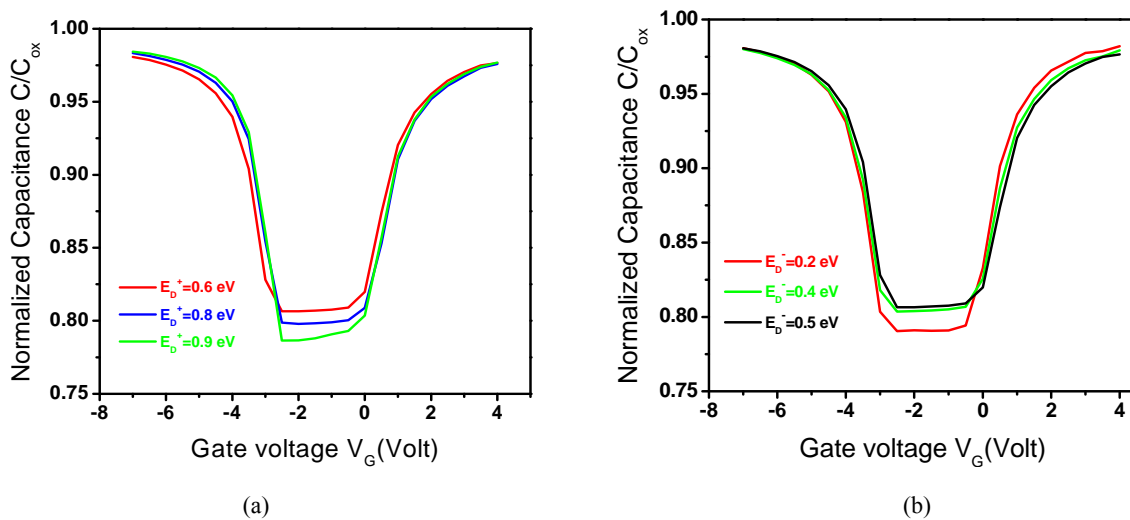


Fig. 8. The variation of quasi-static capacitance with the gate voltage for different N_{tja} and N_{tjd} (a); E_{TA} and E_{TD} (b).

3.2.3. Effect of Interface Density of State

The effect of the density trap states on the quasi-static capacitance as a function of voltage gate V_G is shown in Fig. 9. We note that the introduction of these states at the $\text{SiO}_2/\text{pc-Si}$ interface gives a shift effect of the $C(V)$:

1. To the left for donor type;
2. To the right for acceptor type.

3.3. Effect of Thickness of Polysilicon Layer

The Influence of polysilicon active layer's thickness L_c and the result where silicon or nitride are used as a gate dielectric on the quasi-static capacitance is shown in Fig. 10. The decrease of the thickness pull up the curve $C(V)$ and shift it to the left because of the effect of the defects that are important, it overcomes by the use of Si_3N_4 as a gate insulator.

4. Conclusions

The 2D geometric model of pc-Si active layer we have adopted for reporting the columnar growth of grain boundaries by LPCVD technique deposition, the two-dimensional modeling we have developed is based on the numerical solution of Poisson's equation, it allows us to well investigate the behavior of quasi-static capacitance of Metal/Dielectric/TFS systems as function of granular structure (number of grain boundaries and grain size), density of state localized at grain boundaries and $\text{SiO}_2/\text{pc-Si}$ interface in particular dangling bonds and discrete levels of trap states.

It has been found that the device performances based on pc-Si depends on the layer quality:

1. Traps resulting from defects at grain boundaries have an effect of pushing back the $C(V)$ curves upwards;
2. Interface traps have an effect of shifting the $C(V)$ curves to the right or to the left according to their type.

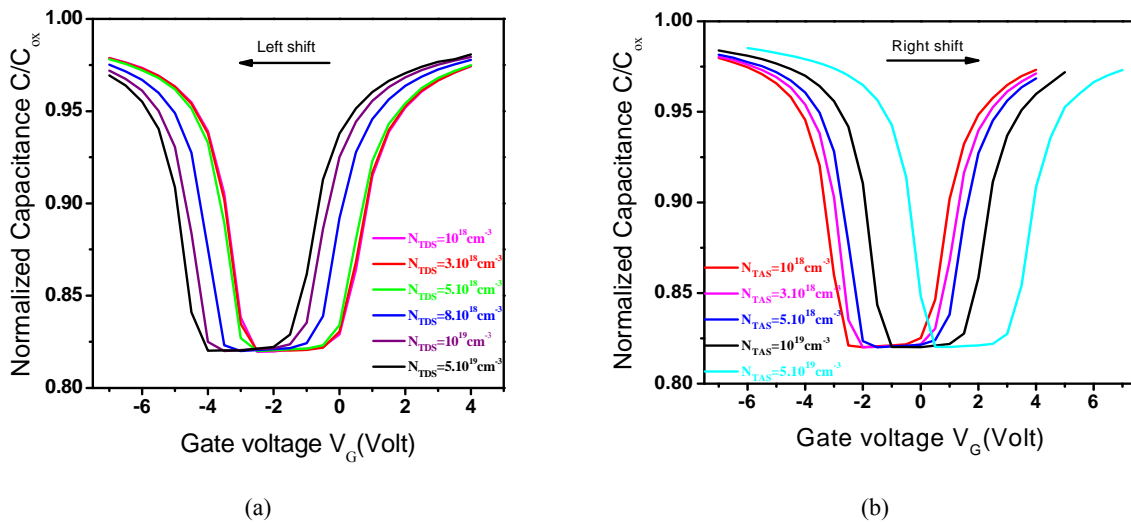


Fig. 9. The variation of quasi-static capacitance with the gate voltage for different N_{TDS} (a) and N_{TAS} (b)

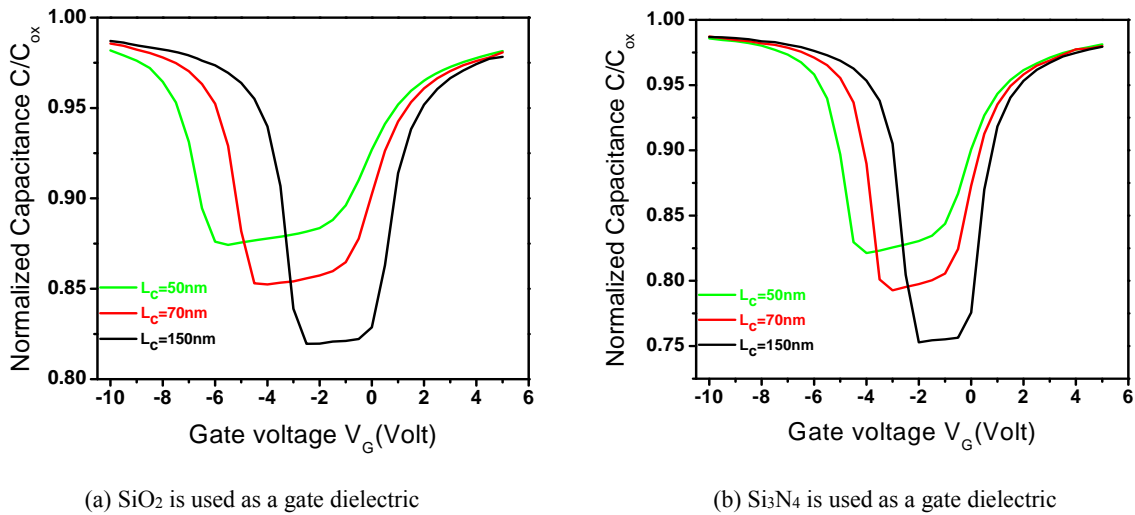


Fig. 10. The variation of quasi-static capacitance with the gate voltage for different L_c .

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