Design and Application of Counter’s Interface IP Core Based on Avalon Bus

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Received: 15 August 2013 /Accepted: 25 October 2013 /Published: 30 November 2013

Abstract: With the wide application of the NIOS II soft-core processor based on FPGA in the control field, the research of the interface IP (intellectual property) core between NIOS II’s Avalon bus and peripheral is very valuable. It combines FPGA and realizes the function of encoder pulses’ shaping, filtering, frequency multiplication, checking phase, counting and latching in this paper, then it makes use of Verilog language to finish the design of counting model and Avalon bus’s interface IP core, finally it takes SOPC (programmable on-chip system) technology to customize the NIOS II soft-core processor. Practical application shows that the design is stable and reliable, it not only can effectively and accurately obtain the pulse signal, and also to simplify the circuit. Copyright © 2013 IFSA.

Keywords: NIOS II soft-core processor, Encoder, FPGA, Avalon bus.

1. Introduction

With the FPGA performance getting higher and higher, the stronger data acquisition advantage of FPGA becomes more obvious in the control field, which make up for the IO port shortcoming of CPU [1-2]. In the past of servo driver’s design, most of the speed signals acquisition is completed by the encoder, where the encoder count module normally is constituted by the counter chip with other chips. This makes the design of peripheral circuits become Complicated, at the same time, it takes up more FPGA IO ports, which results in a lack of IO resources, therefore, we can completes the design of counter model in the FPGA.

In order to complete the encoder pulse signal acquisition, the design can adopt this scheme: we can customize a NIOS II soft-core processor in the FPGA based on the SOPC technique, it takes advantage of the rich internal resources of the FPGA to realize encoder counter model’s function of encoder pulses’ shaping, filtering, frequency multiplication, checking phase, counting and latching, which is counter model in the Fig. 1.

![Fig. 1. Block diagram of the overall program.](image)

In view of the limitations by NIOS II processor IO port, counter module can be linked to the Avalon
bus of the NIOS II processor. Thus, the design of interface IP core between Avalon bus and counter model becomes very important. The design process of interface IP core is primarily expounded in this paper. It makes use of Verilog language to realize the design of interface IP core between Avalon-bus and counter model, and simplifies the design of encoder counter circuit. Concrete block diagram is shown in the Fig. 1.

2. Design of Encoder Interface Circuit

In order to enhance the anti-interference ability of the system in the industrial field, generally speaking, in order to obtain the accurate pulse, the pulse signals need be isolated, filtered and shaped before the encoders pulse signals enter into counter model. The Optocoupler TLP113 is used for the photoelectric isolation of the signal, the capacitors C1 and C2 are used to realize the signal filtering, the SN7414N inverter is used for shaping the pulse signal. The circuit is shown in the Fig. 2.

The DIR of output direction signal is connected to the UPDOWN pin of the 32-bit counter in order to achieve the counter function by increasing or decreasing the output pulses. The PULSE signal of the output pulse is connected to the CLOCK pin of the 32-bit counter. 74373×2 is a 32-bit latch. The latch is added between the counter and the soft-core processor in order to achieve the count value to be latched. The output signal of D-latch is connected to the coe_cout_in [31..0] of the soft-core processor. Control signals such as sclr, cnt_en and latch_n are enabled by the IO port out_port_the_pio_for_control [5..0] of the soft-core processor [2..0] in Fig. 6. The concrete connection is shown in Fig. 3.

![Fig. 2. Signal procession circuit of encoder pulses.](image)

![Fig. 3. Counting and latching circuit of encoder pulse.](image)

![Fig. 4. Frequency multiplication and checking phase of encoder.](image)
3. Design of Counting Model and Bus Interface

3.1. Avalon Bus Performance and IP Core

Avalon bus is a kind of bus which is used for internal connection between the system processor and peripherals and developed by the Altera Corporation. The Avalon port is divided into master port and slave port. The master port is a collection which initiates the signal transmission of Avalon type. The slave port is an Avalon signal type collection which is in response to the transfer requesting, the basic signals are address, read-data, write-data, read, write, chip-select, etc. For the data width is not 32, Avalon slave address alignment have dynamic address mode and static mode. The mode of the dynamic address alignment is 8-bit for the increase unit, while the mode of the statistic address alignment is 32-bit for the increase unit.

IP interface function is to build a user bridge between counter module and Avalon bus interface. The count pulse value can be obtained through this interface. In order to meet the function of IP interface, this model requires signals that they are clk, reset_n, chip-select, address, write, write-data, read read-data, byteenable, the model output signal is count_in, this signal is connected to 32-bit latch.

3.2. Register File Configuration

Register file is bridge that realizes the exchange signal between the processor and peripherals. The two registers are mainly used in this design, the latch_en register is used to load counter value of coe_count_in into counter register; the counter register is used to store counting pulse value for soft processor reading. In register file, address signal of Avalon bus has two bit, 00 indicates to read enable signal latch_en, 01 indicates the counter value of register counter, 10 and 11 of the address are retained. Under control of chip selection and reading signal, it reads counting register. Under control of chip selection and writing signal, it writes the data enable signal into register.

3.3. Software Implementation and Comprehension

The function description of the Avalon bus IP core is completed by the Verilog language [5]. The following is a part of the code to obtain the counting value.

```verilog
module count_bridge(
    csi_clk,
    csi_reset_n,
    avs_chipselect,
    avs_address,
    avs_write,
    avs_writedata,
    avs_read,
    avs_byteenable,
    avs_readdata,
    coe_count_in);

input csi_clk;
input csi_reset_n;
input avs_chipselect;
input [1:0]avs_address;
input avs_write;
input [31:0]avs_writedata;
input avs_read;
input [3:0]avs_byteenable;
output [31:0]avs_readdata;
input [31:0]coe_count_in;
reg [31:0] avs_readdata;
reg latch_en_selected;
reg counter_selected;
reg [31:0] counter;
reg latch_en;

//*************init**************//
always @(avss_address)
begin
    latch_en_selected<=0;
    counter_selected<=0;
    case(avs_address)
        2'b00:latch_en_selected<=1;
        2'b01:counter_selected<=1;
        default:
            begin
                latch_en_selected<=0;
                counter_selected<=0;
            end
    endcase
end

//*****write register latch_en*******//
always @(posedge csi_clk or negedge csi_reset_n)
begin
    if(csi reset_n==1'b0)
        latch_en=0;
    else
        begin
            if(avs write & avs_chipselect & latch_en_selected)
                begin
                    if(avs_byteenable[0])
                        latch_en=avs_writedata[0];
                end
        end
end

//**********to get counter**************//
assign enable=latch_en;
always @(posedge csi_clk or negedge csi_reset_n)
begin
    if(csi reset_n==1'b0)
        counter<=0;
    else
        begin
            if(enable)
                begin
```

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4. NIOS II Processor Customization and Application of IP Core

NIOS II processor is a kind of embedded processor, it adopts flowing water technique, signal instruction flow is 32 bit general RISC processor, which provides total 32-bit instruction set, data and address bus, 32 general registers, 32 general interrupt source, 32 bit signal instruction of 32×32 Multiply and division, it can order accuracy float calculation instruction and peripheral interface of in chip or out chip. Its performance can be up to 100DMIPS in Cyclone II [5].

In this paper, it customizes the Nios II / f (fast) soft-core processor based on the SOPC technique, at the same time, system can add counter interface component shown in the Fig. 6, wherein coe_count_in_to_the_counter_bridge_0 / 1 is added a counter interface IP core.

Next, we can write the software code in NIOS IDE integrated development environment and read the encoder pulse count value by the IP core interface. The form of structure is used in design, the count0 is the pointer which points to the first address of the IP core, and to get the count value of the IP core latch_en and counter register.

Based on the method of M tachometer and by the NIOS II CPU processing, you can get to the motor speed. Header files are defined as follows [7]:

```c
#define SOPC_H_
#include "system.h"
#include "../inc/types.h"
#define _count0
typedef struct
{
    uint8 latch_en;
    uint32 counter_value;
} count0;
```
count_str;
#ifdef _count0
#define count0 ((count_str *)
  counter_bridge_0_base)
#endif /*count*/
#endif /*SOPC_H*/

5. Conclusions

The actual application shows that the function of the encoder frequency multiplication, checking phase and the latch achieved by this method can meet the actual demand well.

The design of IP core makes counter model and Avalon bus combine very well, which can accurately read the pulse of encoder counting. It reflects the superiority of the embedded NIOS II soft-core processor.

References

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