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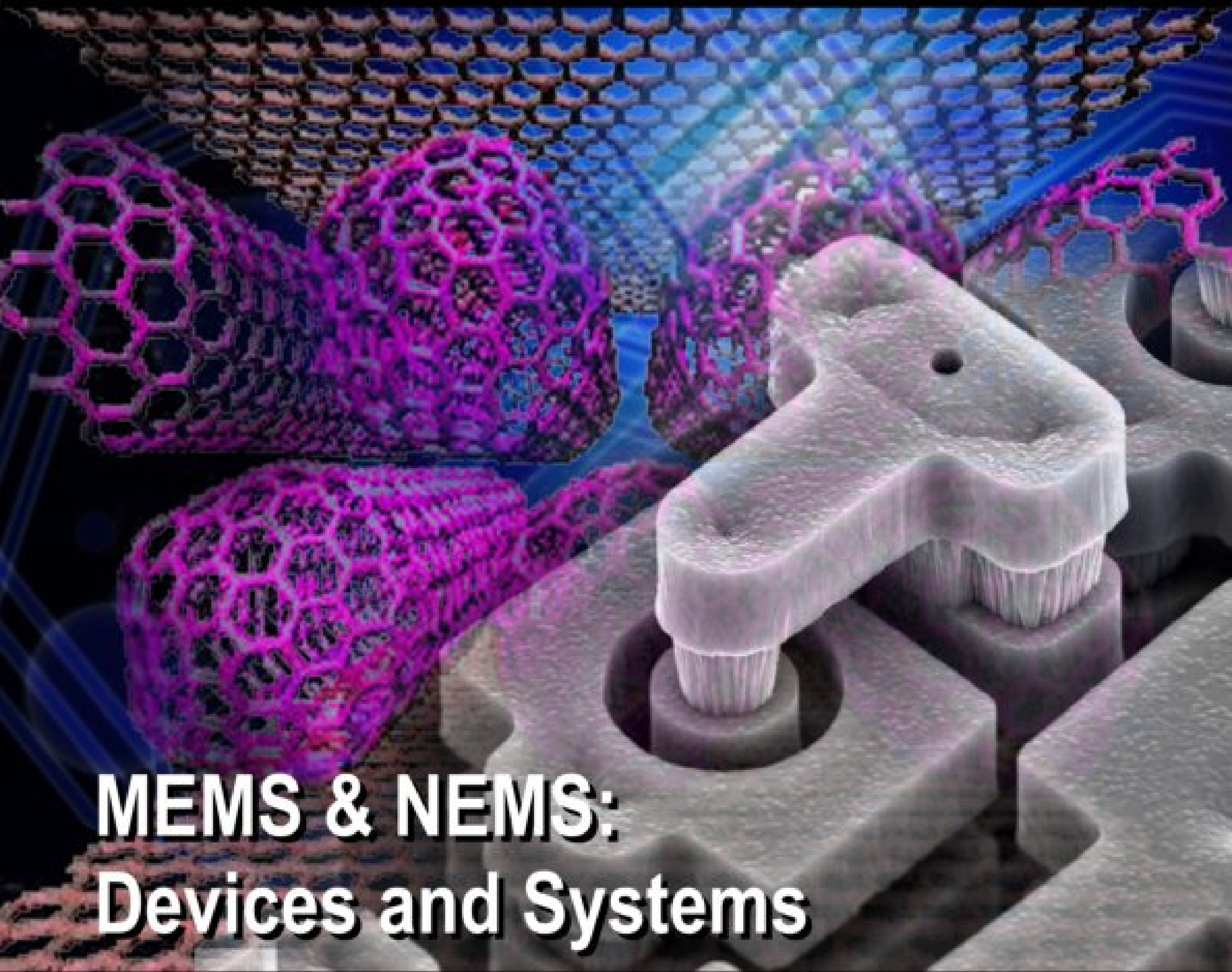

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Foreword

The 10th annual NSTI Nanotech Conference and Trade Show was held this year during 20-24 May at the Santa Clara Convention Center, in Santa Clara, California. The conference has grown this year to host 3000 attendees and 250 exhibitors, while the resulting proceedings boasts over 3000 pages of peer-reviewed micro and nanotechnology research.

A number of authors publishing in the Joint Electronics and Microsystems Symposia track were invited to submit a revised version of their papers to this special issue. Papers were selected from a number of symposia within the track, including: MEMS & NEMS, Sensors & Systems, Micro & Nano Fluidics, and MSM – Modeling Microsystems. These symposia brought together researchers from a number of disciplines to discuss topics ranging from theoretical developments, to design and fabrication, through to industrial applications of MEMS and NEMS sensors, devices and systems.

The joint symposia are motivated by the dream of smarter, smaller, and more complex systems that integrate micro and nano system technologies with intelligence, power and communication ability at the same micro or nano scale. The resulting increase in complexity poses an enormous challenge to engineers when designing, modeling, and fabricating such integrated micro and nano systems. The joint symposia aimed at bringing together researchers from different disciplines to exchange ideas about how to best develop such systems.

As with the joint symposia, this special issue includes papers ranging from those with a higher level focus to those covering low-level physical aspects of MEMS and NEMS devices and their modeling and fabrication. Four of the papers presented in this special issue correspond to invited talks: Sanna et al., examine miniaturization trends in preventative medicine and include some results from the EU project ANGEL; Adams et al., describe the results of the NASA funded GEMSTONE project, which involved creating and field-testing a small system of atmospheric probes; French and Yang explore the opportunities and pitfalls of scaling, whilst Nieva presents a number of new trends for using MEMS sensors in harsh environments.

We are very thankful both to the NSTI directors and Nanotech chairs (Dr. Matthew Laudon and Dr. Bart Romanovicz) and to the *Sensors & Transducers Journal* for offering the opportunity to publish this special issue.

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Microfabrication and Characterization of an Integrated 3-Axis CMOS-MEMS Accelerometer

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Abstract: This paper reports the fabrication and characterization of a monolithically integrated 3-axis CMOS-MEMS accelerometer with a single proof mass. An improved microfabrication process has been developed to solve the structure overheating and particle contamination problems in the plasma etching processes of device fabrication. The whole device is made of bulk silicon except for some short thin films for electrical isolation, allowing large sensing capacitance and flat device structure. A low-noise, low-power amplifier is designed for each axis, which provides 40 dB on-chip amplification and consumes only 1 mW power. Quasi-static and dynamic characterization of the fabricated device has been performed. The measured sensitivities of the lateral- and z-axis accelerometers are 560 mV/g and 320 mV/g, respectively, which can be tuned by simply varying the amplitude of the modulation signal. The over-all noise floors of the lateral- and z-axis are 12 μg/√Hz and 110 μg/√Hz, respectively when tested at 200 Hz. *Copyright © 2007 IFSA.*

Keywords: CMOS-MEMS, Integration, Accelerometer, Microfabrication, Characterization

1. Introduction

Monolithic 3-axis accelerometers have drawn great interests from both industry and academia [1-6]. Capacitive sensing is widely employed in these accelerometers due to its high sensitivity. Most of the commercially available 3-axis accelerometers are based on thin-film microstructures and majority of them use hybrid packages, whose performances are normally limited by the structure thickness, residual stress and parasitics [1, 4-6]. The noise floors of these reported 3-axis accelerometers are normally on the order of hundreds of μg√Hz. By using some uncommon bulk micromachining process, some 3-axis accelerometers with high resolutions have been demonstrated [3, 7]. High cost is a major concern for these devices due to the dedicated process steps.

A single-crystal silicon (SCS) 3-axis accelerometer was developed using CMOS-MEMS technology to achieve high resolution, small size and low cost simultaneously [8]. But it has two drawbacks. First, although most of the sensing structures are made of single-crystal-silicon (SCS), the z-axis sensing still employs Al/SiO_2 thin-film spring beams, which has poor temperature performance. Second, the silicon undercut for electrical isolation of substrate silicon also undercuts the silicon underneath comb fingers, which increases the comb-finger gap and in turn reduces the sensitivity and signal-to-noise ratio. Recently, a new sensor design and fabrication process were proposed by Qu *et al* [9] to overcome the drawbacks in [8]. Better temperature performance was achieved by employing a torsional SCS-based z-axis spring; and the comb-finger undercut problem was much alleviated by performing the electrical isolation formation and the sensing structures etching separately.

However, there are still two significant issues in [9]. First, the isolation trenches are prone to be contaminated in the following reactive ion etch (RIE) and deep-RIE (DRIE) processes, preventing capacitive comb fingers and other microstructures from being released successfully. Second, the overheating during the dry release step severely undercuts the sensing comb fingers and springs, increasing the comb-finger gaps and even causing device failure.

In this paper, a further modified CMOS-MEMS process is developed to resolve these two remaining issues. The detailed characterization of fabricated 3-axis accelerometers is also presented.

2. Structure and Interface Circuit Design

The 3-axis CMOS-MEMS accelerometer reported in this paper features a single proof mass for 3-axis sensing, in which an imbalanced torsional z-axis sensing element is embedded in the lateral proof mass [9]. A two-stage dual-chopper amplifier (DCA) is integrated with the 3-axis accelerometer for each axis as the continuous-time readout circuit [10]. Detailed structure and circuit design are reported in [9] and [10], respectively.

Fig. 1 shows an SEM micrograph of a fabricated 3-axis accelerometer, where the dimensions of the lateral- and z-axis sensing elements are also given. The thickness of all the structures is about 35 μm and the gap for all the comb-fingers is about 2.1 μm. The length of the lateral- and z- axis sensing comb-fingers are 85 μm and 55 μm, respectively, both having the same width of 4.8 μm. The length and width of z-axis torsional mechanical springs are 400 μm and 4 μm, respectively. The crag-leg springs for lateral axes have the same length and width of 320 μm and 5 μm in both directions. The proof mass has a footprint of 1 mm × 1 mm.

3. Fabrication Process

The post-CMOS microfabrication reported in [9] improves the device performance by reducing the undercut on comb fingers and mechanical springs. This is accomplished by performing the electrical isolation etch and the final release of comb fingers and mechanical springs separately. Top metal layer (M4 in TSMC 0.35μm CMOS process that is used in this device) is only used to pattern the electrical isolation structures. After the isolation trenches are formed, as shown in the insets of Fig. 1, M4 is removed by wet or plasma aluminum etch to expose the patterns of other structures of the accelerometer.

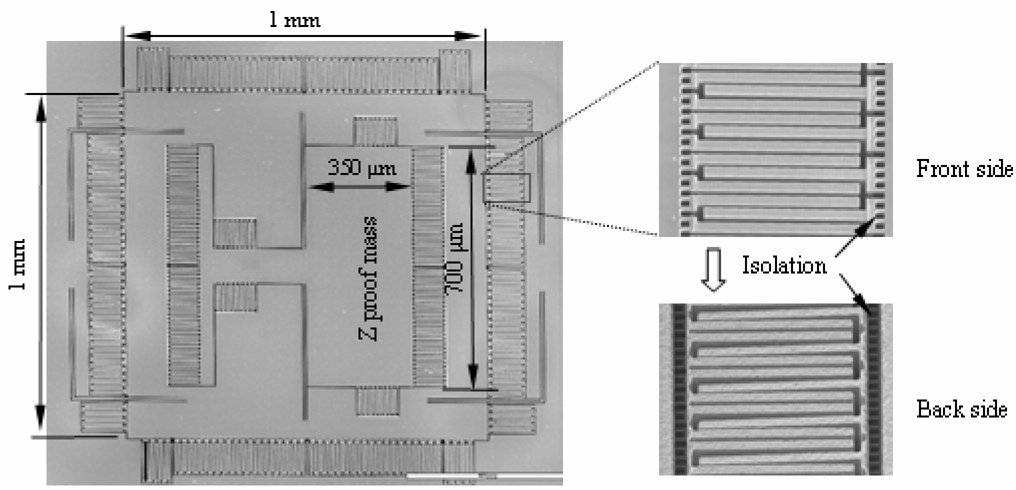

Fig 1. SEM photograph of the sensing element of the fabricated CMOS-MEMS 3-axis accelerometer. The insets show front and backside of the electrical isolation structures.

Some negative effects caused by the two-step etch process were observed. The first one is the contamination of the isolation trench formed after the first silicon DRIE. In the following plasma etching steps, including SiO_2 RIE and silicon DRIE, particles and polymers from assorted sources are prone to accumulate on the sidewalls of the isolation trenches. They act as micro masks in the last release DRIE step, preventing the microstructures from being completely etched through. Fig. 2 shows micro connections on the ends of sensing comb fingers. They result from the micro mask effect of the contaminants deposited on the isolation trench sidewall, and connect the rotor and stator sensing comb fingers together, making the proof mass unmovable.

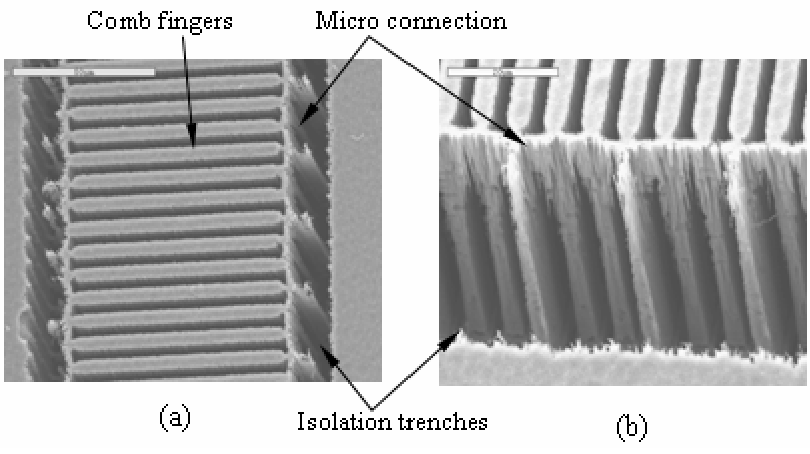

Fig. 2. SEM micrographs showing the micro connections caused by the contamination of the isolation trench in plasma etch steps. (a) top view; (b) side.

The second negative effect is the rapid silicon undercut of comb fingers and mechanical springs due to the overheating of these fine structures during the plasma etch. This undercut happens within a very short over-etch after the accelerometer is released. The reason for the severe undercut is the reduced thermal conductance from the comb fingers to the substrate. The heat generated from chemical reaction and ion bombardment in silicon DRIE can not be dissipated effectively, which consequently raises the temperature of the suspended microstructures. This positive feedback eventually leads to high etching rate and the comb fingers will be undercut very quickly. The same effect was also observed on the z-axis sensing element where the heat can only be transferred through the two long torsional springs.

An improved process, as illustrated in Fig. 3, has been developed to overcome the above two effects.

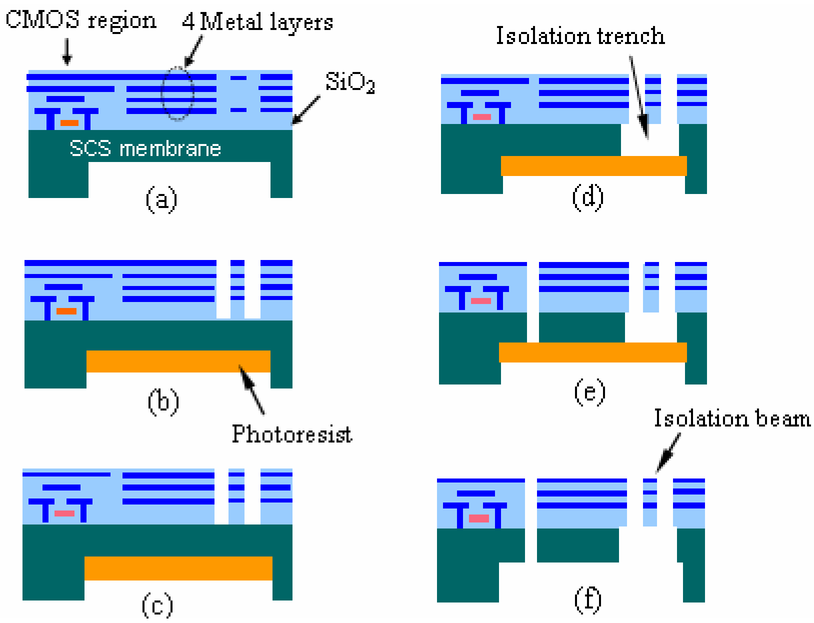

Fig. 3. Post-CMOS microfabrication process flow. (a) Backside etch. (b) Backside PR coating followed by front side anisotropic SiO_2 etch. (c) Top Al etch. (d) Deep Si etch and undercut to form isolation structures. (e) Anisotropic SiO_2 etch and DRIE Si etch for comb fingers and mechanical springs. (f) PR ashing for final release.

There is only one slight modification to the CMOS-MEMS process used in [9]. After the backside etch that produces a silicon membrane and defines the structure thickness (Fig. 3(a)), a thick sacrificial photoresist (PR) layer (~50μm) is applied on the back of the silicon membrane (Fig. 3(b)). After the isolation etching is completed (Fig. 3(c)-3(d)), this PR layer functions as a thermal path during the DRIE silicon etch that forms the entire microstructure (Fig. 3(e)). Finally, the PR is removed by oxygen plasma ashing to release the device (Fig. 3(f)). In Fig. 4, a comparison is made between sensing comb fingers fabricated with and without backside photoresist coating. The undercut of the silicon on comb fingers is greatly reduced and the finger damage is completely avoided by using the modified process (Fig. 4(a)). In contrast, without the PR layer as thermal path, electrical isolation trenches greatly reduce thermal flow from comb fingers to substrate. Consequently comb fingers are overheated and seriously undercut (Fig. 4(b)).

Furthermore, the PR layer helps reducing the backside contamination caused by back scattering. It also helps in tuning the isolation trench profile and relocating the contaminants on the sidewalls. As a consequence, microstructures can be completely released without the micro connections caused by the contaminant particles. This can also be observed in Fig. 4(a).

It should be noted that the thermal effect and the modified process described above are valid to many other MEMS devices with structures similar to this 3-axis accelerometer. A proper device design also helps in reducing the thermal problem described above. By considering the aspect-ratio dependent etching effect (ARDE), we can design the device in such a way that the etch-through sequence for different structures can be well controlled.

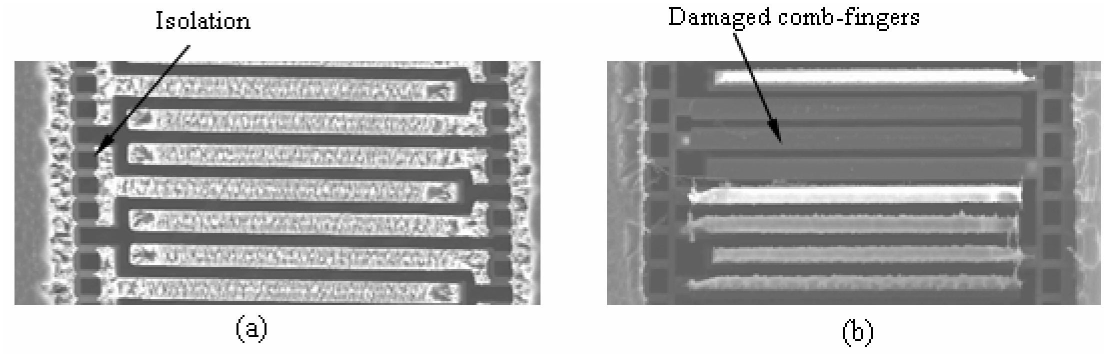

Fig. 4. Comparison of microstructures fabricated with and without backside PR coating. (a) With PR coating, the comb fingers are completely released with slight footing effect; (b) without coating, some comb fingers are completely damaged due to the heating effect.

4. Device Characterization

Fig. 5 is the photograph of a wire bonded die showing the locations of the 3-axis sensor and interface circuits. A dummy on-chip interface circuit was tested with an overall gain of 40 dB and a 16 nV/√Hz electronic noise floor was measured.

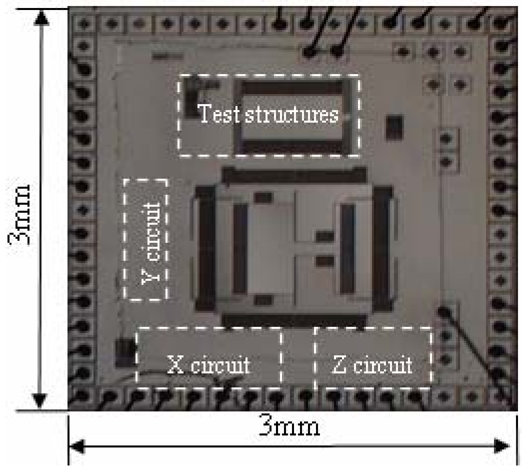

Fig. 5. Photograph of the wire bonded die.

The sensitivities in the lateral axes and z-axis were measured as 560 mV/g and 320 mV/g, respectively, at a 1.5 V modulation signal, by using a quasi-static rotation stage. The resonant frequency of z-axis was measured as 1.5 kHz using a Polytech laser vibrometer. It's about 15% lower than the simulated results, reflecting a remaining slight undercut to the mechanical springs in the plasma etch process. The resonant frequencies of lateral axes are still under test. Due to the asymmetry of the z-axis proof mass, the z-axis sensing element has relatively high cross-axis sensitivities which were measured to be 2.1% from the x-axis and 4.7% from the y-axis, as shown in Fig. 6. The noise measurement was conducted using a LDS shake table and SRS network spectrum analyzer. The spectral response of the z-axis output at a 200 Hz, 0.5-g external acceleration is shown in Fig. 7. The overall noise floor of the z element is 110 μg/√Hz. Although both x- and y-axis have the same number of identical sensing comb-fingers, there is a slight sensitivity difference between these two lateral axes due to the arrangement of the mechanical springs. The spectrum of y-axis output under a 200 Hz, 0.05-g acceleration is shown in Fig. 8. A noise floor of 12 μg/√Hz is demonstrated.

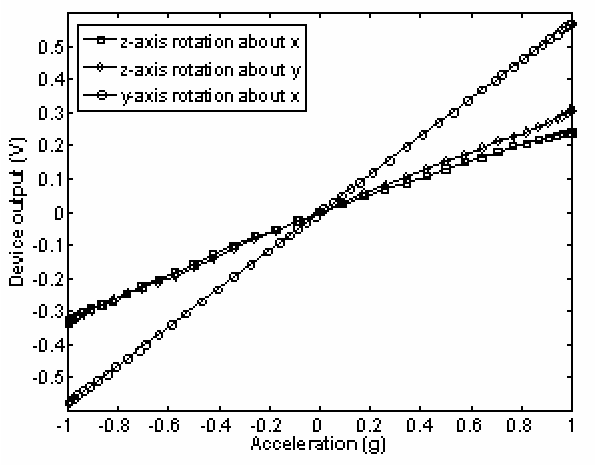

Fig. 6. Static test results of the z- and y- axis using a precision rotary stage.

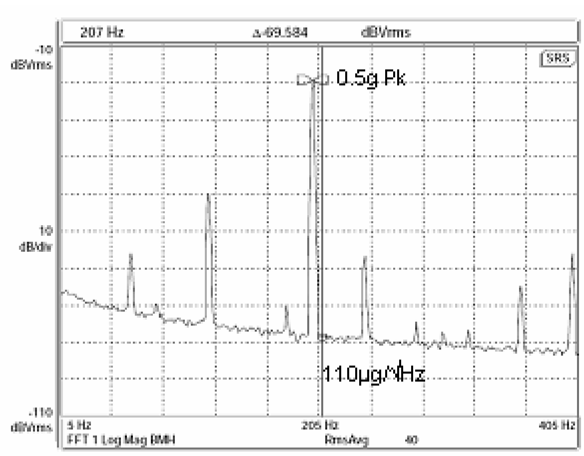

Fig. 7. The spectrum of the z-axis output under 0.5g at 200 Hz (RBW = 1Hz).

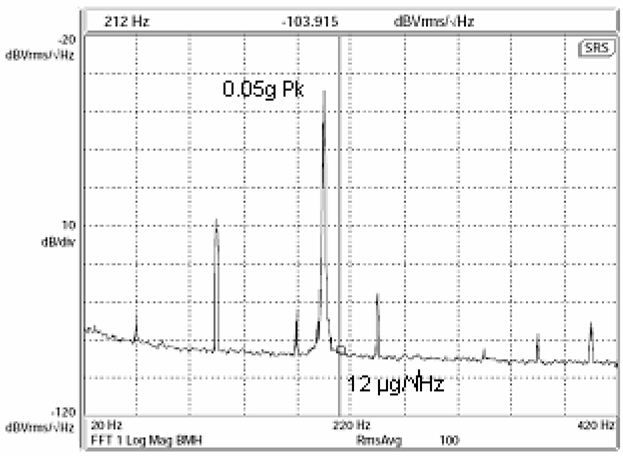

Fig. 8. The spectrum of the y-axis output under 0.05g at 200 Hz (RBW = 1Hz).

An overall temperature coefficient of sensitivity (TCS) of approximately 0.28%/°C was measured, which is mainly caused by the gain drifting of the first open-loop amplification stage of the on-chip amplifier. This is verified by circuit simulation, and a temperature insensitive amplifier is under design. In order to measure the temperature-dependent curling of the sensing comb drives, a band heater was taped on the back of the PLCC-52 sensor package, and the sensor temperature was measured by a spot thermocouple. The vertical curling of the sensing comb fingers was measured using a Wyko optical profilometer. A maximum negative 0.533 μm net curling at the free end of the comb-fingers was measured in a temperature range from room temperature to 96°C. Since the sensor structure thickness is about 50 μm, the corresponding change of the electrode engaged area was approximately 0.23%. Based on these data, a positive 304 ppm/°C temperature coefficient of sensitivity (TCS) of the lateral-axis sensing was derived. Due to the complete SCS structure, temperature-induced structure curling was not observed on the z-axis sensing element.

The measured performance of the device is summarized in Table 1. As a comparison, the performance of ADXL330, a 3-axis accelerometer from ADI, is included.

Table 1. Performance summary of the reported device and comparison with ADXL330 from ADI [1].

Parameters	**Measured values**	
	This work	**ADXL330**
Chip size (mm × mm)	3×3	4×4 (package)
Lateral axes sensitivity (mV/g)	560	300
Z axis sensitivity (mV/g)	320	300
Circuit noise floor (nV/√Hz)	16	-
Power consumption of each axis (mW)	1	0.64~1.15
Lateral axes noise floor (μg/√Hz)	12	170
Z axis noise floor (μg/√Hz)	110	350
Sensitivity temperature drift (%/°C)	0.28	0.01

5. Conclusion

A 3-axis CMOS-MEMS accelerometer with a single proof mass has been demonstrated in this work. The single-crystal silicon incorporated in the device ensures robust sensor structures and high resolution. Low-power consumption (1 mW for each axis) and low-noise floors in all three axes are achieved simultaneously with a compact device size. Compared to the previous processes, this modified post-CMOS microfabrication process has greatly increased the release yield by removing and relocating the contaminants generated in the plasma etching process. It also has increased the process tolerances by providing additional thermal path to the suspended microstructures in plasma etching processes. Though only photoresist was used in this work, there exist many other more suitable materials for the additional heat dissipation. This method can be widely used in micromachining MEMS devices with similar suspended structures. Due to its small size, low power consumption and high resolution, this 3-axis accelerometer has a variety of applications including health monitoring, video games and infrastructure securities.

Acknowledgements

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Guide for Contributors

Aims and Scope

Sensors & Transducers Journal (ISSN 1726- 5479) provides an advanced forum for the science and technology of physical, chemical sensors and biosensors. It publishes state-of-the-art reviews, regular research and application specific papers, short notes, letters to Editor and sensors related books reviews as well as academic, practical and commercial information of interest to its readership. Because it is an open access, peer review international journal, papers rapidly published in *Sensors & Transducers Journal* will receive a very high publicity. The journal is published monthly as twelve issues per annual by International Frequency Association (IFSA). In additional, some special sponsored and conference issues published annually.

Topics Covered

Contributions are invited on all aspects of research, development and application of the science and technology of sensors, transducers and sensor instrumentations. Topics include, but are not restricted to:

- Physical, chemical and biosensors;
- Digital, frequency, period, duty-cycle, time interval, PWM, pulse number output sensors and transducers;
- Theory, principles, effects, design, standardization and modeling;
- Smart sensors and systems;
- Sensor instrumentation;
- Virtual instruments;
- Sensors interfaces, buses and networks;
- Signal processing;
- Frequency (period, duty-cycle)-to-digital converters, ADC;
- Technologies and materials;
- Nanosensors;
- Microsystems;
- Applications.

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