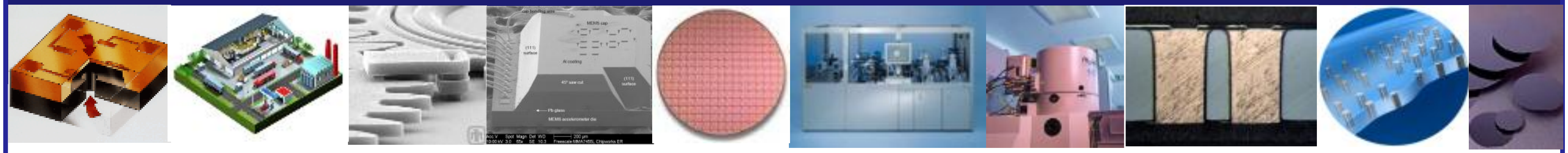
Trends in MEMS Manufacturing & Packaging



New Manufacturing Approaches for MEMS Pave the Way to Smaller, more Cost-Effective Devices!

YOLE DÉVELOPPEMENT

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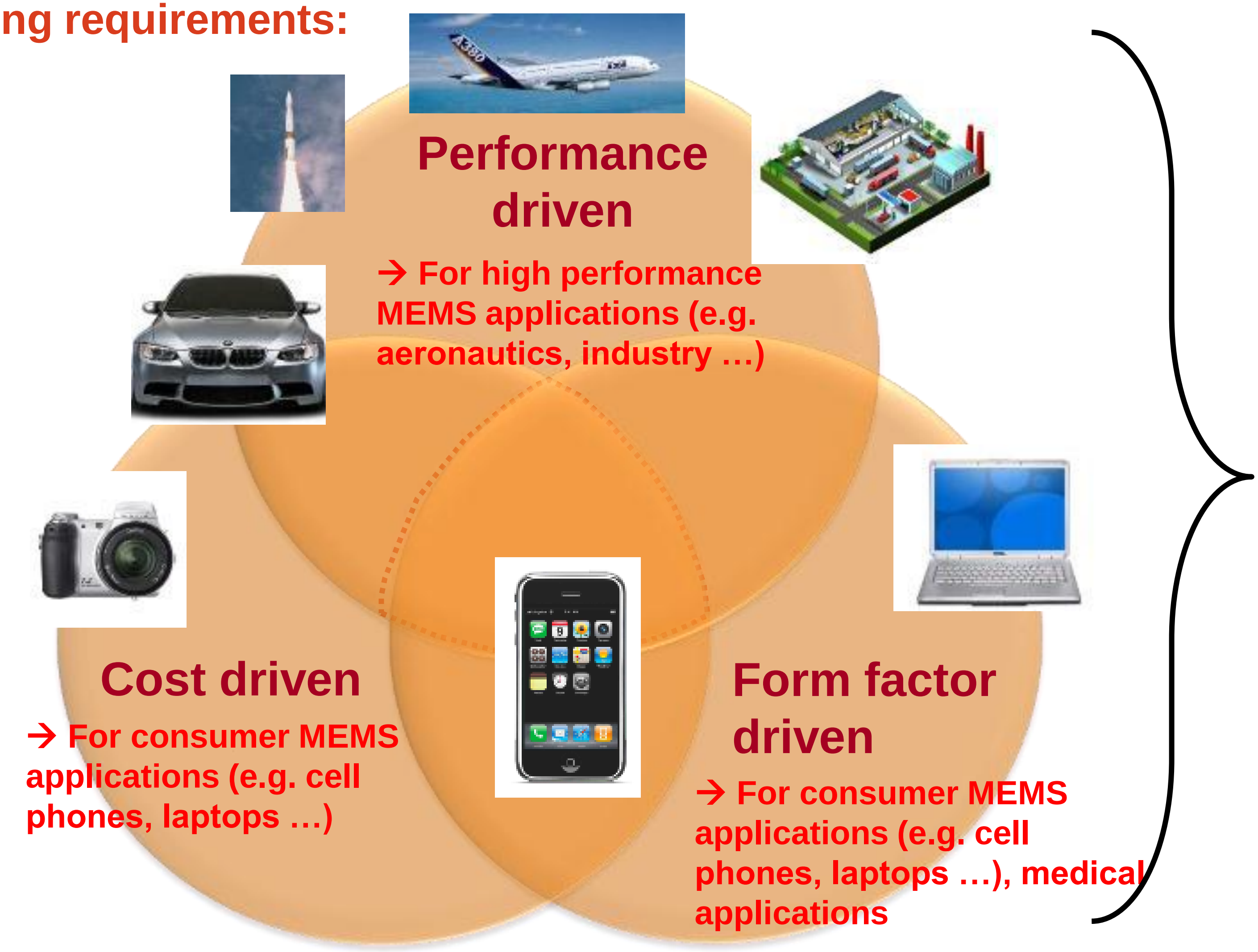
New MEMS manufacturing processes drivers

→The development of <u>new innovative MEMS processes</u> have to answer to the following requirements:



Performance driven

→ For high performance MEMS applications (e.g. aeronautics, industry …)

Cost driven

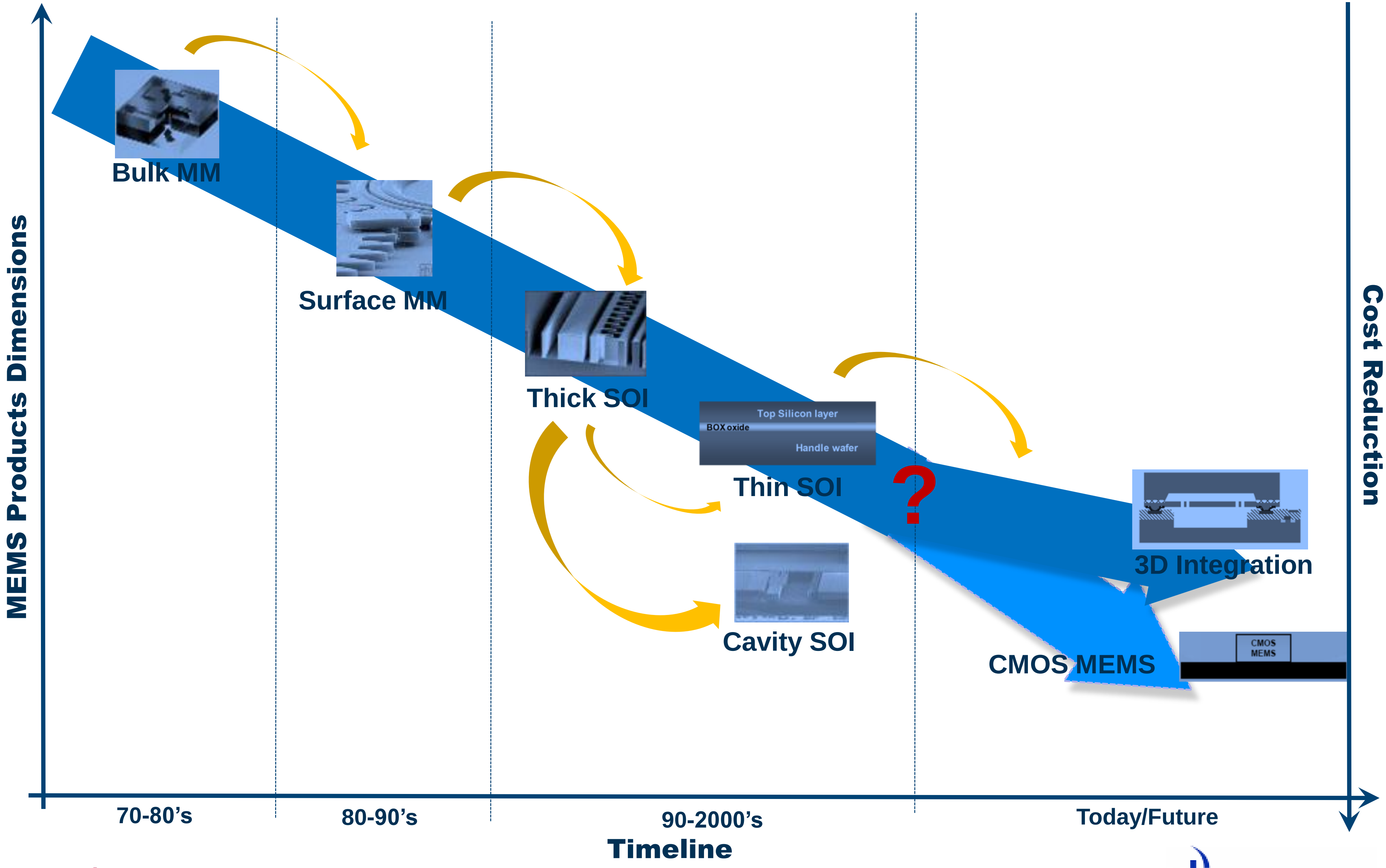
→ For consumer MEMS applications (e.g. cell phones, laptops …)

Form factor driven

→ For consumer MEMS applications (e.g. cell phones, laptops …), medical applications

Both new MEMS manufacturing & MEMS packaging technologies can solve these issues.

The 4 evolutionary steps for MEMS manufacturing

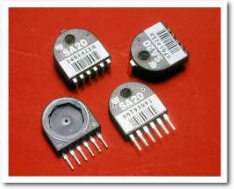


30 years of MEMS Manufacturing History

Over the time, the MEMS manufacturing evolution has aimed at climbing the value chain towards increasing functionalities at the system level.

Major breakthroughs

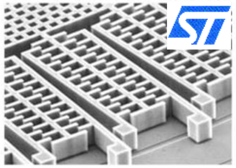
In the 1990s Sensonor had international success with SA20, a sensor for Airbag systems. It was made up of a **piezoresistive beam of Silicon**. Around 35 million sensors were sold all over the world, and the company had an estimated 60-70% of the European market for airbag sensors



Processing level

1990s'

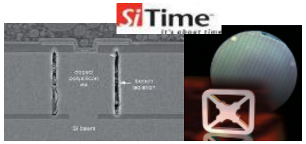
In the 2000s, the **comb drive** architecture is becoming one of the major MEMS architecture for sensing inertial movement.
TI success for DMD is just starting.



MEMS level

2000s'

Packaging is becoming an enabling process step. First MEMS products using 3D TSV are coming to the market.

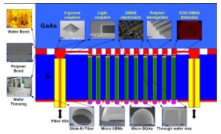


SiTime's MEMS oscillator

Packaging level

2010s'

CMOS MEMS has been phased out. **3D integration** has allowed the integration of different functionalities at the Si level. Room temperature bonding and cost competitive TSV technologies have made such realization possible.

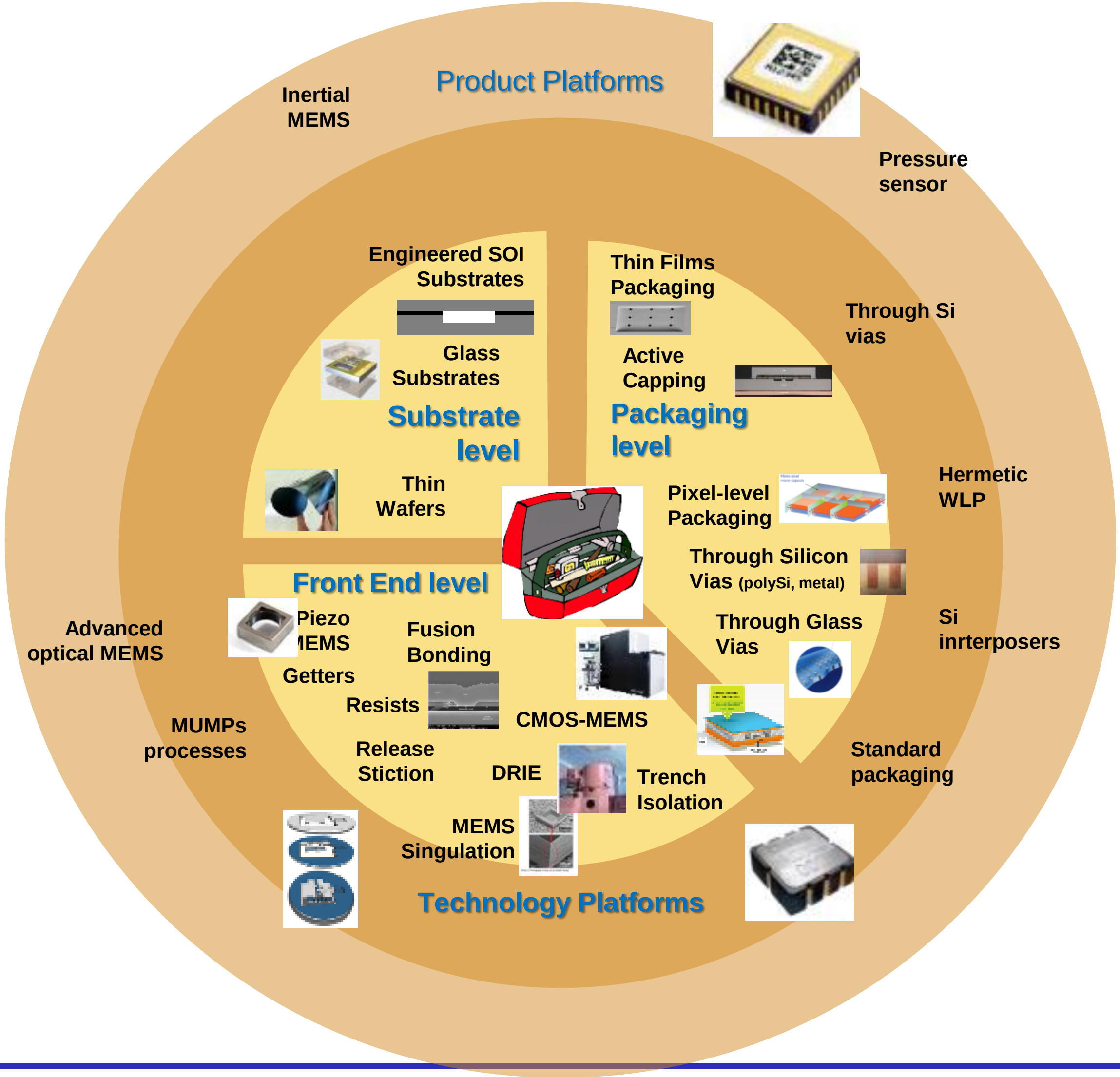


System level

2020s'

Analyzed MEMS Technologies

- **Graph shows the MEMS technologies investigated in this report. These technologies will affect the MEMS manufacturing/packaging at different levels: Substrate level** (SOI, glass, thin wafers), **MEMS die level** (getters, fusion bonding, release stiction, singulation, CMOS MEMS, DRIE, trench isolation) **and packaging level** (TGV, TSV, pixel-level packaging, thin film capping, active capping).
- **Technology & products platform are transverse approaches.**



Product Platforms

Inertial MEMS

Pressure sensor

Hermetic WLP

Si inrterposers

Standard packaging

MUMPs processes

Advanced optical MEMS

Substrate level

Engineered SOI Substrates

Glass Substrates

Thin Wafers

Packaging level

Thin Films Packaging

Active Capping

Through Si vias

Pixel-level Packaging

Through Silicon Vias (polySi, metal)

Through Glass Vias

Front End level

Piezo MEMS

Fusion Bonding

Getters

Resists

CMOS-MEMS

Release Stiction

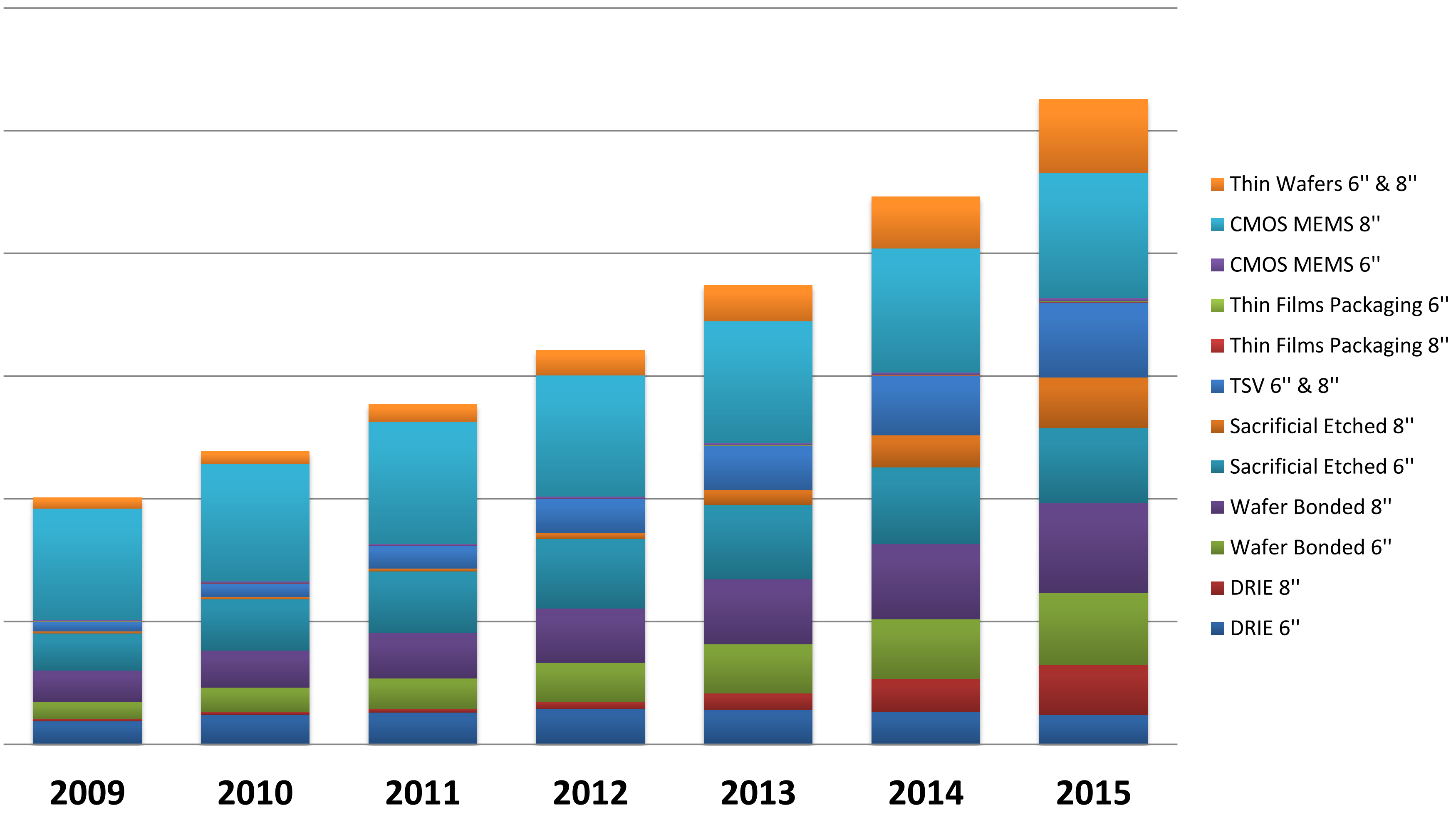
DRIE

Trench Isolation

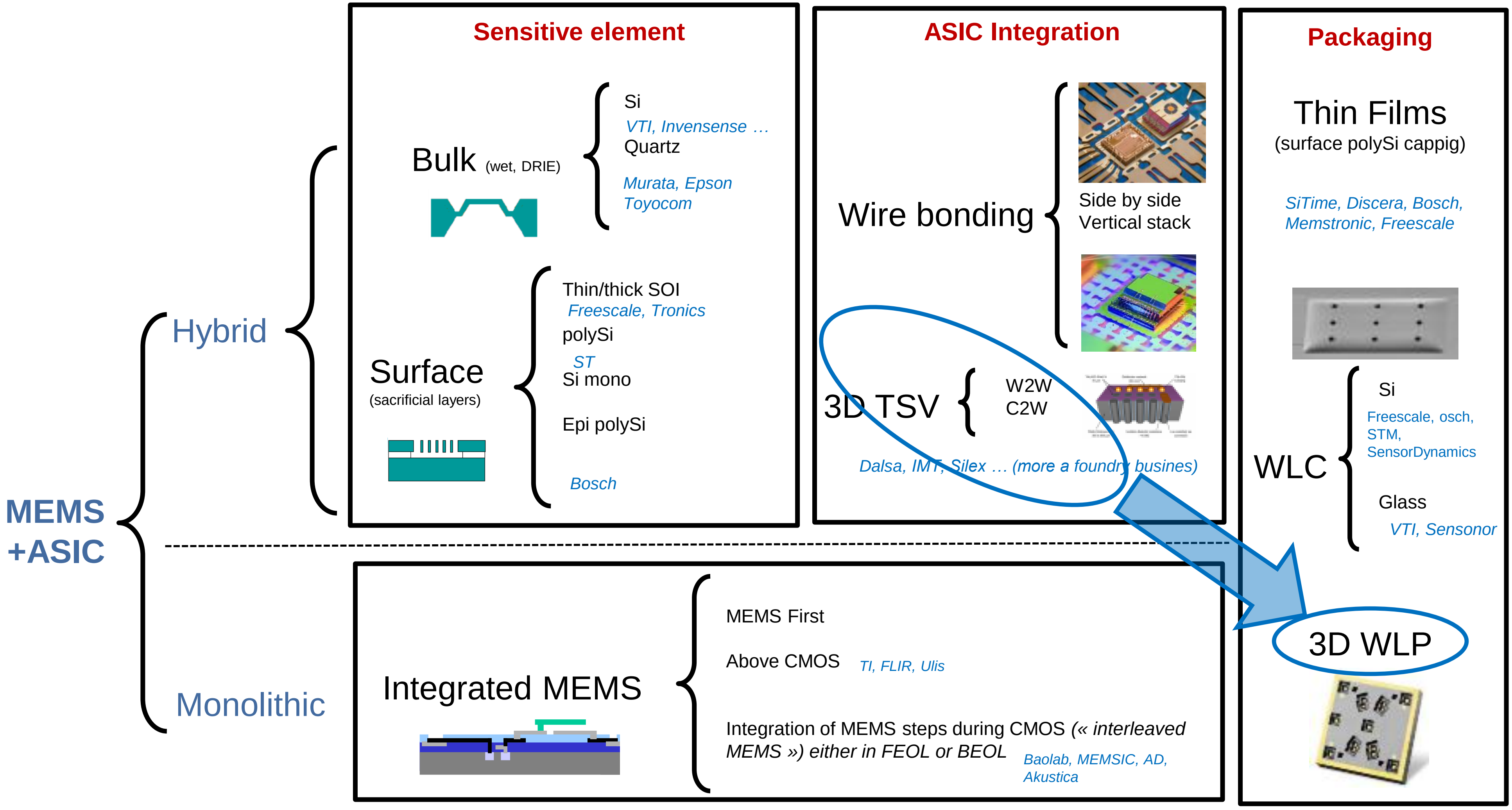
MEMS Singulation

Technology Platforms

MEMS Wafer Forecasts by Type of Process



The different MEMS technological approaches



MEMS +ASIC

Hybrid

Monolithic

Sensitive element

Bulk (wet, DRIE)

Si

VTI, Invensense …

Quartz

Murata, Epson Toyocom

Surface (sacrificial layers)

Thin/thick SOI

Freescale, Tronics

polySi

ST

Si mono

Epi polySi

Bosch

ASIC Integration

Wire bonding

Side by side

Vertical stack

3D TSV

W2W

C2W

Dalsa, IMT, Silex … (more a foundry busines)

Packaging

Thin Films (surface polySi cappig)

SiTime, Discera, Bosch, Memstronic, Freescale

WLC

Si

Freescale, osch, STM, SensorDynamics

Glass

VTI, Sensonor

3D WLP

Integrated MEMS

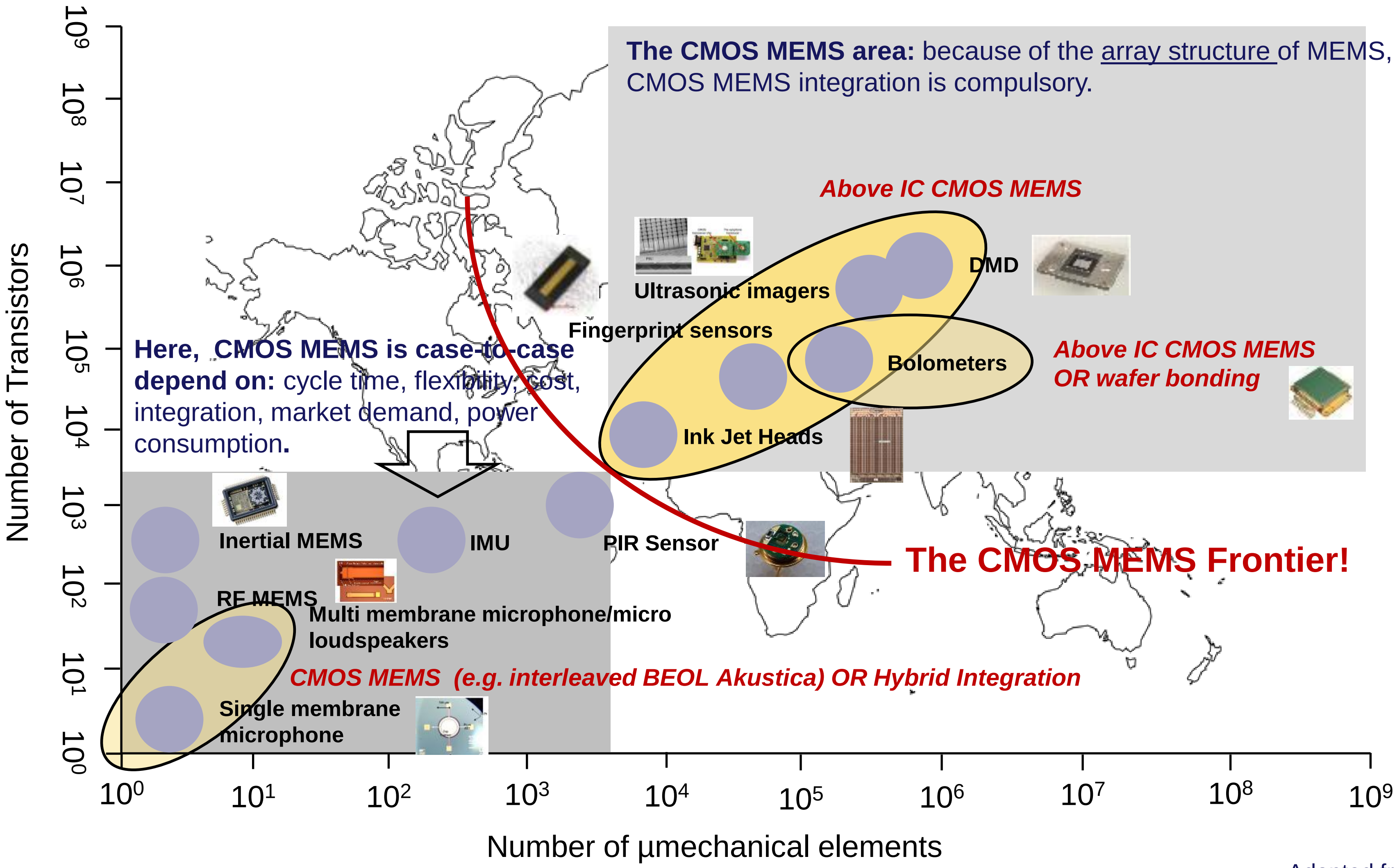
MEMS First

Above CMOS *TI, FLIR, Ulis*

Integration of MEMS steps during CMOS (« *interleaved MEMS* ») *either in FEOL or BEOL* *Baolab, MEMSIC, AD, Akustica*

Executive Summary

Yole MEMS Integration Technology Map, The CMOS MEMS Frontier !



The CMOS MEMS area: because of the array structure of MEMS, CMOS MEMS integration is compulsory.

Here, CMOS MEMS is case-to-case depend on: cycle time, flexibility, cost, integration, market demand, power consumption**.**

Adapted from Akustica

Example of Inertial MEMS Evolution

	2000	2010	2020
MEMS die size (mm²)	10 mm²	~2-3 mm²	1-2 mm²
Packaged die size	2x5x5 mm³	QFN package (3.0 mm x 3.0 mm, height 0.9 mm)	< 1x2x2 mm³
Power consumption	0.1 mW	0.05 mW	< 0.05 mW
MEMS ASP ($)	>$3 (3-axis)	$0.7	<$0.5
Volume (Munits)	35	771	> 2 500
Major manufacturing evolution	• 4” & 6” wafer size • Integrated MEMS from AD • Mostly wire bonding side by side	• 6” and 8” emerging • SOI wafers and epiPoly Si approaches (3µ thick proof mass) • AD shifts to hybrid • Stacked/side by side wire bonded MEMS & ASIC	• Mostly 8” wafer size • Capping is removed • ASIC becomes the active capping • 3D TSV implemented