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Compact Beamformer Design with High Frame Rate for Ultrasound Imaging

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Abstract: In medical field, two-dimension ultrasound images are widely used in clinical diagnosis. Beamformer is critical in determining the complexity and performance of an ultrasound imaging system. Different from traditional means implemented with separated chips, a compact beamformer with 64 effective channels in a single moderate Field Programmable Gate Array has been presented in this paper. The compactness is acquired by employing receive synthetic aperture, harmonic imaging, time sharing and linear interpolation. Besides that, multi-beams method is used to improve the frame rate of the ultrasound imaging system. Online dynamic configuration is employed to expand system's flexibility to two kinds of transducers with multi-scanning modes. The design is verified on a prototype scanner board. Simulation results have shown that on-chip memories can be saved and the frame rate can be improved on the case of 64 effective channels which will meet the requirement of real-time application. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: Ultrasound, Time-of-flight, Beamformer, Synthetic aperture, FPGA.

1. Introduction

Ultrasound diagnosis and treatment have been widely used in medical field. Two-dimension (2D) ultrasound imaging has played an important role in clinical diagnosis. Typically, ultrasound imaging system is composed of the front-and back-end processes [1]. A high-quality beamformer is essential for the front-end ultrasound imaging system. Delay-and-sum (DAS) and minimum variance (MV) are two basic theories for beamformer design. Although MV method can give a high-quality image output, it is hard to be implemented by hardware because of its complex algorithm. DAS method is an actual way for beamformer's circuit implementation. Tracing the evolution of ultrasound imaging history, many techniques have been investigated to simplify structure and improve image quality. Synthetic aperture (SA) [2] can obtain equivalent image quality of 64 effective channels by active 32 channels. Harmonic imaging (HI) [3] is an important means to improve image quality. Combining these two techniques will further promote the beamformer's performance. Different parameters are needed for both synthetic aperture and harmonic imaging. A large numbers of on-chip memories [1] were previously consumed to store the huge parameters; hence it is not flexible for online configuration.

Traditionally, beamformer is implemented by Application Specific Integrated Circuit (ASIC) or by processors, such as Media Processor (MP), Graphics Processing Units (GPU) and Digital Signal Processor (DSP) [4]. The cost is expensive when it is implemented by ASIC and it is usually difficult to support high data rate on real-time ultrasound imaging applications due to their serial properties in MP and DSP. GPUs can provide a higher frame rate, but the complex structure and normally the necessary of personal computer (PC) limit their applications in portable devices. Field Programmable Gate Array (FPGA) have provided an attractive approach in ultrasound imaging systems [1, 2, 5] for the virtues of flexibility, parallel technique and the capacity of high throughput. Yang [2] applied constant parameters in beamformer, but it cannot be configured online and the memory cost is expensive. Schneider [1] introduced a 64-channel B-mode imaging system based on a FPGA and a DSP. The experiments showed that the system can reach 120 scan lines per frame and 30 frames per second. A beamformer with capacity of processing 512×256 pixels' image at 40 frames per second has been presented by Chen [5]. He used two FPGAs to implement the beamformer. Normally, it is a tradeoff between cost and performance, but there is still a large margin to be explored.

In this paper, a single-FPGA-based compact beamformer with dynamic configuration is presented. For the convenience of hardware implementation, a simplified time-of-flight calculation method, which uses a quantized arc length formula, is proposed. To improve the frame rate and fulfill the requirement of real-time ultrasound imaging, multi-beams (four beams per emission) method is adopted. Dynamic configuration provides a flexible approach for different applications. Thus synthetic aperture and harmonic imaging can be integrated to a single FPGA with efficient memory utilization. Time sharing and interpolation are also employed to reduce the resource cost of the beamformer.

Next sections are organized as follows: The simplified time-of-flight calculation is deduced in section 2. Architecture and methodology of our design are presented in section 3. Implementation and results are shown in section 4, and the conclusion is drawn in section 5.

2. Method of Time-of-flight Calculation

To get a focus point, dynamic time-of-flight (TOF) calculation has been presented [7, 8]. But from the aspect of circuit implementation, the work is still too complex. To overcome this problem, a simplified approach of calculating the time-of-flight of a transmit/receive ultrasound wave is pointed out. Fig. 1 is the mathematic model of the transmit/receive delay distance calculating diagram for a convex transducer array. There are N elements in the probe array, the probe radius is R, and the probe pitch is P. i is the specific element of the channels.

From the basic sonic wave focus theory, sonic waves are bilateral symmetry. On transmitting, the central line channel (y axis) has the longest delay time, which is located in the middle of the transducer array. Relative delay distance (D_t) of element i can be given by (1). D_t' is the absolute transmitting delay distance and F_r is the focus depth of the scan lines, where x_t and y_t are expressed by (2) with angle (θ') shown in (3). θ can be described by the arc length formula ($\theta = P / R$).

$$D_t(i) = D_t' - F_r = \sqrt{x_t(i)^2 + (y_t(i) - F_r)^2} - F_r, \quad (1)$$

$$\begin{cases} x_t(i) = R * \sin(\theta') \\ y_t(i) = R * \cos(\theta') - R \end{cases}, \quad (2)$$

$$\theta' = \theta \times (i - 15.5), \quad (3)$$

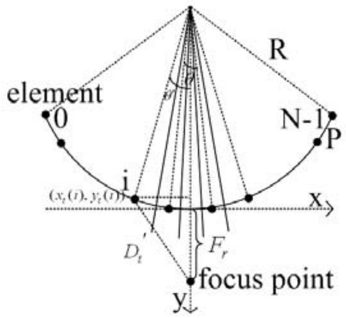

Fig. 1. Mathematical model of time-of-flight calculation.

Four beams (solid lines in Fig. 1) are received after a transmit event. Absolute receiving delay distance (D_r) is given by (4). n is one of the four beams, m is one of the receiving elements and k is the quantized scan depth. x_r and y_r can be expressed by (5) for a convex transducer array. The TOF of transmit (T_t) and receive (T_r) are given by (6). The TOFs are normalized by clock period (T_{clk}) and acoustic wave speed (c=1540 *m/s*). If a linear transducer array is used, TOF can be generated by a similar method based on the Cartesian coordinate system.

$$D_r(k,n,m) = \sqrt{x_r(n,m)^2 + (y_r(n,m) - F_r(k))^2} + F_r(k), \quad (4)$$

$$\begin{cases} x_r(n,m) = R * \sin((P/R) * (m - 30.75 - n * 0.5)) \\ y_r(n,m) = R * \cos((P/R) * (m - 30.75 - n * 0.5)) - R \end{cases}, \quad (5)$$

$$\begin{cases} T_t = D_t(i) / c / T_{clk} \\ T_r = D_r(k,n,m) / c / T_{clk} \end{cases}, \quad (6)$$

In our method, Polar coordinate system and Cartesian coordinate system are applied in the convex transducer array and linear transducer array respectively. In practical terms, the coordinator x and y are pre-calculated by Matlab and then stored in the two-port random-access memory (RAM) of FPGA. As a result, TOF generation is convenient for hardware implementation.

3. Architecture and Methodology

Schematic diagram of the whole medical ultrasound system is shown in Fig. 2. Main modules (system control, transmit, receive, interface bus, signal process and disp control) are implemented in one FPGA. Off-chip memories (RF SRAM, DRAM and DSC SRAM) are used for data storage. An ARM processor is used as the man-machine interface controller to enhance capability of the system. Communication with keyboard, terminal (universal serial bus) and personal computer is handled by ARM.

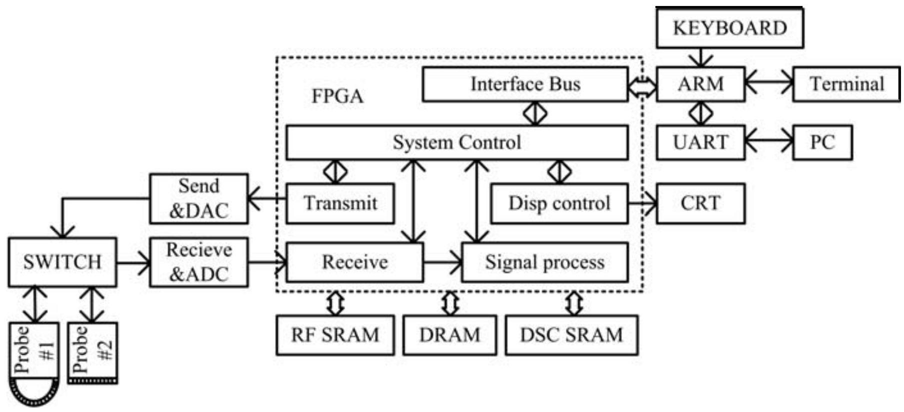

Fig. 2. Functional block of ultrasound imaging system.

DAS method is applied in the receiving process. After a transmit event, the switch blocks the transmitting, RF signal coming from convex or linear transducers will be sampled by analog-to-digital converters (ADC). There are four ADCs with eight channels in each ADC in our system. The RF data is sampled at 40 MSa/s before being sent to FPGA via a low-voltage differential signal (LVDS). A digital symmetric 17-tap band-pass finite impulse response (FIR) filter array is used to filter low frequency noises generated by receive amplifiers with variable gain. To reduce the burden of multipliers, the filter is implemented only by addition and shift operations. A beam is focused based on DAS for phased sub arrays. The geometrical TOF (represented as reading addresses) for each channel is generated on the fly to get the proper data stored in on-chip RAM. To improve frame rate for real-time ultrasound imaging, multiple receive beams with a single transmit event [6] is applied in this paper. The 32-channel RF data is then summed across the aperture domain prior to the formation of a B-mode image. Finally, the formed beam is scan-converted for video display by the signal processing module and the display control module.

Since expanding the aperture size will improve the lateral resolution of an image, 32 active channels are compounded to 64 effective channels. HI can improve the tissue-harmonic and contrast-agent imaging processes by reducing the echoes centered on the fundamental frequency while keeping the echoes centered on the second harmonic [3] in a medical field. The reception structure diagram is shown in Fig. 3. The 32-channal data is read out to perform interpolation at the other port of the RAM buffer. Reading addresses are generated from the Receive Focus Generate module. After four-phase interpolation completed by Phase Generate module and Multi-plus unit module, receiving data of each channel is apodized according to lateral resolution [4] and is summed to construct a beam. The compound module is used to compound the beams of two emissions. An additional RF SRAM is used to store a frame image. Pipeline technique is employed on receiving so that beam data is refreshed by every clock.

Traditionally, 32 individual address generator units are needed to form a beam if there are 32 channels. An efficient and compact approach is proposed to reduce resource cost in Fig. 4. There are two adders (adder and subtracter), several registers (represented as D) and four switches (A, B, C, S) in each channel. To accomplish four-phase interpolation, the system is capable to handle 160MSa/s (40MSa/s×4). Each channel is refreshed by every 128 clocks (4 clocks for the four-phased interpolation of a point, 4 clocks×32 channels). To explain the operating principle, channel 0 is taken as a demonstration. S is switched to left for the first 4 clocks before it is switched to right for the rest 124 clocks. B and C are acting the same with S (down for the first 4 clocks, up for the rest 124 clocks).

Switching of A is similar to C except that they are not switching at the same time (4 clocks ahead of C). Difference of B and C is shifted to right by 5 (divide by 32) before it is accumulated. As a result, four-phase interpolation is accomplished in 4 clocks and the rest 124 clocks are used for linear interpolation. The timing relationship of generated addresses is illustrated in Fig. 5. Generated addresses (*RD0*, ..., *RD31*) are coming from corresponding channels (*channel 0* to *channel 31* in Fig. 4). The 31 data (labeled by the first two characters *CH*) between *RD0* and *RD32* is the result of interpolated data.

Since time sharing and linear interpolation techniques are employed in this paper, only one square root is needed.

Compared with direct calculation of TOF, our structure is compact and resource is saved (approximately 124 folds with 31 times of resources are saved).

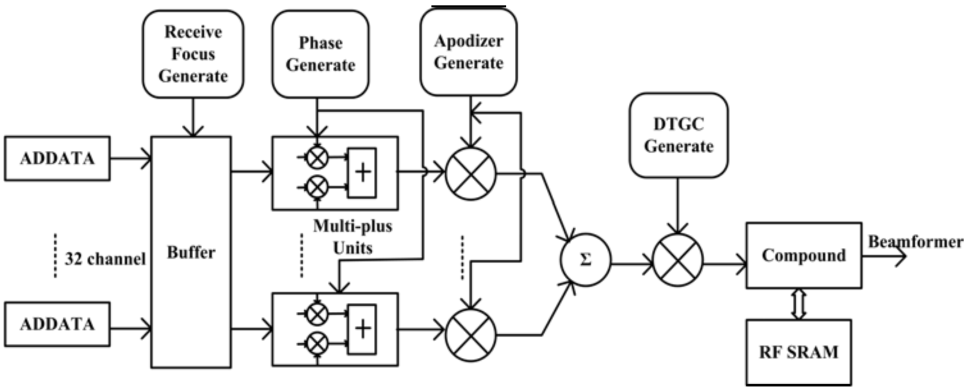

Fig. 3. Structure of reception.

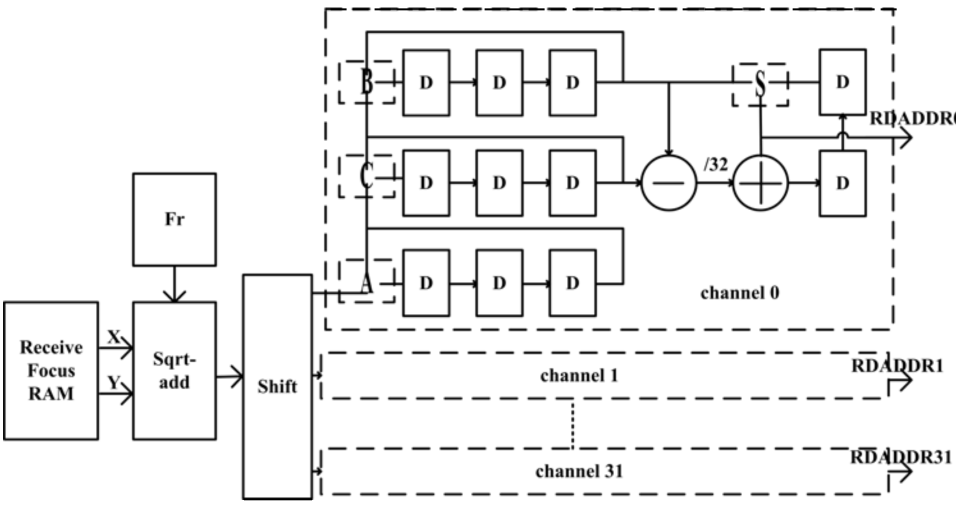

Fig. 4. Structure of reading addresses generator.

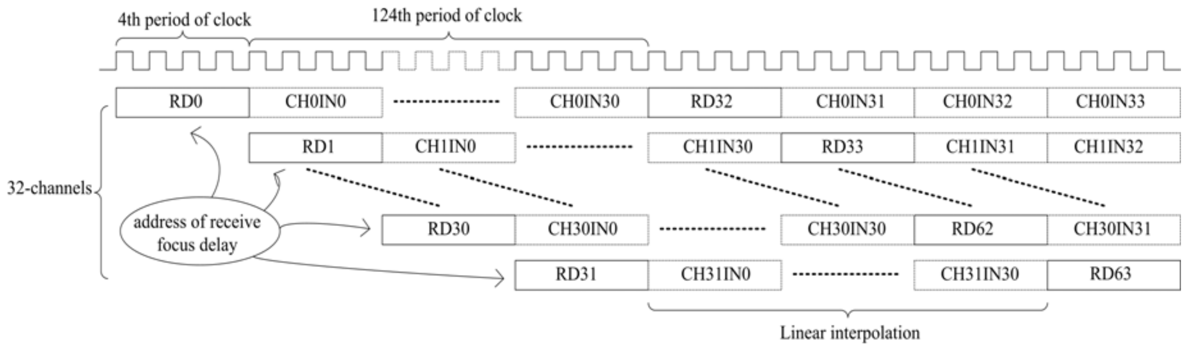

Fig. 5. Timing relationship of the generated addresses.

4. Implementation and Results

4.1. Implementation

The front-end design has been tested on a prototype board with a single Cyclone IV FPGA and an ARM coprocessor in Fig. 6. In our system, 128 elements of transducer with center frequency of 3.5 MHz is used as the detect probe. The transmit focus can be set to one of several possible points for any given emission. Receive focusing is dynamic. On reception, a raster-type scanning method is employed. The point by point scanning is firstly along the horizontal line and then along the vertical line until the whole frame image is scanned. The maximum imaging depth is more than 310 mm to form an image of 512×256 pixels. The whole system (transmit, receive, system control and interface bus modules) has been verified by Modelsim SE 6.2b and synthesized by Quartus II 10.1. The synthesized result is shown in Table 1. Specially, the resource cost of transmitting and receiving blocks are also listed, because they are the key modules of beamformer design.

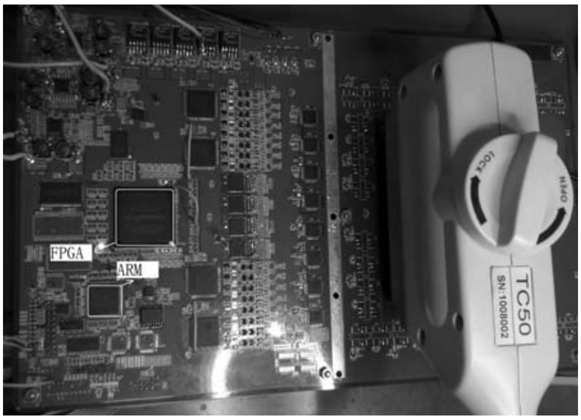

Fig. 6. Prototype board of medical ultrasound scanner.

Table 1. Resource usage based on device EP4CE75F29C6.

Module	Logic elements	Memory Bits	Multiplier 9-bits	Frequency (MHz)
Beam-former	44849	620608	198	177.9
Transmit	895	136192	0	195.7
Receive	40575	185391	198	192.2

4.2. Result and Analysis

To evaluate different scanning modes in influence of frame rate, the relationship of maximum frame rate and imaging depth is compared. Frame rate of a medical imaging system can be calculated by (7), where $N \times T$ is the number of transmitting times of a frame image and T_{rate} is the scanning period of a transmit event. T_r is the receiving period represented by $2 \times h / c$ with h standing for imaging depth. T_d is the constant delay time between transmitting and receiving.

$$F_{rate} = N_T \times T_{rate} = N_T \times (T_r + T_d) \qquad (7)$$

Relationship between maximum frame rate and imaging depth is shown in Fig. 7. The maximum frame rate is decreased with the increase of the imaging depth for the Normal, SA and HI scan modes. When the imaging depth is 310 mm, under the normal scanning mode, the HI scanning mode and the SA scanning mode, the maximum frame rate per second is 37.77, 18.89 and 18.45 respectively. The relationship between maximum frame rate and scan lines per frame for these modes is illustrated in Fig. 8 (the imaging depth is 150 mm). In all cases, frame rate is inverse proportion to scan lines per frame. It can be seen from Fig. 7 and Fig. 8 that a high frame rate is achieved (38.64 *f/s* with 150 *mm* imaging depth and 120 scan lines) which can meets the requirement of real-time application.

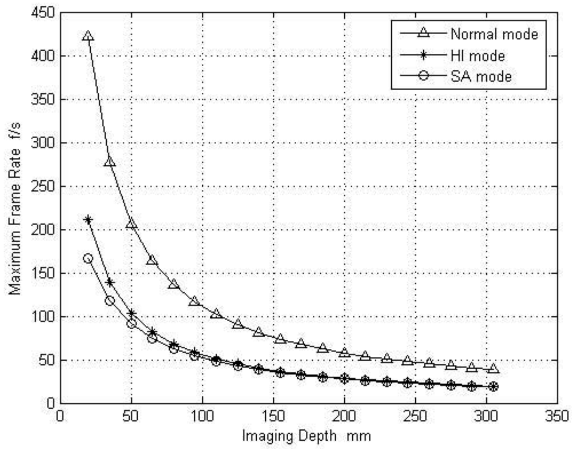

Fig. 7. Maximum frame rate under 120 scanlines.

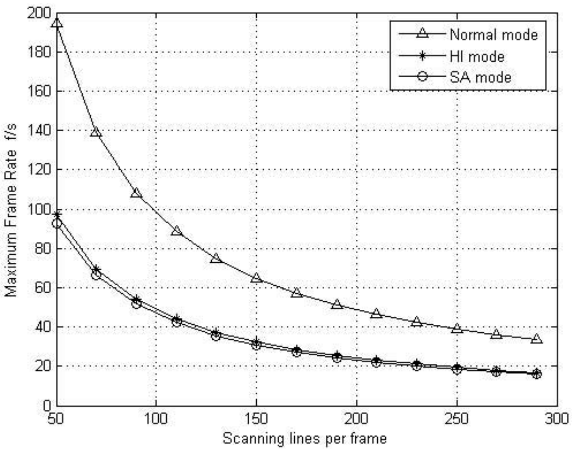

Fig. 8. Maximum frame rate under the imaging depth of 150 mm.

Four beams with a single transmit event is used to decrease the times of transmitting so as to improve frame rate according to (7). A performance comparison is summarized in Table 2. With 64 effective channels, the frame rate is improved about 28.8 % compared to [1]. As a result, our beamformer system achieved an enlarged function with improved frame rate in a single moderate FPGA.

Table 2. Performance comparison (imaging depth: 150 mm, scanning lines: 120).

	Channels	Frame rate per second	Scanning mode	Device
In [1]	64	30	Normal	A EP2C35 FPGA and a TMS320C6416 1 GHz DSP
Proposed	32	80.96	Normal	A EP4C75 FPGA
	64	38.64	SA	
	32	40.48	HI	

5. Conclusions

A flexible, universal and compact beam-former has been implemented in a single moderate FPGA. A compact structure is designed by combining synthetic aperture and harmonic imaging. To improve frame rate, a simplified TOF calculation method is investigated to achieve four receive beams with a single transmit firing. The online configuration provides much more flexibility and wider range of applications for the system. Time sharing and linear interpolation are applied to save resource cost. Wide range of imaging depth and multiple scanning modes are achieved in B-mode real-time imaging with a high frame rate. The beam-former not only shows a bright potential in color Doppler imaging system with less modification, and also provides necessary frame rate for three dimensions real-time ultrasound imaging.

Acknowledgements

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