

FPGA-based Array CCD Sensor Drive System Design and Implementation

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Abstract: CCD Sensor is the crucial equipment for environment perception which is widely used in various fields such as surveillance, vision navigation and machine vision. The commercial CCD device has been encapsulated the sensor driver inside which is not opened for secondary development. Even this mode facilitates the usage but it really can't content the customizable need. For solving this challenging but imperative issue, we designed a novel CCD sensor driver system which implements the efficient and effective image acquisition task in customizing approach. The working principle and driving timing sequence about ICX625AQA the interline CCD image sensor used in our system are discussed in detail. For handling with this data intensive task, a high performance Field Programmable Gate Array (FPGA) controller is used for data allocation and translation, the peripheral circuits including AD9974 and CXD3400 drive interface which process the horizontal signal and vertical signal, respectively. The system execute code is compiled and configured in the Quartues II IDE and is simulated used the SignalTap. Some significant results also are proposed at the end of this paper. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: Interline transfer, Field programmable gate array (FPGA), Dual-channel output, Charge coupled device (CCD), ICX625AQA.

1. Introduction

Charge-coupled device (CCD) was invented initially in 1970s, it has many excellent features, such as high sensitivity, large dynamic range, low noise, low power consumption and fast sampling speed [1]. The CCD sensor is such a device for the movement of electrical charge, usually from within the device to an area where the charge can be manipulated, for example conversion into a digital value, and is widely used in professional, medical, and scientific applications where high-quality image data is required particularly in high-precision measurement,

space remote sensing, robot vision and other associate fields [2-3]. CCD image sensor converts optical signal into charge signal by an optical - sensitive surface, and then according with certain rules to output image based on corresponding pulse timing driver. CCD image sensor has better performances in optical filling rate, the uniformity of the response of pixels and quantum efficiency than CMOS and become a science of choice detector for high frame rate imaging acquisition system increasingly [4], the array CCD image sensors can be implemented in several different architectures. The most common are full-frame, frame-transfer, and

interline [5]. Each of these architectures has its different approach to the problem of shuttering. The interline transfer because of its advantages and fast readout speed CCD camera has been used in high frequency [6]. The mainly driving circuit of interline transfer CCD includes biased voltage circuit, the horizontal timing-driven circuit and vertical timing-driven circuit. In such circuits mentioned above, the first encountered issue is how to generate the CCD drive timing. In generally, there are four different methods to deal with this challenging matter: direct digital circuits, microcontroller-driven, EPROM-driven and programmable logic devices method [7-9]. Direct digital circuit can get higher-speed driving frequency but accompany with design complication and debug difficulty, Microcontroller drive owns the advantage of easy programming and flexible adjustment but the frequency of driving circuit is too lower to meet the high-speed requirements, EPROM-driven is simple to structure and debug but the usually occupies larger structural space, programmable logic devices such as field programmable gate array (FPGA) includes many advantages such as the ability to re-program in the field to fix bugs, can be repeated or improved after completing the design and easy to update and maintenance. Thus characteristics make the FPGA gradually dominates the application for CCD sensor driver. The driver circuits implemented based FPGA is higher integration, reliability and performance, lower power consumption, cheaper price cost and shorter development cycle period [10].

In this paper, we focus on how to design a novel CCD sensor driver system which implements the efficient and effective image acquisition task in customizing approach based on FPGA. Firstly, we discuss the parameters and work principles about ICX625AQA, one of the typical CCD sensors. Secondly, we describe the design of hardware driving circuit including horizontal drive, vertical drive and voltage generation circuit as well as illustrate the circuit layout and manufacture board. Thirdly, we introduce the workflow of the software running on the FPGA which including the horizontal and vertical timing modules. The simulation of the timing also is conducted to verify the validity of the software. Fourthly, we integrate the hardware part and software part together to achieve the high fidelity image. Finally, we conclude our work and prospect the further tasks.

2. ICX625AQA Structure and Characteristics

ICX625AQA is an interline transfer area array color image sensor produced by SONY Corporation, The total gross number of pixels up to $2536 (H) \times 2068 (V)$, approximately 5.24 Mega, The valid number of pixels are $2456 (H) \times 2058 (V)$, approximately 5.05 Mega effective pixels. Each pixel unit cell size is $3.45 \mu\text{m} (H) \times 3.45 \mu\text{m} (V)$, the

effective pixel imaging area is 86.39 square millimeter. ICX625AQA fans out the signal within dual output channels. There are three operating modes can be handled when proper operating the sensor which are full pixel scan output model, in this mode, all pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing; in the 4/16 line output model, the signals are read out four lines (1st, 5th, 8th and 12th line) for each 16 lines and two pixels of the same color are added in the horizontal register, all effective area signals are output at higher frame rate than the all pixel scan mode; the last operation mode is the center readout scan output mode, this mode realizes high frame rates by sweeping the top and bottom of the picture with high-speed transfer and cutting out the center of the picture. The image output rate of the ICX625AQA can achieve to 15 frames/sec in the all-pixel scan mode also output using various addition and elimination method [11]. An electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. High sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology. This CCD image sensor is driven by one four-phase vertical transfer pulse (V_1 , V_2 , V_3 and V_4), one two-phase horizontal transfer pulse (H_1 and H_2), another electronic shutter pulse (SUB) and one reset pulse (RG) simultaneously. Those various pulses mentioned above combined with each other constitute CCD image sensor's drive timing pulse.

3. Driver Circuit Analysis and Design

Stable power circuit is essential for ICX625AQA work properly. There are several extinguished power circuits to provide energy for the CCD sensor, such as the positive 15 V bias voltage, the negative 8 V bias voltage. The horizontal transfer pulse and the vertical transfer pulses are shown in Fig. 1. Bias voltage circuits not only provides CCD sensor power but also content the power consume in FPGA main chip system, the horizontal drive circuit and vertical drive circuit provides horizontal driving clock signal and vertical driving clock signal for CCD sensor respectively. Each circuit such as Horizontal drive circuit, AD conversion circuit and the vertical driving circuits works in different clock frequencies but shares the common clock synchronization signal. These circuits work harmoniously to ensure the CCD image sensor can output the small analog signals which stand for the environment light intensity. The small analog signals are prone to be influenced by the electronic noise, one AD conversion circuit which holds high magnification times and SNR is used for correct image acquisition [12]. FPGA processors is used to be the main chip which is responsible for outputting timing and controlling signal for each chip desired, at the same time, it also

receives the valid data coming from AD conversion output for further processing. The relationship between those circuits mentioned above is shown in Fig. 1.

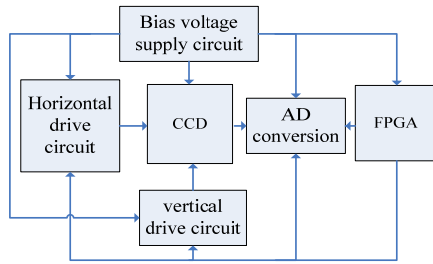


Fig. 1. System hardware block diagram.

3.1. The Horizontal Drive Circuit

As discussed above, ICX625AQA adopts the dual-channel drive model to fan out the image signals which ask the AD conversion circuit must match this issue. In our system, the high performance AD convert chip named ADA4800 is chosen as a buffer amplifier. In this section, we mainly focus on generating the CCD drive signal, in our work, we select ADI's AD9974 to provide horizontal pulses drive signal, the Circuit diagram of AD9974 is shown in Fig. 2. AD9974 integrates double-pass high-speed signal processing circuit for high speed digital video camera applications. Each channel is

specified at pixel rates of up to 65 MHz, and in internal integrated analog front-end processing circuit, including the black level clamping, CDS, programmable amplifier (VGA) and a 14-bit analog-to-digital converter circuit. The Precision Timing core in it allows adjustment of high speed clocks with approximately 240 picoseconds resolution at 65 MHz operation. The timing driver provides the high speed CCD clock drivers for the RG1, RG2, H1A to H4A, and H1B to H4B outputs. AD9974 generates flexible high speed timing signals using the Precision Timing core. This core, composed of the Reset Gate RG, Horizontal Driver H1 to Horizontal Driver H4, and SHP/SHD sample clocks, is the foundation for generating the timing for both the CCD and the AFE. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling [13]. AD9974 can be seamless connection with ICX625AQA and can conveniently connect the clock signals to the ICX625AQA pins i.e. H_{1A}, H_{1B}, H_{2A}, H_{2B}, and RG₁, RG₂. AD9974 has two three-wire serial communication interfaces which can be used to configure the internal registers for generating the horizontal clock pulse and forward analog control signal. There also are two high-speed master clock signals named CLI_A and CLI_B are generated as internal reference clock inputs which is should be pay attention in PCB layout to avoid noise interference.

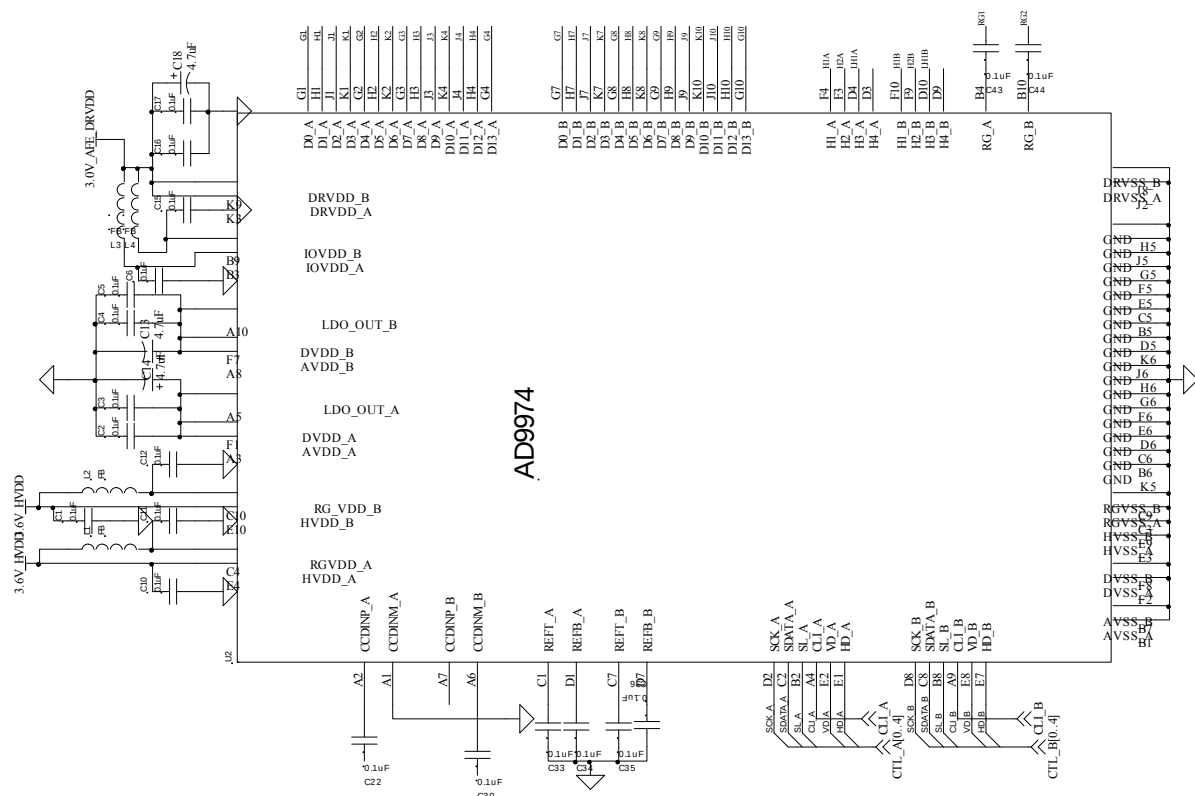


Fig. 2. AD9974 Signal connection schematics.

3.2. The Vertical Drive Circuit

In generally, The output voltage amplitude comes from FPGA can't satisfy the requirement of CCD sensor vertical drive signal, To deal with this issue, we choose the exclusive drive chip produced by SONY named CXD3400 as CCD vertical driver chip. CXD3400 contains six channels and can work at the high-speed readout mode. The CCD sensor ICX625AQA must be driven in ten channel vertical signals which are $V_{\phi 1}$, $V_{\phi 2}$, $V_{\phi 3}$ and $V_{\phi 4}$ four-phase vertical drive signal while the signal $V_{\phi 2}$ and $V_{\phi 3}$ further are divided into four signals. So, we have to use two CXD3400 chips to deal with the ten signals simultaneously. When the conversion inside the CCD sensor has been completed, the signals of $V_{\phi 2}$ and $V_{\phi 3}$ provide the VH, VM and VL three-level signals synchronically to read out to the vertical conversion signal. The one thing we have to emphases is that the pins of CXD3400 process circuit must be connected to FPGA pins directly in specific rule in order to ensure proper signal generation. The vertical drive circuit schematics based on two CXD3400 is shown in Fig. 3.

3.3. Voltage Generation Circuit

The power stability is crucial for ICX625AQA, even minimums voltage fluctuation can lead to this

high-precision sensors break down. On the other hand, the power has to own some redundancy capacity than pre-estimated total power consume [14-15], in our paper, we adopt the special power supply chip produced by Texas Instruments named TPS54594 which is a DC/DC power switching chip with dual 5 V (4 A/2 A) output and requires 12 V input. The 5 V/4 A power channel supply power to the TPS54286 and two LDO which are other power switching chips, The TPS54286 outputs the 3.3 V voltage for FPGA system while the two LDO output 3.0 V and 3.6 V voltage for AD9974 respectively. The 5 V/2 A power channel supply power to LT3486 exclusively. The LT3487 dual channel switching regulator generates positive and negative outputs for biasing CCD imagers. The device delivers up to -8 V at 90 mA and 15 V at 45 mA from a lithium-ion cell, providing bias for many popular CCD imagers. Low cost LDO linear regulator, low noise, quiescent current, which is its outstanding advantages. DC/DC switching power supply chip advantage is the high conversion efficiency can be high current, but the output disturbance is large, the volume is relatively large. According to the advantages and disadvantages of the two power chip, we chose this construct power circuit. Voltage Generation Circuit schematic diagram is shown in Fig. 4.

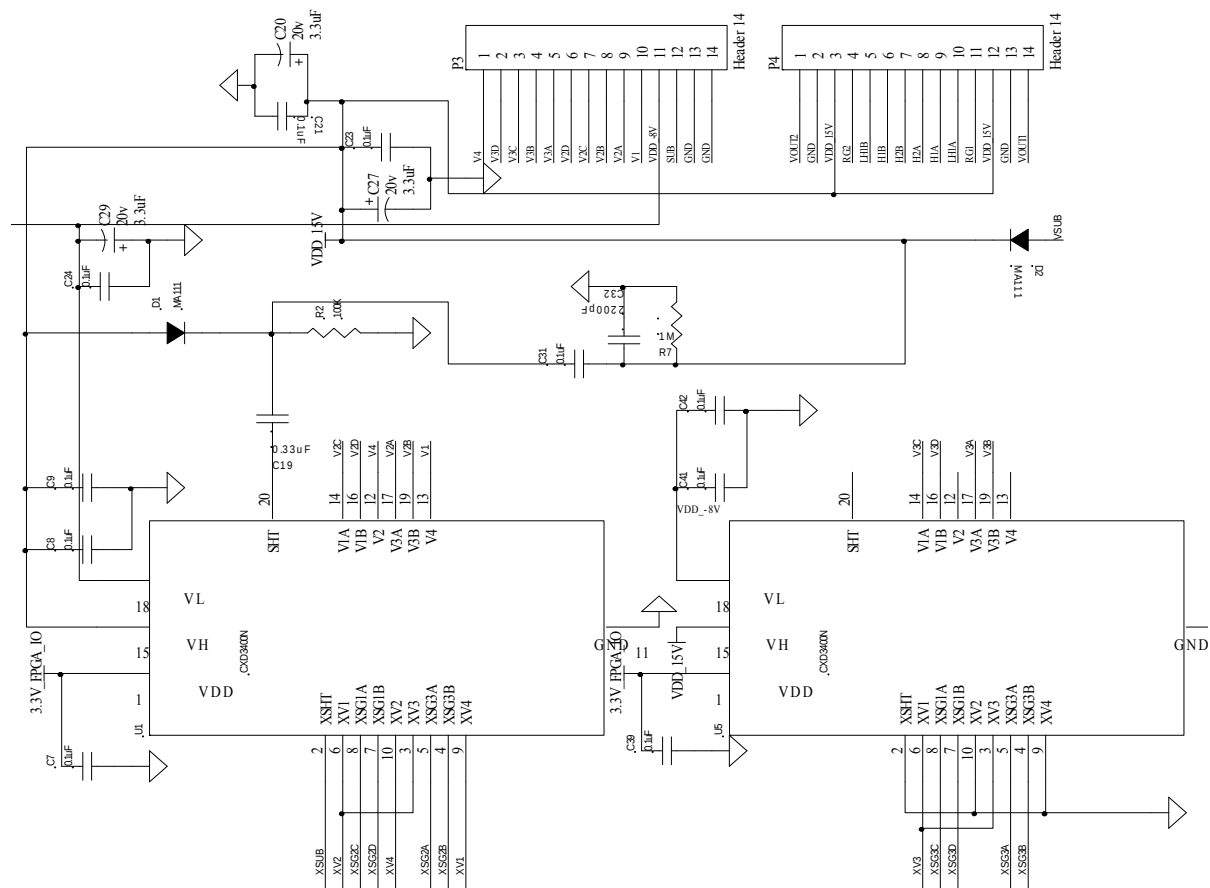


Fig. 3. CXD3400 Signal connection schematics.

4.2. Driver Timing Design

In our program, we design the complicated driver timing in Verilog HDL language [19]. The detailed procedure about the software diagram is shown in the Fig. 6. The program running in FPGA is divided into several modules. The pixel counter module which initialize the AD9974 controls the horizontal and vertical signal by means of two counters [20], AD9974 initialization module is called three-wire serial interface module to do the initialization of AD9974 module. The counters begin to count as soon as the configuration procedure finished. So the AD9974 module and the CXD3400 module generate horizontal and vertical clock signal synchronically. When one frame AD conversion is completed, the counter module calls the image read module reads image data. We will discuss the horizontal and vertical drive timing design separately in following sections.

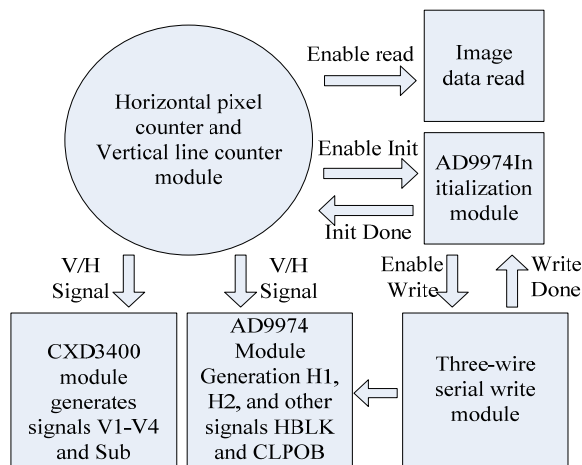


Fig. 6. The workflow of software.

4.3. Horizontal Drive Timing Design

Horizontal drive module consists of three sub-modules which are three-wire serial write module, AD9974 register initialization module and vertical sync counter module [21]. Through the initial configuration, the AD9974 internal Precision Timing core uses a master clock input (CLI_X) as a reference. This clock input should be the same as the CCD pixel clock frequency. The internal timing core divides the master clock period into 64 steps or edge positions, the high speed clocks, RG, H₁ to H₄, SHP and SHD, are generated by positions. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. The H₁ and H₂ horizontal clocks have separate programmable rising and falling edges, as well as separate polarity control. The time sequence of those signals is shown in Fig. 7. There are 1924 raw bits signal transferred by horizontal synchronization signal HD. There are 1228 effective pixels within the raw bits. In

synchronical valid period, the HBLK and PBLK signals occupy 615 bits during in effective voltage phrase, in the similar way, CLPOB signal occupies 40 bits, the rest are blank bits.

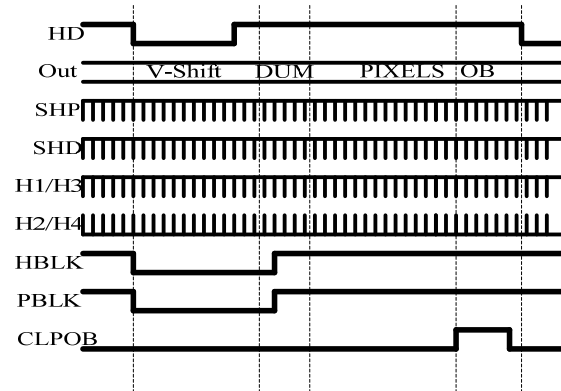


Fig. 7. The basic horizontal signal timing diagram.

4.4. Vertical Drive Timing Design

Once anyone image frame is outputted, the next frame must be transferred to vertical field. As we know the CXD3400 chip provides the vertical transfer clock signal which is valid during this transferring period. When each row of pixels shifts, CXD3400 module acts once. The four-phase vertical transfer signals are shown in Fig. 8. The signals also are combined by CXD3400 to meet the requirement of vertical transfer clock.

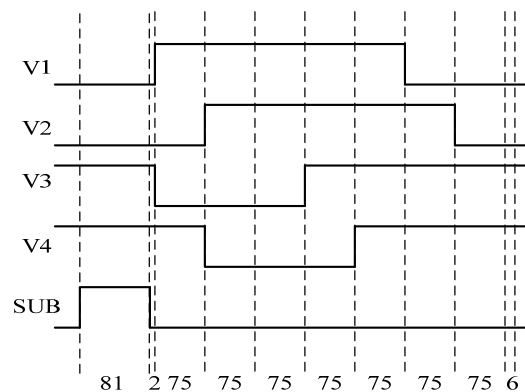


Fig. 8. All pixels read timing diagram.

4.5. Timing Logic Simulation

The designed and implemented drive timing program is simulated in the Signal Tap IDE [22]. The simulation of three-wire serial control signal which is used in AD9974 is shown in Fig. 9. The simulation signal contains enable signal Send_En, complete signal Send_Done, allowing signals SL and transmit serial clock signal SCK. When Send_En become effective status, SL signal becomes low to activate

serial port to sent out valid data at the edge moment of SCK rising. When the data transfer finished is completed, Send_Done will drop down the voltage level to notify FPGA that the whole frame data has been transferred completely, then the FPGA will start

up or terminate the next frame data acquisition process according to the situation of Send_En signal. SL signal is effective at each rising edge of SCK data read period. SL at least keeps ahead the rising edge of SCK t_{ls} nanoseconds.

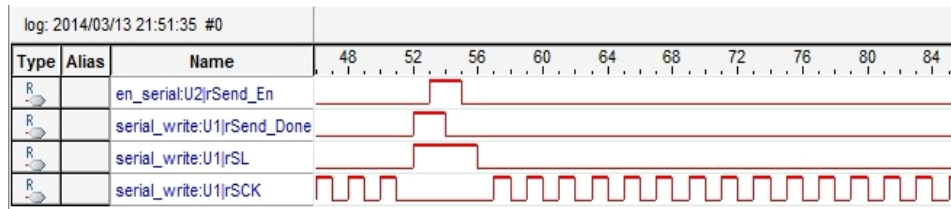


Fig. 9. Serial control module simulation diagram.

FPGA must provide the vertical sync and horizontal sync clock signal to motivate the AD9974 generates the horizontal drive clock [23]. Meanwhile, the Sub exposure signal and the vertical transfer clock signal also are accompanied by FPGA. The signal time sequence is shown in Fig. 10. In this figure, we can figure out that when the horizontal synchronization signal is valid, the signals of Xsub and Vsub combines to generate Sub signal as well as the signals V_1 - V_4 combines to generate the vertical transfer signal.

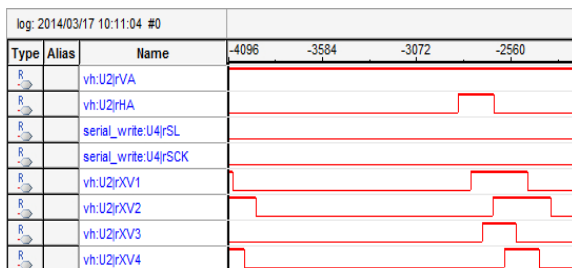


Fig. 10. Sync signal and the vertical transfer signal simulation diagram.

5. Experimental Test

After the completion of the production of circuit boards, through the timing analysis, we completed the design of the driver modules, and ultimately successful run on the board in the simulation test. AD9974 and CXD3400N output signals are shown in Fig. 11. Because the oscilloscope only has two probes, SUB signal is a reference signal for the combination of V_1 - V_4 in Fig. 11. Fig. 12 is the waveform of the horizontal drive signal, the vertical works in the idle phase. The bandwidth of oscilloscope is 100 MHz, and when the horizontal drive signal reaches 60 MHz, the waveform is display with a certain amplitude error.

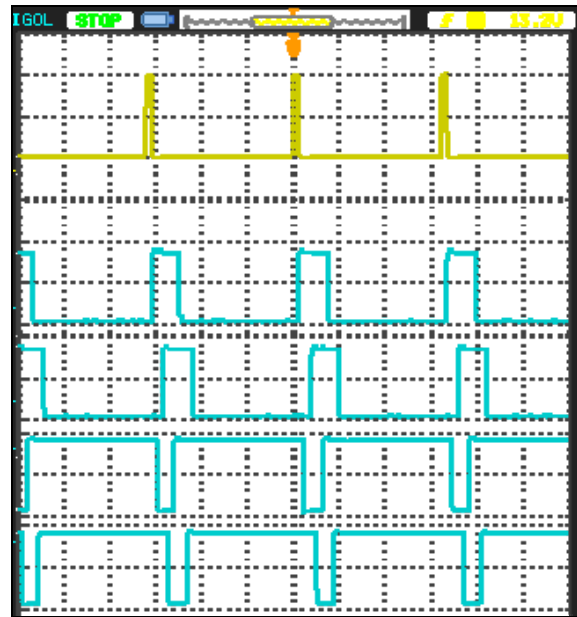


Fig. 11. The waveform of vertical drive signals

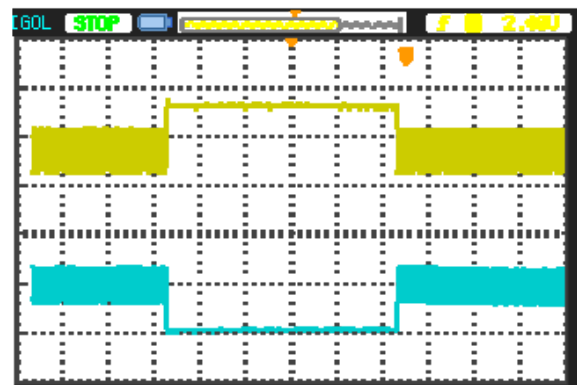


Fig. 12. The waveform of horizontal signals.

6. Conclusions

In this paper, we discussed how to design and implement the novel CCD sensor driver system

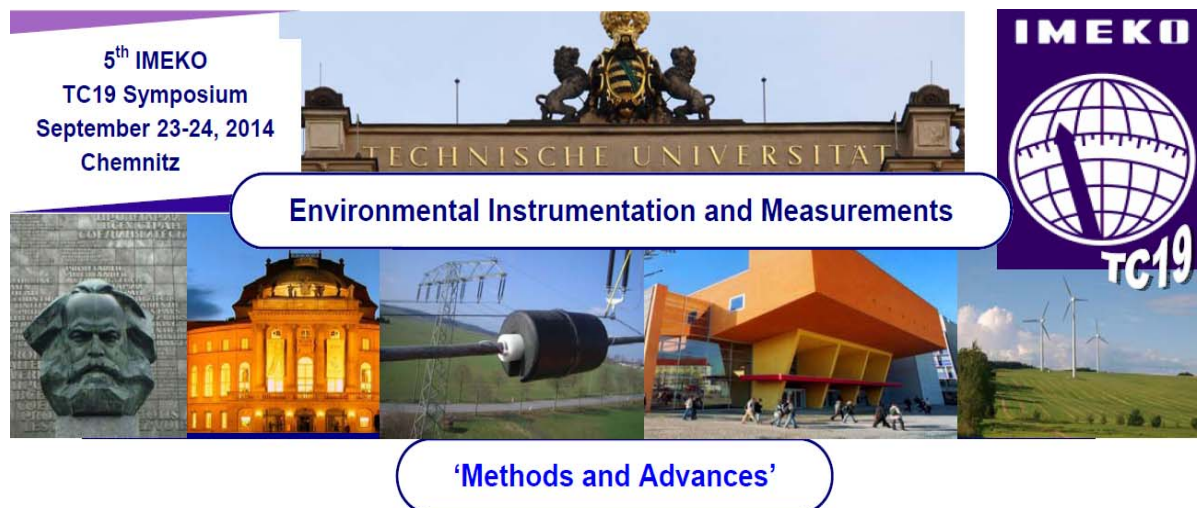
based on FPGA. The working principle and driving timing sequence about ICX625AQA the interline CCD image sensor used in our system are discussed in detail. We adopted the special vertical driver chip CXD3400 and horizontal driver chip AD9974 to enhance anti-jamming capability of the circuits, the peripheral circuits including AD9974 and CXD3400 are illustrated as well as some simulations are conducted to verify the correctness of the process program. Our work provides a practical approach to implement the efficient and effective CCD sensor image acquisition task in customizing pattern.

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