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A Novel Approach for Simple, Fast and Cheap Packaging of MEMS and MMIC

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Abstract: The packaging of MEMS and MMIC devices has become a trending topic in the last years. This paper presents a novel approach for MEMS and MMIC packaging. The proposed packaging procedure combines simple single layer printed circuit board (PCB) techniques, Wire-Bonding and 3D printing, resulting in a simple, fast and cheap alternative. Since there is no need for Via Holes the package performance is privileged while the fabrication process is simplified. The novel approach was used in the design and fabrication of a package for a RF MEMS digital phase shifter. The simulation and measurements data are presented alongside with the related conclusions.

Keywords: Packaging, MEMS, MMIC, PCB, LTCC, Wire-Bonding, Via Holes, Pick and Place, Phased array antennas, SMD, Flip chip, S11, S21 and S22.

1. Introduction

The most of electronic devices are vulnerable up to some degree to the surrounding environmental conditions and packaging is the key word to solve this issue. The MMIC and RF MEMS are not exceptions to this rule, on the contrary, they present especial requirements and constrains to the packaging technologies in order to guarantee that there is no significant performance degradation for packaged devices. Both of them, the MMIC and the RF MEMS, have experienced a migration from the military field (low volume and almost independent cost) to the massive commercial applications (high volume and mainly bounded cost). The transition to high volume commercial applications has pulled the attention on new packaging techniques which require low cost, high out-put and compatible with standard automatic circuit production (i.e. compatible with SMD Pick and Place machines).

Many efforts in the development and improvement of packaging techniques have been reported in the literature. In [1] a typical low frequency package technique like injection molding is improved for RF and microwave applications showing very good performance but, the injected material makes it not suitable for some high frequency MMIC and for the RF MEMS, in which usually there are moving parts. In [2] a variation of the injection molding technique is presented by which instead of injecting the whole circuit, a base is injected at first on which the chip is bounded and wired and, finally, it is covered with a lid leaving the chip inside an air cavity. The technique overcomes some of the issues of classical injection molding technique related to the chip embedding into the material which is still showing a low flexibility in the package to board RF transitions. Consequently, a new expensive matrix must be designed every time that a new transition is applied. The design of freedom degrees is limited due to process constraints, thus resulting in a not robust design.

In [3-5] interesting LTCC and PCB based packaging techniques have been proposed overcoming the most issues of injection molding. But, the need for Via Holes, the complex alignment techniques required for the multiple fabrication steps and the LTCC cost make them less attractive for some applications because of lower design robustness, fabrication limitations and higher cost.

In this paper, a novel approach is proposed which is based on simple and reliable PCB single layer and 3D printing techniques. The approach was validated through the design, fabrication and measurement of a package for a RF MEMS phase shifter. The objective of the phased array antennas combines the functions: 2-axis gimbal and gimbal controller, in a single, low-cost package. Phased array technology offers significant benefits over mechanically pointed parabolic antennas, including the elimination of deployable structures, moving parts and torque disturbances due to moving antennas impart in the spacecraft applications. The phase shifter is a fundamental component in the phased array antennas. This component allows to modify the signal phase on each irradiating component of the array, to control the position of the radiation beam as emitted by the antenna.

The design process, as well as the simulated and measured data, are presented in the following paragraphs of this work.

2. The Proposed Approach

The proposed approach uses Flip chip technique eliminating the Via Holes need and, consequently, the well-known and simple standard single layer PCB techniques are able to be applied.

The use of standard PCB techniques offer higher design flexibility for both, the package to chip and the package to board transitions, since it is possible to integrate different structures like: transmission lines, stubs, inductors and interdigital capacitors. Higher design flexibility and simplicity cause a better output and design robustness driving to a shorter design cycle and a lower design cost.

The package consists of two main parts: a PCB board acting as a base where the device to be packaged is mounted and a plastic lid which closes the package and protects the device forming an air cavity (Fig. 1).

Once the PCB base is designed and fabricated, the chip is electrically connected using Wire-Bonding techniques (Fig. 2).

In Fig. 2, it is possible to observe the RF access lines and a T-shaped line on the side of the PCB board. On the T-shaped line, an electrostatic voltage is applied to the MEMS RF switches to get down a membrane which will cause a capacity variation. This change will produce a different exit phase with regards to the entry phase.

A plastic lid is then fabricated by direct 3D printing and it is mounted on the PCB thus shutting it, forming an air cavity and fabricated by direct 3D printing and it is mounted on the PCB thus shutting it, forming an air cavity and closing the package (Fig. 3). The 3D printing can be performed in a particular environment, surrounded by an abundant gas atmosphere (i.e. Ar or H_2) in order to preserve the packaged chip from humidity. This may be required for some vulnerable circuits and components like the RF MEMS switches.

The resulting package is compatible with the standard SMD Pick and Place production equipment and it was designed to be mounted using Flip chip technique (Fig. 4).

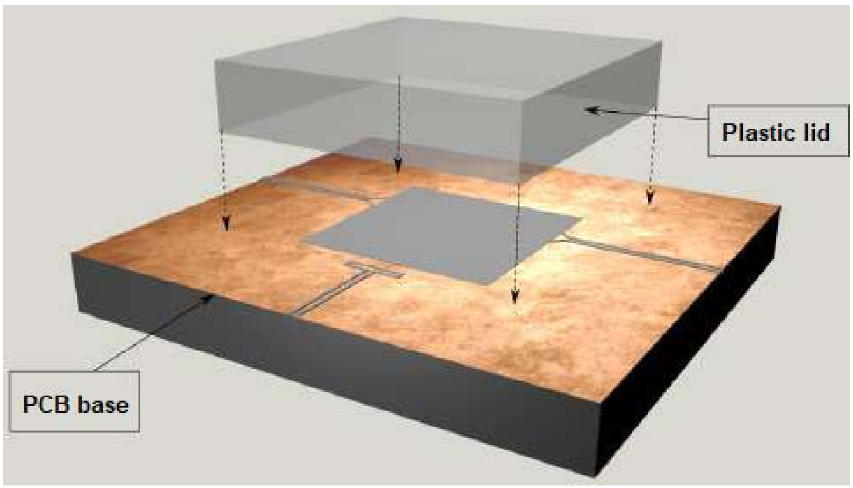

Fig. 1. Package main pieces: single layer PCB base and plastic lid cover.

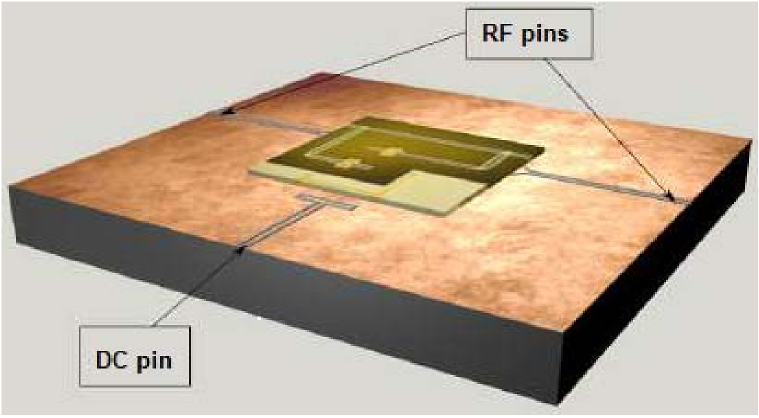

Fig. 2. Example of the PCB base and mounted chip on it.

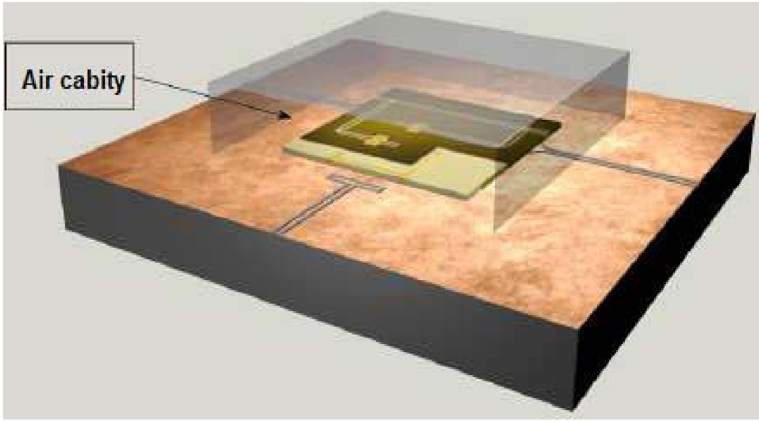

Fig. 3. Complete package. Half of the plastic lid was cut and removed from the drawing to show the air cavity inside the package.

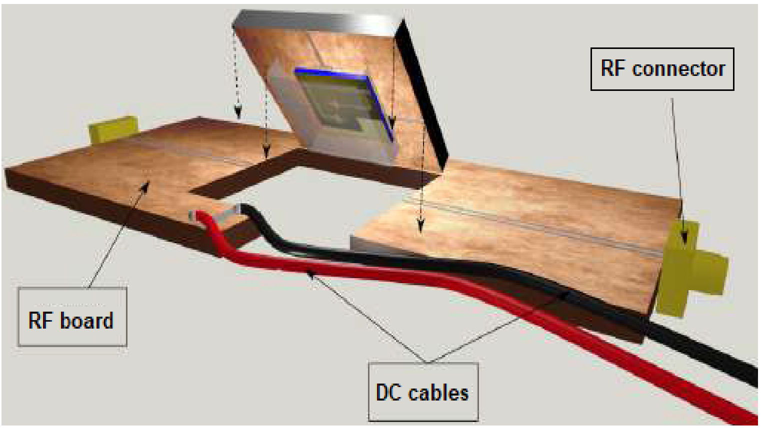

Fig. 4. Mounting of the Flip chip package on the board side. Half of the plastic lid and a quarter of the board were cut and removed from the drawing to show the air cavity inside the package and the details of the Flip chip mounting.

3. Package Design and Simulations

In order to evaluate the feasibility and quality of the proposed technological approach, it was tested through the design of a package for a RF MEMS phase shifter operating in a 200 MHz band around the 8.25 GHz.

Specifications to be accomplished for the package performance are reported in Table 1.

Table 1. Package specifications.

Specification	Value Limit
Return Loss	< -10 dB
Introduced Additional Insertion Loss	< 1 dB

The package design can be partitioned into the following main design tasks:

- Design of the chip to package transition (including chip, Wire-Bonding and package PCB board). For a successful design take all them into account for a successful design.
- Package design to board transition at RF and microwave frequencies. The footprint on the board will be part of the package and should be included in the design from the beginning.
- Final evaluation of the overall package performance and a reliable optimization. The former tasks involve 3D electromagnetic (EM) simulation, modelling and microwave circuit CAD simulations.

The first step was to derive a model of the device to be packaged. This can be a 3D electromagnetic model, being usually the case for passive devices like filters, RF MEMS, etc. In this case, the device to be packaged was the RF MEMS phase shifter [6] reported in Fig. 5.

The next step was to perform a 3D electromagnetic model of the full package including the lid and the chip to package transition. The resulting model was simulated and optimized considering the tabulated specifications so as to define the PCB, the Wire-Bonding (with Ag) and the plastic lid (Fig. 6).

The next step was to include the effect of package on the board transition. A 3D model of the [full board + package + chip] system was created and simulated for the final tuning and the evaluation of the design performance. The simulation shows the whole device adaptation to both RF MEMS switching states which are part of the MEMS phase shifter. Both curves remain lower than 10 dB (specified and tabulated values). Simulation can be observed in Fig. 7. In the same Figure, the simulated packaged and naked devices performance are compared.

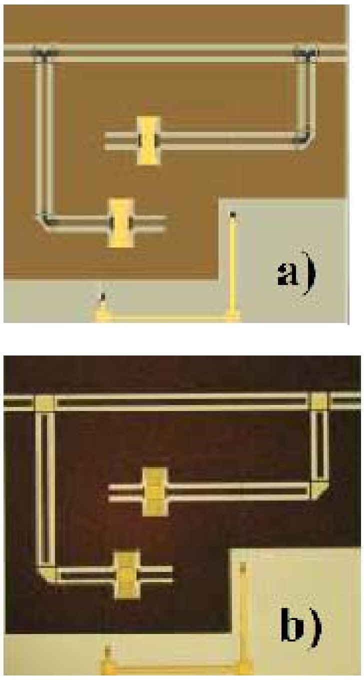

Fig. 5. RF MEMS to be packaged: a) 3D model for EM simulations, b) photograph of the actual chip.

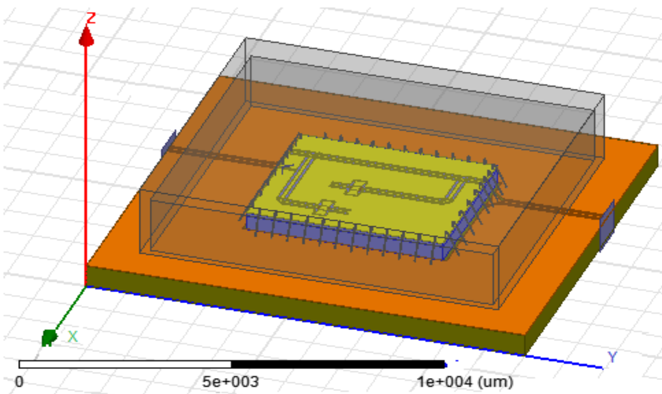

Fig. 6. CAD Figure of the 3D electromagnetic model to simulate the packaged chip.

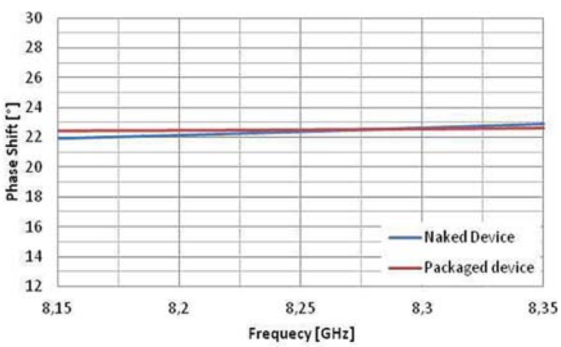

Fig. 7. Module of S11 parameter, which was simulated with the phase shift using the RF MEMS in their two states (on and off).

4. Fabrication Measurements Set-up and Results

In order to validate the proposed approach the designed and simulated package was fabricated and the corresponding RF MEMS phase shifter was packaged inside. The performance of the packaged device was measured and compared to simulations and to the naked device measurements.

4.1. Package Fabrication

The package base was fabricated on a Ro3010 substrate using a standard PCB lithographic process to print the circuit. The Ro3010 substrate was selected due to its dielectric constant (Ɛr) value of 10.2 because it is very close to the one of the high resistivity silicon substrate (Ɛr =11.63) of the RF MEMS phase shifter [7]. The matching between the Ɛr values simplifies the chip to package transition since both access lines, on the chip side and on the package side, will exhibit similar dimensions. The corresponding mask and the actual board are shown in Fig. 8.

After the PCB base fabrication, the chip was bonded to the base using a nonconductive glue (Sn992-Pb free). This a welding alloy with a low melting point temperature, compatible with the thermal properties of the lid material. Cabling was then fabricated using the Wire-Bonder machine reported in Fig. 9.

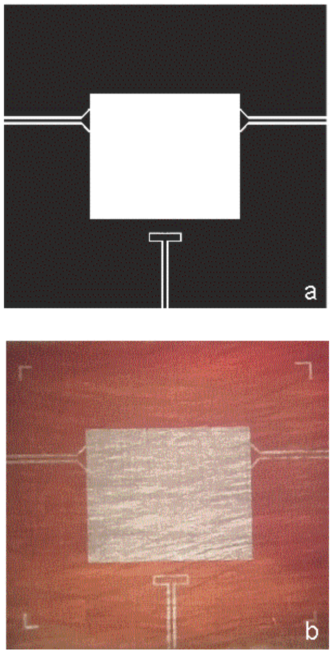

Fig. 8. Package base: a) mask for photolithography; b) Actual fabricated PCB board fabrication.

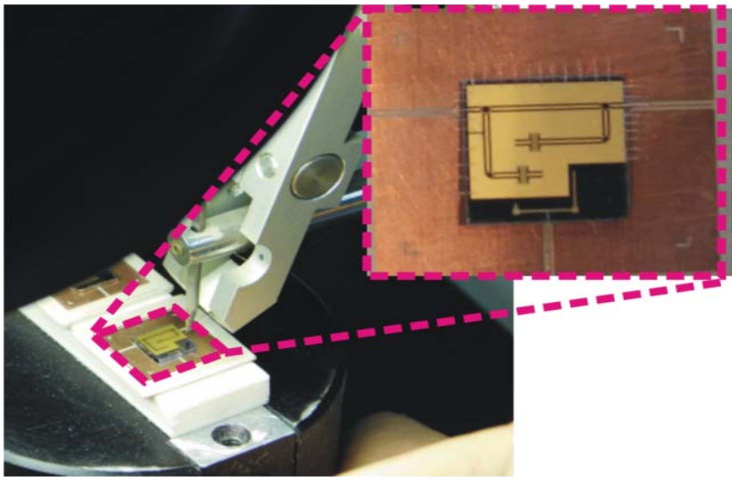

Fig. 9. Wire-bonding set-up and details of the wired chip to the PCB.

The package fabrication was then finished by 3D printing of the lid, closing the package and creating the air cavity which will contain and protect the chip from eventual adverse environmental conditions. For the 3D printing of the lid, an especial alignment procedure was carried out in order to assure its correct placement. The 3D printer was put into a sealed chamber (Fig. 10) under Argon atmosphere in order to avoid the trapping of humidity residuals into the package. The final package was mounted in a PCB containing the designed trails, it is shown in Fig. 11.

4.2. Measurement Set-up and Results

The final package was mounted on a PCB board containing the designed footprint. The package was welded using Sn992 Pb-free Soldering Alloy which exhibits a low temperature melting point compatible with the lid material thermal properties. The mounted package was then measured using the set-up reported in Fig. 12.

In order to remove the undesired effects of the VNA cables, RF and PCB test board connectors, the corresponding set of TRL standards [8] (Fig. 13) were designed, fabricated and used for the instrument calibration.

The relevant data, as obtained from the S parameter measurement, are presented (Fig. 14(a, b, c) and comparison between the packaged and naked chips are shown. As it can be noticed from measurements data, all the proposed specifications were included in the requirements accepted for a typical package.

Fig. 10. Sealed chamber under Argon atmosphere, to which the package plastic lid was bonded.

Fig. 11. Photograph of the final package.

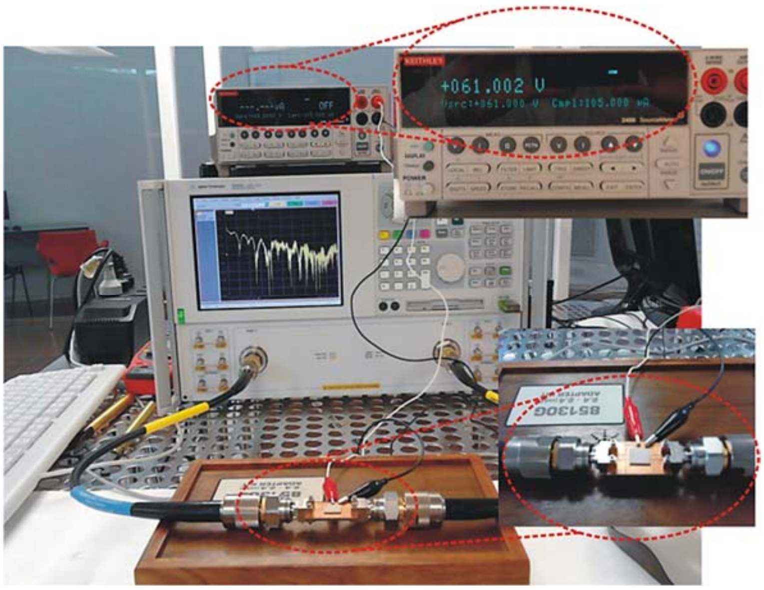

Fig. 12. Measurements set-up and details of the final board assembly.

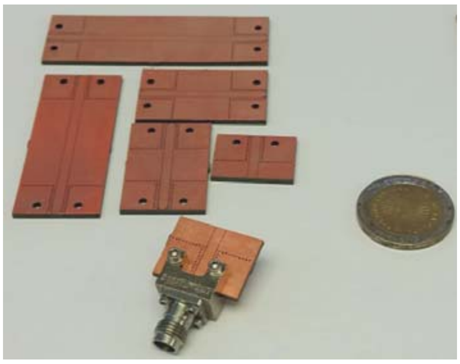

Fig. 13. PCB sheets to calibrate the TRL of the vector network analyzer (VNA).

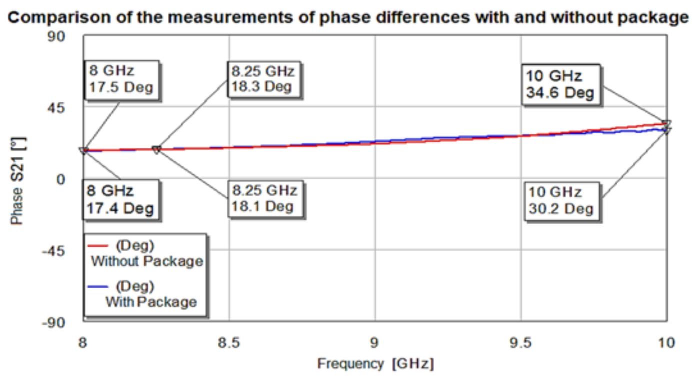

Fig. 14(a). Measured phase shift (Δφ) before and after packaging measurements. Results show that the package introduces an acceptable degradation with regards to the specifications.

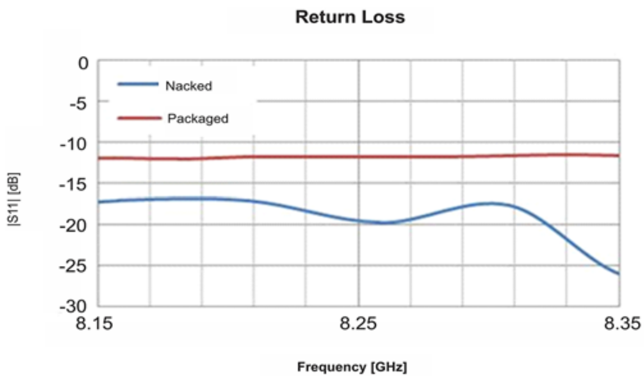

Fig. 14(b). Measured input return loss, before and after packaging, show that the package introduces degradation and keeping the return loss better than the -10 dB specification.

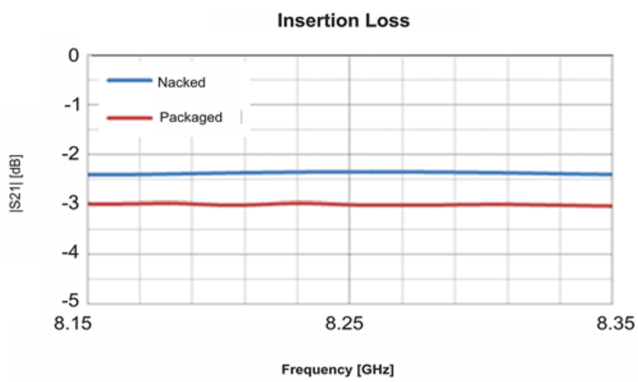

Fig. 14(c). Results of measured insertion loss show the additional less than 0.5 dB, thus fulfilling a better value than 1 dB specification.

Electrical measurements, as well as the phase shift in the naked chip and that of the packaged device, have driven to interesting results which validate the proposed package. Besides, this type of development is economically accepted since it only consists of a PCB and a 3D printer to implement it. With regards to possible future work, several packages could be fabricated by printing on a large surface of PCB chips (which could be previously bonded and connected by Wire Bonding techniques). This type of packaging, contributes to solve problems related to climatic and surrounding situations in naked chips, exhibiting this work line a considerable low cost.

The fabrication was performed with low cost standard PCB and 3D printing process result shows that it is possible to use the proposed approach to produce simple and cost effective packages by combining standard single layer PCB and 3D printing techniques feasibility of the proposed approach work on this topic, two important performed regards the formal evaluation of the package's lid mechanical adhesion and the production of a significant number of packages in order to evaluate the package quality by thermal cycling and harsh environment tests.

5. Conclusions

In this work, the simulation and the laboratory validation of a low-cost package for RF circuits and MEMS microwaves is proposed. Details of the fabrication, from the mask design to the measurement of the finished device are described. It is concluded that the degradation which was introduced by the package is minimal and its behavior can be compared with that of Argon packaged devices. Besides, measurements of these devices have revealed a similar output as compared with that of commercial devices of this type.

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