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Research on the Relationship between Phase Synchronization and Frequency Stability in Atomic Clock Circuit

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Abstract: The implementation of the atomic clock circuit usually adopts frequency processing scheme. However, the quantization error in frequency processing greatly limits the frequency stability of the atomic clock's output from theoretical calculations. This paper analyzes the cause of quantization error and its relationship with the degree of signal synchronization. Based on this relationship, we study the effect of phase synchronization on frequency stability and explore how to effectively suppress quantization errors to improve measurement accuracy. Experiments show that using the regularity of phase information obtain continuous and lossless phase information. It can improve the accuracy of the gate acquisition and reduce the influence of quantization errors. Frequency stability can be improved from $1/\tau^{1/2}$ to $1/\tau$. The research on this relationship can be applied in various fields, such as high precision measurement of time and frequency, communication technology, navigation signal processing, and even defense science and technology for essential improvements.

Keywords: Frequency stability, Phase synchronization, Frequency measurement, Frequency processing, Quantization error.

1. Introduction

It is the highest accuracy and stability of frequency and time [1-2]. Measuring frequency and time is the most important activities for many fields [3-4], such as radar navigation, mobile communications, aerospace and navigation, geological exploration and other fields. The frequency source measurement accuracy cannot meet the theoretical requirements. Thus, improving measurement precision is a common issue. The frequency stability of the hydrogen atomic clock changes with time along $1/\tau$ (developed by the Shanghai Astronomical Observatory in 2006 [5]). The frequency stability of the crystal oscillator below a few seconds also conforms to the law of change. This phenomenon is the same as the trend of the phase processing law derived from the control of the phase-continuous atomic energy level transition phenomenon [6]. Passive atomic clocks, such as rubidium clocks and cesium clocks use frequency

processing schemes, and its medium and long-term stability changes $1/\tau^{1/2}$ as time goes on. Products implemented by phase processing show higher frequency stability. However, owing to insufficient understanding of the complex phase phenomenon and the complicated of structure for phase processing. The frequency-based processing scheme appears in many precision frequency source [7]. In order to achieve high accuracy, it is further researched that frequency stability changes from $1/\tau^{1/2}$ to $1/\tau$. This paper uses phase synchronization processing to obtain continuous phase information, studies the influence of phase synchronization degree on phase information, and effectively controls the switching position of the gate to suppress the quantization error caused by ADC, thereby improving the frequency stability of the standard devices.

2. The Relationship between Quantization Error and Phase Synchronization

In high-precision frequency measurement, the measurement accuracy of instruments and meters is subject to certain limitations due to interference from process defects, complex circuits, and noise. Especially, when the analog signal is converted into digital signal, part of the phase information of the output signal is lost due to phase asynchrony, resulting in a deviation between the output value and the actual input value. The actual input and output signal difference size is related to the number of ADC quantization bits, that is, the sampling rate decreases as the number of ADC bits increases. Due to the limited number of ADC bits, the resolution of the measurement is limited, resulting in inherent information loss in the quantization process of analog signals. High-precision measurement can be obtained with high-digital ADC for digital measurement, but it is still inevitably affected by quantization error, conversion rate, signal bandwidthand so on. These factors limits its application [8]. Digitization makes the phase continuity can be better obtained during atomic energy level transitions. Different state of phase synchronization causes different phase information loss in the output signal, which can result in quantization error between the output value and the actual input value [9]. The quantization error is related to ADC (Analog-to-digital converter) bits.

When input voltage U is constant, several or several adjacent sampling points of the output signal are quantized to the same digital value due to noise interference. The sampling points change step by step within a period, this is the fuzzy area ΔR [10], which can be calculated by

$$\Delta R = LSB = \frac{1}{2^N} U , \tag{1}$$

where LSB is the least significant number, N is ADC bits and U is input voltage. Eq. (1) sees that fuzzy area is equal to least significant bit. Or fuzzy area ΔR can also be obtained by knowing the voltage and the number of ADC bits. The center position of fuzzy area is closer to true value, but it is technically difficult to achieve [11].

Therefore, the actual difference value of input and output or ADC quantized voltage value needs to be continuously corrected according to the distance from the border to the center. And it can only be infinitely close to the true value. However, the maximum quantization error is expressed by

$$\Delta V = \frac{1}{2}\Delta R = \frac{1}{2} LSB , \tag{2}$$

where ΔV is the maximum quantization error. For N-bit ADC, the half of the fuzzy area is called maximum quantization error. Meanwhile, the maximum quantization error can be expressed as 1/2 LSB.

For a measurement system, the magnitude of the ADC quantization error directly affects the accuracy of the sampling position. For a multi-period sampled input signal, the adjacent sampling points change in a single direction at fixed time intervals, that is, increase or decrease. When data points are strictly synchronized between transition border and sampling clock. The sampling points can sequentially cover all phase information. There is a flat area after sampling, in which the ideal phase coincidence point is hidden and difficult to capture. Therefore, the border of fuzzy area is selected as the flag of gate switch to improve the resolution of measuring equipment and finally achieve better accuracy. The accuracy improvement factor is expressed by quantized fuzzy area and the stability of quantized fuzzy area. Therefore, the accuracy improvement factor is calculated by

$$A = \frac{\Delta R}{\Delta \delta} , \tag{3}$$

where A is the accuracy improvement factor, ΔR is the quantized fuzzy area, $\Delta\delta$ is the stability of quantized fuzzy area, which is determined by the slight deviation of δ_1 and δ_2. The calculation formula of $\Delta\delta$ is

$$\Delta \delta = \delta_1 - \delta_2 , \tag{4}$$

where $\Delta\delta$ is much smaller than δ_1 and δ_2. The slight deviation of δ_1 and δ_2 is respectively error value at the switch gate and is also the interval between ideal gate and actual gate. The size of quantized fuzzy area $\Delta\delta$ is related to the resolution. Principle of quantization error suppression is shown in Fig. 1.

Where the bottom line is actual gate. The middle line is ideal gate. The top line is the selected border.

It can be seen from Fig. 1 that actual position is different from ideal position. The ideal door signal is difficult to capture. The quantization border has the highest stability and the highest accuracy. Therefore, selecting the value at the border is regarded as the switch flag of the measurement gate.

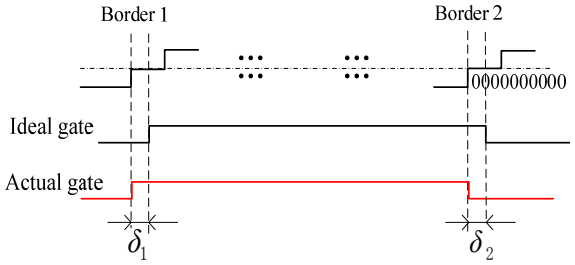

Fig. 1. Principle of quantization error suppression.

It can be discarded the background of circuit of random noises, such as noise and environmental noise. Although the selected location is different, the relationship between actual sampling point and ideal point is the similar. The total gate time remains unchanged so that it is closer to the true phase coincidence point or the true value. The method of selecting the gate by the border effectively offsets the measurement fuzzy area caused by ADC quantization. Therefore, the value at the border of the sampling point can effectively suppress the problem of insufficient ADC quantization resolution. Quantization error can be eliminated and phase synchronization greatly is improved, thereby improving the accuracy of its measurement control.

The actual error is different from the ideal error. However, the actual error can be expressed as

$$\Delta V' = \frac{1}{2}\Delta\delta = \frac{\Delta R}{2A} = \frac{1}{2A}LSB, \tag{5}$$

where $\Delta V'$ is the actual error, which is half of the stability of quantized fuzzy area. And the ratio of ΔR to 2A is expressed as $\Delta V'$. Of course, the actual error can be calculated by the ratio of LSB to $2A$.

3. Experiments and Analysis of Different Phase Synchronization Degrees

3.1. Experimental Scheme

The precision frequency measurement of block diagram is shown in Fig. 2. The two-way signals meet the same frequency and have a small frequency difference. One way is measured signal $f_1=\Delta f+f_0$ and clock signal f_r, the other way contains reference signal f_0 and clock signal f_r. Clock signal f_r is the special and stable intermediary source signal. f_r only serves as an intermediate bridge, avoiding two signals between f_0 and f_1 direct comparison.

It can be seen from Fig. 2, two-way signal is sampled by dual-channel ADC to get Δf_1 and Δf_2. The sampling data of ADC is received in FPGA. Due to noise interference, filter is required to filter out the influence of random noise. The gate opening and closing time can be generated. N_0 and N_1 are calculated by the gate time signal generation circuit in FPGA. Two-way count value can be sent to MCU by serial communication protocol. The error signal ε is calculated by MCU. ε is generated by frequency difference that has been set $\Delta f'$ and the actually obtained frequency difference Δf. Then, ε is converted into a corresponding voltage u_c by DAC. VCXO is driven by u_c for precise frequency control in a closed loop. The correction of the measured signal frequency has been achieved by real-time adjustment signal frequency.

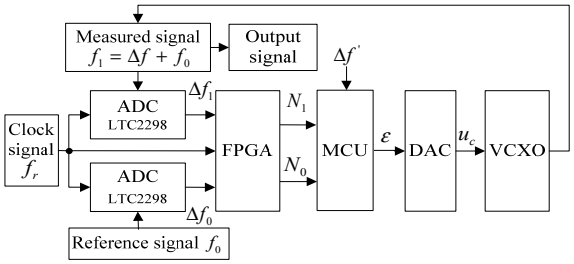

Fig. 2. Block diagram precision frequency measurement.

Within the period required for the phase of the measured signal and the reference signal to completely coincide, relative phase deviation between reference signal and measured signal is arithmetic series is calculated by

$$\Delta T = \frac{f_{maxc}}{f_o f_1}, \tag{6}$$

where ΔT can reach the order of picoseconds. ΔT is step value in arithmetic series, that is, quantized phase shift resolution. f_{maxc} is the frequency of greatest common factor. The reciprocal of f_{maxc} is the least common multiple period, that is, the period required for the phase of the measured signal and the reference signal to completely coincide with each other, f_0 is reference signal and f_1 is measured signal. For the same frequency signals with a small frequency difference, if frequency difference is smaller, the sampling point ΔT is smaller. Therefore, in a least common multiple period, measured signal moves more subtle in phase, and phase information is more complete. For inter-frequency signal, the change of phase difference is often not monotonous but a chaotic change. If the step value of the phase difference between the signals is sorted out of order, it will be found that the step value is still ΔT.

The equivalent counting period and the frequency difference are calculated by

$$T_i = N_j * \frac{1}{f_r}(i, j = 0,1), \tag{7}$$

$$\Delta f_i = \frac{1}{T_i} = \frac{f_r}{N_j}(i, j = 0,1), \tag{8}$$

where T_i (i=0,1) is the equivalent counting period, N_j (j=0,1) is count value of two-way. Equivalent

counting period of two-way can be calculated by count value N_j (j=0,1) and clock signal f_r. Δf_i (i=0,1) is the frequency difference, which has a common intermediate signal. The reciprocal of the equivalent counting period is Δf_i. Of course, Ratio of clock signal and count value of two-way is also expressed as Δf_i. In order to eliminate the influence of common intermediate signals on its results, according to Eq. (6) - Eq. (8), the relationship between f_1 and f_0 can be obtained by

$$f_1 = \left[\frac{N_1 - 1}{N_1} \times \frac{N_0}{N_0 - 1}\right] \times f_0 \tag{9}$$

According to Eq. (9), f_1 can be calculated by N_0, N_1 and f_0. Frequency difference between measured signal and reference signal in the text specifically refers to the frequency deviation between the input signal and the output signal. Frequency difference is calculated by

$$\Delta f = f_1 - f_0 = \frac{N_1 - N_0}{N_1(N_0 - 1)} \times f_0, \tag{10}$$

where Δf is frequency difference. The input reference signal f_o is known. Therefore, the frequency difference can be calculated using the input signal and N_0 and N_x. The output frequency achieves automatically adjusted by Δf.

3.2. Frequency Stability Measurement under Different Frequency Correction

In order to verify measurement accuracy for experimental platform, input terminal f_r and tested terminal f_1 are connected to input and output of the measuring system. Both f_r and f_1 use 8607 as the reference source. The high-stability AFG3101C signal generator is used as a clock signal. (10M-1) Hz is selected by 8607 as an external frequency standard. The frequency stability can be calculated as shown in Fig. 3.

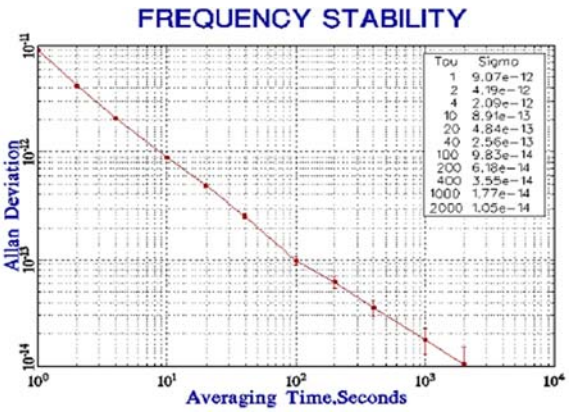

Fig. 3. Characteristic of frequency stability in verifying measurement accuracy experiment.

It can be seen from Fig. 3 that the second-level stability has reached 9.07×10^{-12}. And the thousand-second-level stability has reached 1.77×10^{-14}. At this time, the frequency stability varies along $1/\tau$ as time goes on.

In order to further study the relationship between phase synchronization and frequency stability, different frequency correction values can be selected. 10 MHz of ultra-high stability OCXO 8607 is regards as reference source of Tektronix AFG3101C signal generator, which accesses to the reference signal f_0. The clock signal f_r is set to (10M-1) Hz. Measured signal f_1 is set to 10 MHz from VCXO. The output frequency $f_1=f_0+\Delta f$ can be set to different frequency correction values by connecting with output of VCXO, such as (10M+1) Hz, (10M+2) Hz, (10M+4) Hz, (10M+8) Hz, (10M+10) Hz, (10M+20) Hz. Thus, measurement results of different frequency correction values are shown in Table 1.

Table 1. Measurement results of different frequency correction values.

Δf / Hz	**ΔT**	**Second-level stability**	**Long-term stability**
20	2.00×10^{-13}	1.99×10^{-7}	1.00×10^{-8}
10	1.00×10^{-13}	6.32×10^{-10}	1.25×10^{-11}
8	8.00×10^{-14}	7.92×10^{-10}	1.10×10^{-11}
4	4.00×10^{-14}	2.89×10^{-10}	6.25×10^{-12}
2	2.00×10^{-14}	1.55×10^{-10}	4.10×10^{-13}
1	1.00×10^{-14}	7.07×10^{-12}	2.55×10^{-14}

As shown in Table 1, Δf is different frequency correction values. ΔT is quantized phase shift resolution, shown in Eq. (6).

When Δf =1 Hz, the second-level stability of the output signal is the same as that of the verification measurement accuracy experiment, reaching the order of 10^{-12}. Compared with the verification accuracy experiment, the second-level stability has reached the order of 10^{-12}. When the frequency stability of 1000 s and 2000 s, it can reach the order of 10^{-14}. Therefore, the measurement accuracy is basically the same. In fact, when the phase synchronization accuracy reaches a certain level in the process of system measurement and control, the gate opening and closing flag is more accurate. The system will maximize the suppression of errors, making the output result closer to the true value of the fuzzy area.

When the frequency difference is (1~2) Hz, the theoretical quantization resolution ΔT can reach $(1\sim2)\times10^{-14}$ seconds; when the frequency difference is (4~20) Hz, the measurement resolution ΔT can reach $(2\sim10)\times10^{-13}$ seconds. The phase synchronization accuracy of the signal changes from 10^{-14} to 10^{-13}, and the long-term frequency stability of the frequency source changes from 10^{-14} to 10^{-8} as time goes on. If the phase is continuous when different frequency correction values is 1 Hz. Then, the quantization resolution is too large when different frequency

correction values is 20 Hz. The phase is not continuously sampled. There is a certain gap, and a problem of phase loss.

Experimental result shows that there will have different quantization phase shift resolution and different phase synchronization accuracy under the same hardware conditions. At the same time, the frequency stability will show different changes with the sampling time. For example, the law of frequency stability with time shows $1/\tau^{1/2}$, $1/\tau$ or between $1/\tau^{1/2}$ and $1/\tau$. The frequency deviation of the measured signal can directly affect the resolution of phase processing and the accuracy of phase synchronization. Phase synchronization further affects the determination of the opening and closing time of the virtual gate. Waveforms of frequency stability changes of different correction values are shown in Fig. 4.

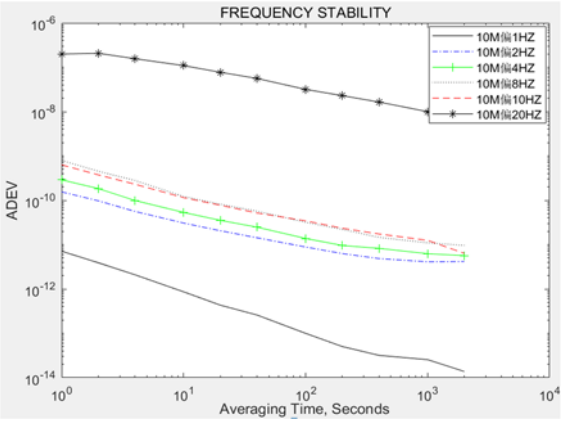

Fig. 4. Waveforms of frequency stability changes of different correction values.

It can be seen from Fig. 4 that as the frequency difference Δf increases, the frequency correction value is different and the quantization phase shift resolution ΔT will also change. The continuity of the phase information of the measured signal and its precision affect the control time of the phase noise on the frequency stability, which in turn affects the accuracy of the gate opening and closing. Fig. 4 shows that the frequency correction value is continuously increased by multiples and the frequency stability is continuously reduced with the continuous increase of the quantization phase shift resolution. That is, the accuracy of phase synchronization between signals is increased, and the information between phases is more comprehensive. Finally, quantization errors can be suppressed, which is expressed as frequency stability of changes from $1/\tau^{1/2}$ to $1/\tau$ as time goes on.

4. Conclusion

In this paper, the cause of the quantization error has been analyzed in digital frequency processing. It has researched the influence of phase synchronization degree on phase information. So the border of the fuzzy area have been selects as the gate switching signal to enhance the problem of phase information loss in traditional frequency processing. The research shows that the phase synchronization accuracy directly affects the continuity of the phase information and thus controls the frequency stability of the frequency source.

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