Sensors & Transducers, Vol. 254, Issue 7, December 2021, pp. 22-30

www.sensorsportal.com

Sensors & Transducers

Published by IFSA Publishing, S. L., 2021
http://www.sensorsportal.com

A Measurement Method Considering Both Phase Noise and Full Frequency Stability

[1] Wei Zhou, [1 *] Miao Miao, [1] Huifang Liu, [2] ChenceYang and [2] Bayi Qu

[1] School of Electro-Mechanical Engineering, Xi'dian University, Xi'an 710071, Shaanxi, China
[2] School of Information Engineering, Chang'an University, Xi'an 710064, Shaanxi, China
Tel.: 13892861331
E-mail: wzhou@xidian.edu.cn, mmiao@mail.xidian.edu.cn

Received: 25 October 2021 /Accepted: 29 November 2021 /Published: 30 December 2021

Abstract: The current mainstream phase noise measurement systems use the reference signal and the measured signal to achieve phase quadrature control after mutual locking, and then through phase information sampling, algorithm processing to get the single-sideband phase noise curve. A novel digital linear phase comparison method - DLPC can automatically keep the orthogonal phenomenon of the signal under test without lock processing. Therefore, it is easy to use and work more stable. This method is different from the traditional method, including the digital DMTD. That is, the frequency stability sampling time corresponding to the deviation of the carrier frequency from 1 Hz to 1 MHz or 10 MHz in the usual phase noise measurement is also the stability index from 1 second to 1 μs or 0.1 μs, respectively. The frequency stability measurement of DLPC can cover the period from the signal carrier frequency to the unlimited time. The new method works more stably, especially in the case of noise interference and poor stability of the measured signal, and lock loss will not occur. At the same time, the new technology can measure the phase noise in time domain and frequency domain simultaneously, and can fully reflect the noise essence of frequency source and the effect of noise influence.

Keywords: Digital, Linear phase comparison, Phase noise measurement, Phase quadrature control, Frequency stability, Carrier frequency.

1. Introduction

Single-sideband phase noise measurement technology plays an important role in the noise analysis of frequency sources and the improvement of its performance. Although the research on phase noise measurement has been conducted for many years, its equipment is complicated and inconvenient to use, especially difficult to obtain information on both time and frequency domain at the same time. Therefore, it is expected that phase noise of frequency domain and frequency stability of time domain can be displayed in one-to-one correspondingly, while its equipment is reasonable simplification and more convenience. In this way, its users could be more fully acquainted the noise of the measured frequency source and its impact.

The current mainstream single-sideband phase noise measurement systems use the reference signal and the measured signal to achieve phase quadrature control after mutual locking, as the Fig. 1 shows [1, 2].

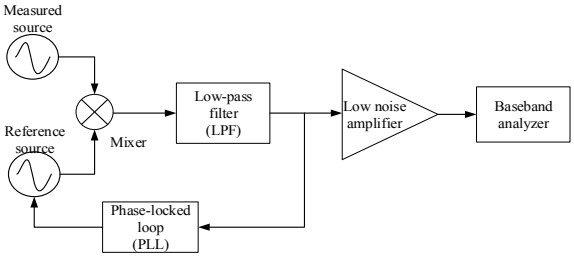


Fig. 1. Loose phase locking method in traditional phase noise measurement.

Its purpose is to realize that the two comparison signals can be completed in phase quadrature，use the reference signal and the measured signal to achieve phase quadrature control after mutual locking and then through phase information sampling, algorithm processing to get the single-sideband phase noise curve. However, the equipment is complicated and expensive, and the operation is also complicated. The response time sometimes is very long, and the stability of the quadrature lock is affected by big noise changes [1].

The digital linear phase comparison method to be involved in the paper firstly realizes the linear representation of the phase change, from 0 to 360 degrees, of the measured signal; achieves the phase noise measurement through researching the algorithm of single-side band phase noise measurement. Because of the ability to measure transient and short-term frequency stability quickly, we are also capable of accomplishing the corresponding measurement between frequency stability in time domain and phase noise in frequency domain.

2. Digital Linear Phase Comparison

The operating condition that the mainstream phase noise measurement system should guarantee, which is the phase quadrature between compared signals can actually be achieved without phase locking. The digital phase comparison DLCP [3-5] between multiple frequency relationships can reflect the natural characteristic that must exist when measured signals in phase quadrature state [5-6]. In digital measurement, when the clock signal frequency is n times (e.g. 10 times) of the measured signal, there will have n relatively stationary sampling clock signals in a period of the measured signal. As Fig. 2 shows, there will always be a clock signal sampling in the phase "quadrature zone" where is at the rising segment and close to the zero phase of the measured signal. In this way, the original full-period phase change of a measured signal converts into n phase difference changes which have 1/n original period and higher sensitivity with an excellent linearity. It is shown in Fig. 3. Whether frequency stability measurement in time domain or phase noise measurement in frequency domain, the phase change rate of the measured signal, $\Delta T/\tau$ ($\Delta f/f = \Delta T/\tau$), is detected and collected, where ΔT is change in phase difference and τ is the time corresponding to phase difference change. From the measurement of phase difference variation, this kind of conversion does not have an influence on phase continuity of signal, which is the variation characteristic of voltage-phase which originally performance in sinusoidal form be converted into an orthogonal representation of n segments.

The phase change from 0 to 360 degrees at lower phase comparison frequency (for example 10 MHZ) is decomposed into several phase changes from 0 to 360 degrees at higher and multiple phase comparison frequencies (for example 100 MHz) with higher resolution. The resolution of the measurement essentially depends on the stability of the AD conversion and its noise characteristics. AD conversion border effects will break through the 100 fs resolution limitation.

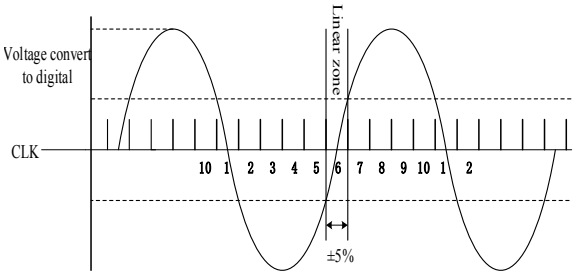


Fig. 2. The digital method of sine waveform linear segment high-frequency clock corresponding to sequence digital phase sampling.

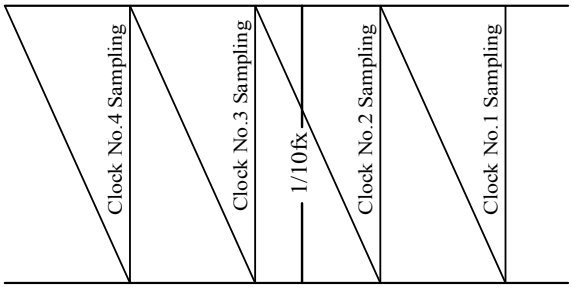


Fig. 3. Phase detection output signal of linear phase processing.

It is undeniable that the current technical indicators in the measurement are affected by the noise of the clock multiplication circuit. Improvement in this area is also one of the keys. Of course, this effect is similar to that of the frequency synthesizer used in the traditional method.

Regarding the problem of the noise effect of the clock signal, several solutions have been proposed. The variety of measured signal frequencies sometimes also provides the simple choice that not required the clock signal frequency doubling. In another aspect, the advantageous combination of multiple references also enables a higher measurement precision with increasing reference and the processing of measured data without doubling frequency, that is, we can avoid the problem of clock frequency doubling. The hardware is not implemented to realize phase-locked frequency doubling, instead, it goes through multiple high-resolution testing sessions, the noise that should be eliminated can be detected and use the software calculating to removing. The way dual AD shares the clock has been experimented with, and it has few effects [6].

The principle block diagram of the system is shown in Fig. 4.

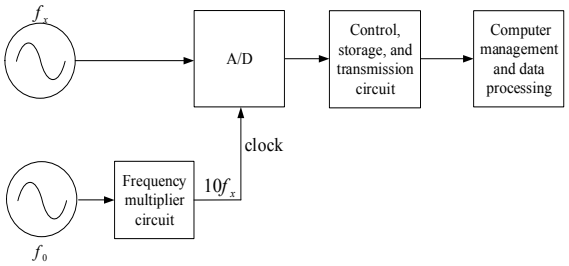


Fig. 4. Principle block diagram of the DLPC system.

The equipment based on the scheme has been conducted to perform a large number of full-frequency stability measurements with different frequency sources, which make sure the transient stability measurement with the carrier period as the shortest sampling time. Therefore, information omitted before can be obtained. The following figures are the results of self-calibration of ultra-high stability crystal oscillator OCXO 8607 (Fig. 5), crystal oscillator measurement (Fig. 6), Cesium clock 5585B measurement (Fig. 7) and DDS output signal's frequency stability (Fig. 8) in full response time.

In the phase comparison process, the relationship between frequency difference and phase difference variations:

$$\frac{\Delta f}{f} = \frac{\Delta T}{\tau} \tag{1}$$

The calculation formula of frequency stability is as follows:

$$\sigma_y(\tau) = \frac{1}{\tau}\sqrt{\sum_{i=1}^{m}\frac{(\Delta T_{i+1} - \Delta T_i)^2}{2m}} \tag{2}$$

For two compared signals, Δf is the frequency difference, f is the nominal frequency, ΔT is the phase difference change and τ is the comparing time.

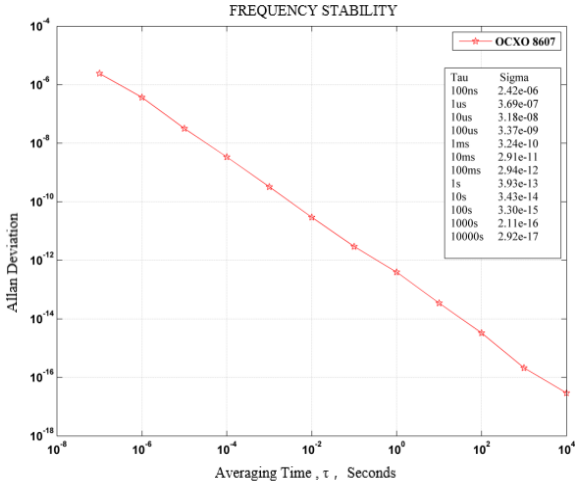


Fig. 5. Self-calibration frequency stability curve of OCXO 8607.

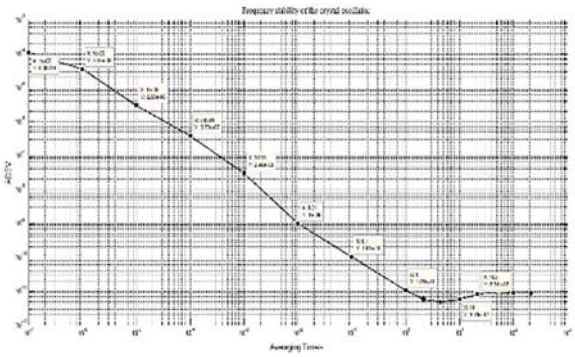


Fig. 6. Frequency stability of crystal oscillator in full response time.

The Cs atomic clock 5585B is compared with the ultra-high stability OCXO 8607, as shown in Fig. 7. The frequency stability of Cs clock 5585B are $<1.2\times10^{-11}$/s and $<8.5\times10^{-12}$/10 s, $<2.7\times10^{-12}$/100 s and $<8.5\times10^{-13}$/1000 s, which is measured by higher lever equipment. The frequency stability measured by the new type are 1.31×10^{-11}/s and 7.63×10^{-12}/10 s, 2.64×10^{-12}/100 s and 7.25×10^{-13}/1000 s, basically consistent with the above. From Fig. 7 it is shown that the frequency stability of Cs clock varies from $1/\tau$ to $1/\sqrt{\tau}$ with the average time changing.

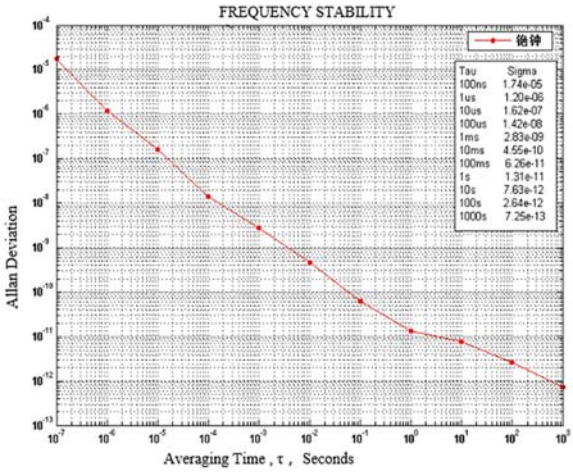


Fig. 7. Frequency stability curve of Cesium clock 5585B.

In Fig. 7, the horizontal axis shows the averaging time in s and the vertical axis the frequency stability, characterized by Allan Deviation.

It can be seen from Fig. 8, compared with high-stability crystal oscillators and atomic clocks, the transient stability of DDS is obviously poorer than the former two, due to the principle of DDS. The main parts of DDS are a phase accumulator and a look-up table. Because its output frequency is determined by searching step length, the spurs are relatively large, making its transient stability worse than crystal oscillators and atomic clocks.

Due to DDS control process of the crystal oscillator adopting phase processing, the frequency stability of DDS in Fig. 8 keeps in the slope of 1/τ with time.

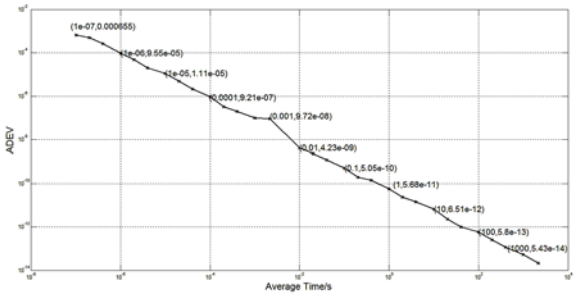


Fig. 8. Full response time frequency stability of DDS.

From the frequency stability of frequency source devices based on crystal oscillator, in full response time, it can be seen that the frequency stabilities of the main transient and short-term show the changing law of 1/τ with the sampling time. This embodies the characteristics of phase-modulated white noise. Comparing with each other, the short-term and the ultra-short-term frequency stability of different types frequency sources also could be known. From Fig. 5, Fig. 6 and other experiments, it can be clearly seen that a high-stability crystal oscillator, without being affected and controlled by other natural reference sources, often owns a changing law of 1/τ within a sampling time less than 1 s. While in longer than 1 s, the low-frequency noise and aging of crystal oscillators will worsen its frequency stability as the sampling time changes.

However, different situation will appear in passive atomic clocks, such as Cs clocks. About the transient frequency stability, we have raised it before a few years [6], but no attention should be paid. Nowadays, with the wide development of the periodic signal parameters measurement, in some measurements related to multiplication factors, especially in the time processing with a signal cycle as a phase step or in the measurement and processing on AC voltage signal, the most obvious effect is the signal's own transient frequency stability.

For the phase noise measurement of a single-frequency component signal, such as a common frequency standard signal, ADC's clock signal can be achieved just by frequency-multiplication. For the phase noise measurement of signals in a wide frequency range, it is necessary to cooperate with a low-noise frequency synthesis instrument used in traditional phase noise measurement systems. According to the measured signal frequency, it need to output a signal equivalent to 10 times frequency of the measured signal.

For the digital measurement of measured signal with higher frequency, it is difficult to always keep at 10 times frequency relation over the measured signal and the clock signal. In the aspect, there are also continuous iteration research, that makes the ADC's clock signal and the measured signal follow a relationship in the least common multiple period [2], to get the linear region of measured signal. In this way, the fastest response time will be shortened, while it also ensures that the clock signal is at a lower frequency and has a certain frequency difference relationship with the measured signal.

3. Time-domain Frequency Stability and Frequency Domain Phase Noise Measurement Based on Phase Information

The new measurement system use ADC as a linear phase discriminator, the phase comparison time can be set flexible with the help of FPGA, extracting the sampling point data in the linear section of the measured signal, the measurement of phase noise from the far carrier frequency to near carrier frequency can be realized. The system is using the spectral estimation algorithm, in order to improve the resolution and reduce the variance, after multiple groups of comparison experiments, the length and coincidence degree of the window are reasonably set. At the same time, to solve the problem of resolution fixed during FFT calculating, the segmentation and splicing of the frequency spectrum are designed, the high resolution and low consumption phase noise measurement is realized.

The 16 bit A/D converter is selected, when the reference voltage is 3.3 V, the quantization resolution can reach 50.35 μV. A 16-bit ADC with a relatively high sampling rate of 105 Msps, the LTC2217 of Yardenow is selected, the analog input range is 2.575VPP, the background noise is 81.3dBFS, the parasitic free dynamic range is 100 dB, and the ultra-low jitter is 85 f_{sRMS} [7].

The block diagram of the phase noise measurement system is shown in Fig. 9.

The working principle of the system is as follows: the frequencies of the system clock and the measured signal are in multiplication relationship, so the nominal frequency of the reference signal could be made the same as the measured, and then multiplied as ADC's clock to sample the measured signal. Using FPGA, the linear region of the sampled signal is judged and the phase difference information is extracted. When the data volume reaches the set value, the data is transmitted to the host computer, through the serial port, for power spectrum estimating and other related processing, and then the phase noise curve and frequency stability are obtained.

The system selects a 16-bit A/D converter. When the reference voltage is 3.3 V, the quantization resolution can reach 50.35 μV, which can meet the measurement requirements in most cases; the 16-bit ADC with a relatively high sampling rate, 105 Msps, is selected. ADC. LTC2217 is a 16-bit A/D converter with a sampling rate of 105 Msps, an analog input

range of 2.75 Vpp, a noise floor of 81.3dBFS, a spurious-free dynamic range of 100 dB and an ultra-low jitter of 85 fs_{RMS}. With excellent noise performance, it is suitable for demanding communication applications.

The FPGA selected in this system is the Spartan-6 series of Xilinx manufacturer. This series provides leading system integration functions, meeting the needs of most users at a lower cost. The series has 13 members, provides an expanding density from 3840 to 147443 logic units, makes its connection faster and more comprehensive, achieves the best balance of cost, power consumption and performance and has been widely used. At the same time, we weigh the relationship between data extraction in linear region, data storage and chip power consumption, the XC6SLX9-2FTG256C chip of the Spartan-6 series is selected. The chip has 256 ports, up to 200 user-available I/O pins, 9152 logic units, and a maximum of 576 kB of Block RAM, which fully meets the system design requirements.

The design flow chart of multiple resolution power spectrum estimation is shown in Fig. 10.

The measurement of phase noise is mainly divided into two modules: phase difference information acquisition and data processing. The data processing module includes the processing of amplitude-phase conversion on the extracted data in the effective linear region, phase difference calculation and removal of gross errors, etc., to obtain the phase fluctuation information, and then, by estimating the power spectrum of the phase fluctuation information, realize the phase noise measurement.

Since the focus of the phase noise measurement is the change trend of the power spectrum curve, for a group of measured data, based on the Welch method, a single data segment average can be used to reduce the variance; at the same time, the appropriate data segment length and data overlap can be selected to perform power spectrum estimation.

In the process of power spectrum estimation, Fourier transform is an indispensable part. Because the FFT operating resolution is fixed, that is, in the result of an FFT operation, the distinguishing capabilities on the power spectrum are the same in the low frequency band and the high frequency band, which will result in waste of resources or low measurement accuracy [8]. For example, suppose that when the spectrum distribution is between 0-10 Hz, a resolution of 1 Hz is required. While, for the spectrum distribution between 100 k-1 MHz, if the resolution is still adopted at 1 Hz, more points will be required and the calculation speed will be slower, resulting in resources waste. However, factually there is no need to using such a high resolution at this stage. In order to balance the pros and cons of the FFT points and the resolution, we have adopted a method of segmenting the measuring frequency range. For different frequency bands, select different sampling frequencies to achieve its power spectrum estimation.

In this system, the phase difference data sampled by the ADC is extracted through FPGA in the linear region with the phase comparison time as the interval, and stored in FPGA. When the data quantity reaching the default value, the data will be transmitted to computer through serial ports, saved and processed by MATLAB software, to obtain its power spectrum distribution curve.

If the number of data points involved in the FFT operation is 2048, the frequency spectrum segmentation is shown as Table 1.

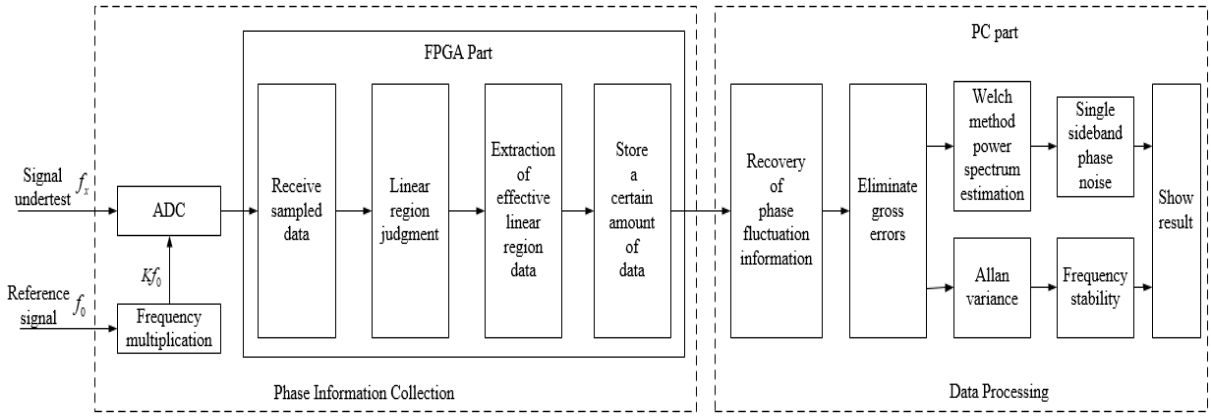


Fig. 9. System overall block diagram.

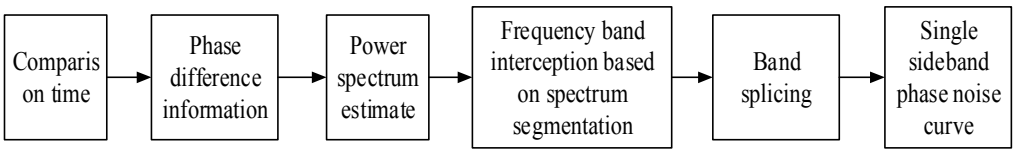


Fig. 10. Procedure diagram of the multi-resolution power spectrum.

Table 1. Spectrum segmentation situation.

Number of paragraph	Phase comparison time	Actual sample rate /Hz	Analysis bandwidth /Hz	Intercept frequency band /Hz	FFT points	Resolution /Hz
1	100 ns	10 M	0~5 M	100 k~1 M	2048	5k
2	1 μs	1 M	0~500 k	10 k~100 k	2048	500
3	10 μs	100 k	0~50 k	1 k~10 k	2048	50
4	100 μs	10 k	0~5 k	100~1 k	2048	5
5	1 ms	1 k	0~500	10~100	2048	0.5
6	10 ms	100	0~50	0~10	2048	0.05

By setting the phase comparing time, the segment processing of the spectrum can be realized. In the first segment, the bandwidth is 0~5 MHz and the frequency resolution is 5 kHz, which is the farthest band away from the carrier frequency, known as the far carrier frequency. Generally speaking, 5 kHz could almost meet the most frequency resolution requirements. In the sixth segment, the bandwidth is 0~50 Hz, and the frequency resolution is 0.05 Hz, which is the closest band the carrier frequency, also called as the near carrier frequency. This resolution can also meet the requirements of near carrier frequency. The division of frequency bands has satisfied the resolution requirements of the entire measurement range.

For the processing of spectrum splicing, when the number of FFT points is 2048, the number of points of the obtained single-sideband power spectrum result is 1024. Between [0, 10 Hz], a frequency band, it can be seen from $f_n=f_s \cdot n/N$ that [0, 1024], the number of points, represents [0, 50 Hz], the frequency range. Herein, the 205th point just is about 10 Hz, then [0, 205] represents [0, 10 Hz]. The point [206, 1024] represents the frequency range (10 Hz, 50 Hz], which belongs to the next frequency band and in which all points are discarded.

In [10 Hz, 100 Hz], the points number of [0, 1024] represents the frequency range [0, 500 Hz], in which [0, 20) represents approximately [0, 10 Hz). Because the above frequency band has been already analyzed on power spectrum, the points in the interval [0, 20) are discarded. The 205th point is about at 100 Hz, so the frequency range [10 Hz, 100 Hz]represents the point [20, 205]; the remaining points is corresponding to the next frequency band, so the points in the interval [206, 1024] are discarded.

In the same way, in [100 Hz, 1 kHz], the selected point interval is [20, 205]; in [1 kHz, 10 kHz], the point interval is [20, 205]; in [10 kHz, 100 kHz], the point interval is [20, 205]; in [100 kHz, 1 MHz], the point interval is [20, 205]. By splicing the spectrums obtained above, the power spectrum curve of the entire interval can be obtained.

If the spectrum segmentation is not used in the power spectrum estimation, let the phase comparison time to be 10 ms, to extract the data of the linear region of the measured signal with the analysis bandwidth of [0, 50 Hz]. The length of the window function is 512, and thus the frequency resolution is about 0.2 Hz. If such a high resolution is still adopted, for the high frequency band above 1 MHz, that at least 5×10^7 points are required, which will lead to too large calculation. However, according to the high frequency band, it is completely unnecessary to use such a high resolution. Therefore, spectrum segmentation method can solve the problem of fixed resolution for frequency spectrum estimation.

According to the multi-resolution power spectrum method proposed above, for the data of the phase difference in the linear region extracted by digital phase processing in this system, the single sideband phase noise curve is shown in Fig. 6, obtained by using Welch method and Hamming window to estimate the power spectrum. The figure reveals that different resolution could be able to obtained for different frequency bands. The method not only meets the resolution requirements, but also, to a certain extent, saves resources and improves the calculation rate.

When the Welch method [8] be adopted to do the multi-resolution power spectrum estimation, for the phase data that sampling point number nfft=2048, set the length of Hamming window as 512 and the degree of overlapping is 50 % to do the measurement about single sideband phase noise.

4. Phase Noise Measurement and Processing Algorithm and Experiment

In order to evaluate the functions and technical index of the novel phase noise measurement system, the comprehensive experiments and measurements are conducted, including the self-calibration experiment of the high-stability OCXO, the phase noise measurement of the rubidium atomic clock as the measured frequency source, and the full-frequency stability measurement. Through the above experiments, both the technical index and the correlation between the indexes of frequency stability and phase noise can be obtained at the same time, helpful to fully grasp the phase noise of the measured signal.

The final test results are shown in figures below. Among them, Fig. 11 is the result of mutual comparison of measuring the oscillator's own frequency by using the ultra-high stability crystal oscillator 8607 as a reference and frequency doubling to generate a clock signal.

The self-calibration experiment, shown in Fig. 12, is conducted using the 10 MHz output of OCXO 8607, one of that as the measured signal, and the other put into a signal generator, SMB100A, as the external reference to generate a frequency multiplied signal, which is the clock of ADC. FPGA is utilized to flexibly set the phase comparison time and sample the measured signal. The extracted phase difference data is transmitted to the host computer through the serial debugging assistant, and then made use of to estimate the power spectrum; at the same time, the phase difference data also is calculated to get the Allan variance, realizing the measurement of the full frequency stability.

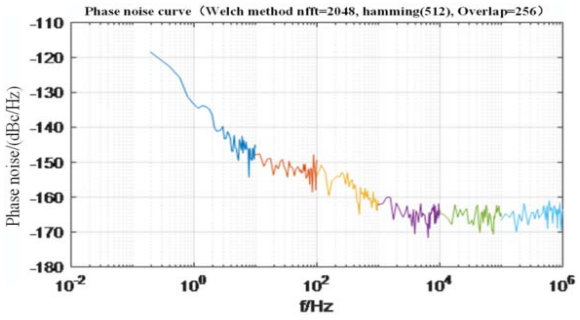


Fig. 11. Self-calibration stability and phase noise of 8607 crystal oscillator.

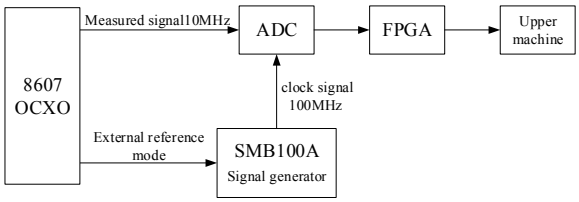


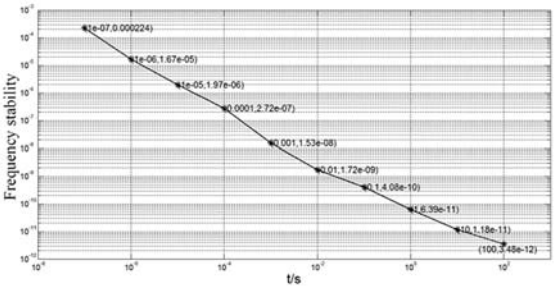
Fig. 12. Block diagram of self calibration experiment of the measurement system.

In the case of self-calibration of OCXO 8607 based on the new designed system, the frequency stability of 100 ns is 2.94×10^{-6}, the frequency stability of 1 s is 4.11×10^{-13}; while the frequency stability of 1 s by 3120A, the current internationally popular instrument, is 2.82×10^{-13}. Although there is still a certain gap between the method and 3120A in the short-term stability index, it cannot be ignored that the measurement range of the new method is much larger than 3120A, and has reached the whole range. Comparing to other measurement methods in the world, the method has significant advantages.

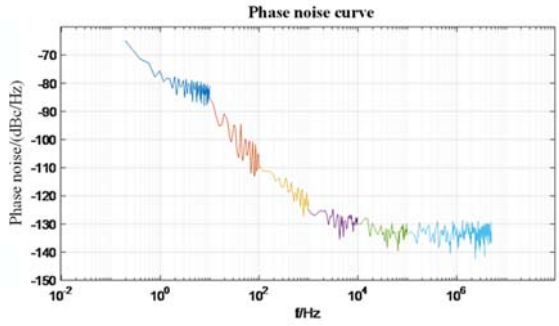
Fig. 13 shows the frequency stability (a) and phase noise (b) of a rubidium clock measured by this system.

The frequency stability measured here is the stability index, on the whole time range, of the rubidium atomic clock under test. The sampling time shown in Fig. 13(a) can range from the carrier frequency cycle of the signal under test, 100 ns, to more than 10 s, factually up to an unlimited time. Therefore, there is a one-to-one correspondence between the sampling time of frequency stability and the frequency deviation from the carrier frequency of the phase noise measurement, shown as Table 1. The correspondence has never been available before in any existing technologies. The frequency stability of a rubidium atomic clock changes with $1/\tau$ to $1/\tau^{1/2}$ variation to reflect the transformation from white noise of phase modulation to white noise of frequency modulation controlled by the atomic energy level transition [5].

This is not obvious from the phase noise diagram (b).



(a) frequency stability of Rb clock



(b) phase noise of Rb clock

Fig. 13. The frequency stability (a), and phase noise (b) of a rubidium clock measured by this system.

Table 2 shows the comparison between the measurement results of rubidium atomic clock using the system introduced in this paper and PN8010 system produced in France.

Table 2. The comparison of rubidium atomic clock phase noise measurement results.

Frequency offset (Hz)	PN8010 (dBc/Hz)	Our system (dBc/Hz)
1	-70.2	-75.5
10	-82.6	-83.7
100	-111.3	-109.6
1 k	-126.8	-123.9
10 k	-134.5	-130.9
100 k	-136.4	-133.2
1 M	-138.3	-135.9

Errors in the phase noise measurement system designed in the paper mainly includes ADC sampling error, clock jitter error, sampling point selection error and frequency multiplication error.

1) ADC sampling error.

In the digital measurement system, due to the limitation of ADC's quantization bits, it is inevitable that there is quantization errors in the measurement process. Here, under the condition of ensuring the sampling rate, LTC2217, an analog-to-digital converter, with a quantization bit of 16 bits is selected to meet the measurement requirements, considering the influence of the main parameters, such as signal-to-noise ratio, differential nonlinearity, integral nonlinearity, etc. the quantization error is as small as possible. Regarding the suppression of digital quantization errors, some new processing methods have been constantly tested, and better results will be obtained.

2) Clock jitter error.

In the process of ADC sampling, the clock signal is a time basis of the measurement system. The sample process is seemed as the multiplication of the measured signal and the clock signal in the time domain or the convolution in the frequency domain. Therefore, the frequency spectrum of the measured signal will be mixed with the frequency components of the clock signal, which appears as the measured signal's spectrum deviation from the sampling clock. It will cause the spectrum of the signal under test to be no longer pure, increasing the spectral line width and affecting the signal-to-noise ratio of ADC sampling (*SNR*).

3) Sampling point selection error in linear region.

In this measurement system, the measured signal is a sine signal. The slope of tangent line at each phase point of the sine signal is different, so that every quantization fuzzy area produced in the quantization process is also inconsistent. In the vicinity near zero phase point, that is, the linearization area of the phase change, the slope at the tangent point and the step value generated in the unit time are maximum, while the sensitivity relatively larger and the measurement error smaller. For two signals with K times multiplication, when sampling the measured signal by the digital linear phase comparison method, it will be sampled as K equispaced points in one cycle, taken $1/K$ out of the full-period near the positive zero-crossing point as the linear region. Obviously, one of the sampling points must fall within the linear region of the signal under test. As shown in Fig. 9, theoretically the larger K, the narrower the linear region and the closer to the positive zero-crossing point the position, the better the linearity, the greater the tangent slope, and the more accurate the measurement. However, the maximum sampling rate of LTC2217 limits K. In this measurement system, for the measured signal of 10 MHz, the maximum is up to K=10, so the linear region is 36°. If the sampling rate is higher, raising Kcan further reduce errors caused by the sampling points selection.

4) Frequency multiplication error.

In this measurement system, the clock signal of ADC is a 100 MHz sinusoidal signal that is multiplied from the reference signal by SMB100A. The noise of RF signal generator will inevitably be introduced into the measurement system during the conversion, which reduce the measurement accuracy. If OCXO 8607 is self-calibrated by directly phase-shifting without a frequency multiplier, the frequency stability of the self-calibration will reach 1×10^{-13}/s. Therefore, further improvements can be developed from this aspect.

5. Conclusion

In the research about single sideband phase noise measurement, there are some digital methods successfully [9-11]. Here our method is simpler and easy to combine with traditional technology. We use the digital linear phase comparison method to solve the problem that phase quadrature and abstract the phase change information can only be achieved by means of phase mutual locking in the traditional system. The function of this link simplifies the system, avoids the trouble caused by losing lock, improves the working efficiency, explains the differences in indicators between different frequency sources.

The linear segment (digital mode) which naturally exists in signal (sinusoidal) waveform can be effectively utilized to obtain satisfactory linearity. Due to limited of the phase variation region of the excellent linear segment under the condition of frequency relation multiplying, starting from the average frequency deviation $\Delta f/f = \Delta T/\tau$ relationship and frequency stability, this will not affect the measurement of the phase difference variation, frequency, and frequency stability. With the deepening of research, other technologies suitable for extracting phase orthogonal information in a wider frequency range will be developed, which is suitable for the wide application of commercial phase noise measurement system.

Acknowledgements

Supported by National Natural Science Foundation of China under No. 11773022 and 1187 3039.

References

[1]. D. L. Yan, Development of phase noise measurement technology, *Aerospace Measurement Technology*, Vol. 26, Issue 5, 2006, pp. 59-61.

[2]. W. Zhou, X. Ou, H. Zhou, The time frequency measurement and control technology, *Xidian University Press*, 2006.

[3]. A digital phase shift aided linear phase comparison method, *Patent 201910243834.*

[4]. A linear phase comparison method based on direct digital phase processing, *Patent 201910243847.5*.
[5]. W. Zhou, Z. Li, W. Qiao, The most potential technology in time frequency domain-Digital linear phase comparison, in *Proceedings of the China Conference on Time and Frequency (CTFS'2019)*, 2019.
[6]. Z. Wei, Z. Li, L. Bai, *et al*., Generalized phase measurement and processing with application in time-frequency measurement control and link, in *Proceedings of the 2013 Joint European Frequency and Time Forum and IEEE International Frequency Control Symposium*, 2013, pp. 429 - 433.
[7]. http://www.bdtic.com/en/linear/LTC2217.
[8]. Q. Ren, Y. Yu, Application of Welch power spectrum estimation algorithm in phase noise measurement, *Automation Instrument*, Vol. 35, Issue 1, 2014, pp. 19-21.
[9]. Allan Ecker, A Digital Method for Phase Noise Measurement, in *Proceedings of the IEEE International Test Conference (TC)*, Washington, 2012, pp. 1-10.
[10]. H. Gheidi, A. Banai, A New Phase Shifter-less Delay Line Method for Phase Noise Measurement of Microwave Oscillators, in *Proceedings of the IEEE European Microwave Conference*, 2008, pp. 325 - 328.
[11]. T. Imaike, Full digital phase noise measurement by using two reference oscillators and multichannel ADCs, in *Proceedings of the Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium ((EFTF/IFCS)*, 2017, pp. 583 - 586.