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Fast FPGA Implementation of an Original Impedance Analyser

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Abstract: This article describes in detail the design and rapid prototyping of an embedded impedance analyzer. The measurement principle is based on the feedback control of the excitation voltage V_D during a fast frequency sweeping. This function is carried out by a high precision synthesizer whose output resistance R_G is digitally adjustable. Real and imaginary parts of the dipole impedance are determined from R_G and the phase of V_D. The digital architecture design uses the hardware-in-the-loop simulation in which the dipole is modeled using an RLC parallel circuit and a Butterworth Van Dyke structure. All digital functions are implemented on a Stratix II FPGA board with a 100 MHz frequency clock. The parameters taken into account are the frequency range (0 to 5 MHz), speed and resolution of the analysis and the quality factor of the resonant dipole. To reduce the analysis duration, the frequency sweeping rate is adjusted in real time. *Copyright © 2011 IFSA.*

Keywords: Electric impedance, Impedance analyser, FPGA, DDS, Hardware in the loop, Piezo sensor.

1. Introduction

It has been shown that the electric impedance Z of an *in situ* transducer does not only contain interesting information on the transducer itself but also on the medium in which it is immersed (quality of the acoustic coupling, variations of acoustic load, presence of reflexions). Many applications exploit this dependence to design measurement systems: simultaneous measurements of the viscosity and the density of a liquid [1], structural or rheological analysis of a material, estimation of the transfer function of an ultrasonic system emitter/sample/receiver [2]. Lastly, the study of Z in the resonance area makes it possible to detect a dysfunction or a drift of the transducer. In these applications, the main difficulty lies in the estimation of Z(f) in real-time, which is generally done by using an impedance analyzer which is not transportable. These practical considerations have led us to study a method for carrying out an in-line estimation of Z(f) with an embedded system. The design uses mixed co-simulation tools. The transducer and its associated analogical component part are simulated under Matlab SimPower Syst. Internal numerical functions of the system use only the specific blocks of the DSP-Builder library that makes it possible to have a virtual prototype directly implementable on a FPGA circuit. In the first part we outline the proposed method for the estimation of Z(f) and the parameter settings necessary for its use. The second part is devoted to the FPGA implementation of the real-time impedance meter. The simulations were carried out using the Hardware In the Loop (HIL) strategy. In the last part, we test the system in the range 1.8 MHz to 2.8 MHz using two models of resonant circuits.

2. Feedback Controlled Impedance Analyser

2.1. Principle and Structure of the System

To determine the impedance Z(f) of a dipole, it is possible to measure both the voltage and the current which flows through the transducer [3, 4]. However, the disadvantage of this solution is that a current sensor has to be inserted and the voltage/current ratio for each frequency has to be measured. In order to avoid these difficulties, we have chosen a feedback method of measurement [5, 6] which is described in Fig. 1.

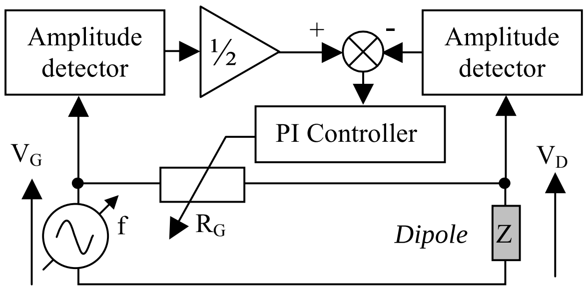


Fig. 1. Principle scheme of the system.

In this system, a sinusoidal voltage generator V_G with an output resistance R_G is used to excite the tested dipole. The generator sweeps the desired frequency band. The voltage V_D applied to the dipole is regulated at constant amplitude whatever the frequency is. For this, the variable resistor R_G is controlled in real time by a proportional-integral controller. The value of R_G and the phase φ between V_G and V_D are used to determine the complex value of Z.

2.2. Optimal Value of the V_D Amplitude

Considering the system of Fig. 1 we can write:

$$V_D = \frac{Z}{Z + R_G} . V_G \ , \tag{1}$$

where Z is the complex value R + jX.

We deduce the amplitude of the voltage V_D:

$$\left|V_D\right| = \frac{|Z|}{\sqrt{|Z|^2 + 2RR_G + R_G^2}} \left|V_G\right| \tag{2}$$

From (1) we can calculate the sensitivity $\frac{dV_D}{dZ}$

$$S = \frac{dV_D}{dZ} = \frac{R_G}{(Z + R_G)^2} V_G \tag{3}$$

This leads to:

$$|S| = \frac{R_G}{(R + R_G)^2 + X^2} \left|V_G\right| \tag{4}$$

$$\frac{|S|}{\left|V_G\right|} \text{ is maximum when } R_G = \sqrt{R^2 + X^2} = |Z| \tag{5}$$

By introducing (4) in equation (2) we get:

$$\left|V_D\right| = \frac{1}{\sqrt{2 + 2\frac{R}{|Z|}}} \left|V_G\right| \tag{6}$$

So the best sensitivity is obtained when the amplitude of V_D is between $\frac{\left|V_G\right|}{2}$ (where Z is purely real) and $\frac{\left|V_G\right|}{\sqrt{2}}$ (where Z is purely imaginary). Reciprocally, when the amplitude of V_D is fixed by feedback control between these limits, then the value of R_G is approximately equal to the module of Z. In our system the amplitude of V_D is stabilized to $\frac{\left|V_G\right|}{2}$. So R_G is exactly equal to $|Z|$ at the resonance and antiresonance frequencies (f_r and f_a) of the dipole.

2.3. R and X Determination

We note the complex amplitudes: $V_G = 1$; $V_D = 0{,}5e^{j\varphi}$.

From (1) and by separating the real and imaginary parts, we obtain the system of equations:

$$\begin{bmatrix} 1 - 0.5\cos(\varphi) & -0.5\sin(\varphi) \\ 0.5\sin(\varphi) & 1 - 0.5\cos(\varphi) \end{bmatrix} \cdot \begin{pmatrix} R \\ X \end{pmatrix} = 0.5 \begin{pmatrix} \cos(\varphi) \\ \sin(\varphi) \end{pmatrix} R_G$$

The elements R and X are calculated according to:

$$R = \frac{0.5\cos(\varphi) - 0.25}{1.25 - \cos(\varphi)} R_G \text{ and } X = \frac{0.5\sin(\varphi)}{1.25 - \cos(\varphi)} R_G \tag{7}$$

The phase φ between V_T and V_G is determined by synchronous detection. R and X are calculated from φ and R_G at each frequency. The complete R-X computing module is represented in Fig. 2.

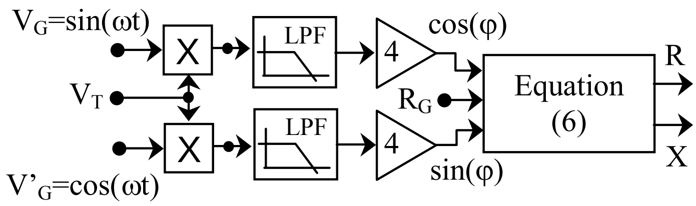


Fig. 2. Synchronous detection and determination of R and X.

With this method, Z is measured with a nominal signal to noise ratio.

2.4. Frequency Sweeping Rate

For a dipole resonant at f_r, the sweeping speed must be adapted to the quality factor Q of the impedance. In the bandwidth $B = \frac{f_r}{Q}$, the maximal sweeping speed v_{max} corresponds to a shift equal to B during the signal settling time τ through the transducer. To obtain amplitude error lower than 1 %, τ must be greater than $\frac{4}{B}$. So, the speed of the sweeping must respect the following condition:

$$v < v_{max} = \frac{B^2}{4} \tag{8}$$

With the speed v_{max}, the analysis duration in the frequency range [f_{01} to f_{02}] equals to:

$$D_{min} = \frac{4Q^2(f_{02} - f_{01})}{f_r^2} \tag{9}$$

3. Modeling and Implementation

3.1. General Architecture

3.1.1. Overview

The general architecture of the system is represented in Fig. 3 [7]. All digital functions are implemented on FPGA circuits. The analog functions concern the transducer and the variable resistor.

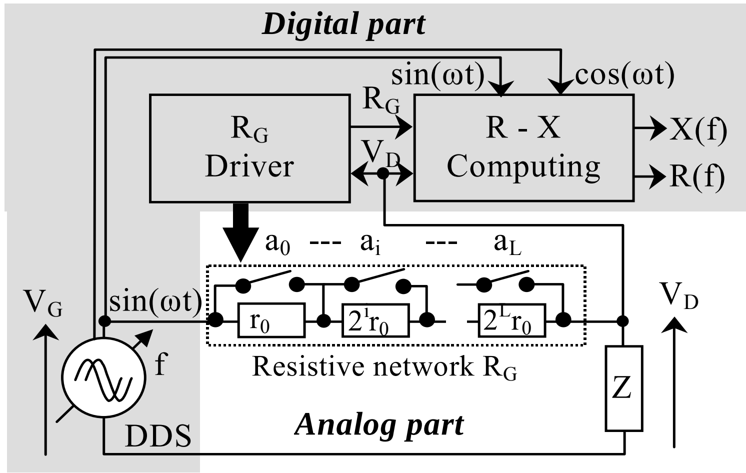


Fig. 3. System architecture.

3.1.2. Numerically Programmable Resistive Network

The resistance R_G takes the form of a serial resistive network which comprises L by-passable resistances. The resistance values are in power of two.

With this configuration, the total resistance of the network is :

$$R_G = r_0 \sum_{i=0}^{L} a_i 2^i \tag{10}$$

Thus R_G can be regulated from 0 to $(2^{L+1}-1)R$.

3.2. Development Environment

3.2.1. Hardware in the Loop Simulation

The originality of this work concerns the design of the feedback system composed of mixed elements. In order to accelerate the development, we have used hardware in the loop (HIL) simulation [8]. This design method allows to test in real time the FPGA architecture in a virtual environment in which the analog components are modeled [11]. This is why we jointly use several simulation tools [9].

The main goal of the HIL simulation is to permit the verification of the digital hardware design with stimuli provided by a discretized model of the real environment. This can notably speed-up the design process [10, 11]. This one can begin even if its sensors and actuators are not available.

In a first time, we can verify the design of the control algorithm and architecture with a pure software model and we can choose the best controller and fine-tune its numerical parameters.

The next step is to refine the model of the digital part by using only synthesizable modules coming either from a library provided by the FPGA manufacturer or a custom library designed by means of an HDL description (VHDL or Verilog) [12, 13]. Currently such modules process only fixed-point data, thus an optimization work must be done here to find the best suited fixed-point arithmetic format in each portion of the design. We have then a reference model for assessing the error introduced by the fixed-point refinement.

Now we have to generate the bitstream that is needed for configuring the FPGA with the digital part of the system under design. The benefit of the HIL environment is that the communication interface with the PC that is running a software model of the simulated environment is automatically added.

The last step is to test the FPGA with real analog interfaces (ADC, DAC, ...).

3.2.2. Rapid Prototyping Steps

Our design comprises four steps organized according to the diagram of the Fig. 4 [14].

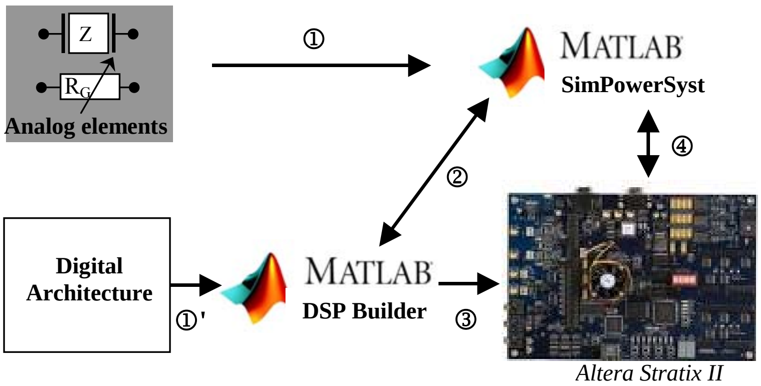


Fig. 4. Steps of design.

- Phase 1. We simulate in floating point under Matlab-SimPowerSystem® the BVD model of the transducer as well as the amplification module and the programmable resistive network.
- Phase 1'. In parallel the numerical functions in fixed point are developed with the Altera-DSP Builder® simulation tools.
- Phase 2. The complete system running is simulated, which enables us to quantify and optimize the whole numerical parameters (registers and signals format, clock rate …).
- Phase 3. The virtual numerical architecture is implemented on a FPGA board.
- Phase 4. The HIL simulation of the generator is then realized. We test its real performances by varying the nature and the type of the modeled transducer.

All the numerical functions are implemented in an Altera Stratix II development board. The card is composed of a 100 MHz clock, two ADC/DAC of 125 Msamples/s, 140,000 logic cells, 9 Mbits embedded RAM, 96 DSP Blocks and 8 PLLs.

3.3. FPGA Implementation of the Digital Part

3.3.1. Numerical Controlled Synthesizer

The sinusoidal generator with a sweeping frequency [13] has a DDS structure which is shown in Fig. 5. The clock frequency is fixed to f_s = 100 MHz.

The first adder provides an integer value N from N_1 to N_2. Each increment of N takes M clock periods (T_s). N is coded on q bits and the second adder has a p-bit format. The r most significant bits address the look up table (LUT) previously loaded with the samples of a sine period.

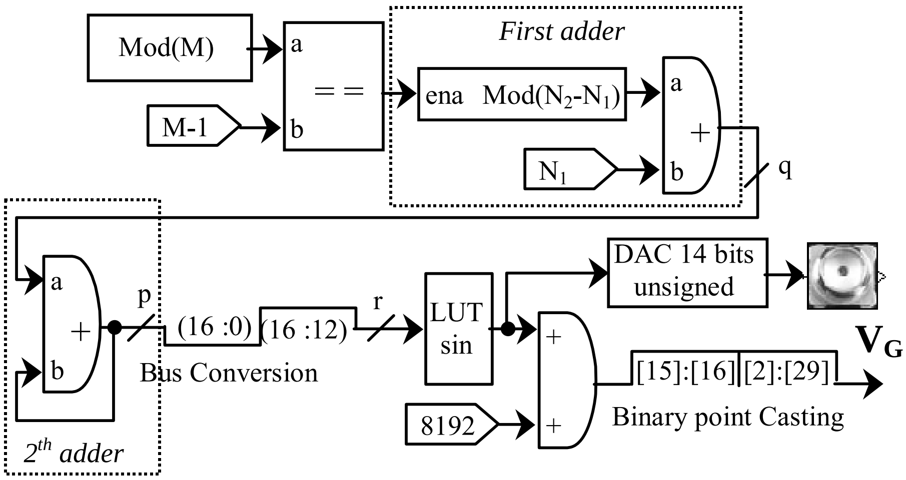


Fig. 5. DDS DSP Builder diagram.

In order to provide a voltage to the resistive network we used the 12 bits DAC of the FPGA prototyping board. It is for this reason that the LUT with 2^r addresses is filled with the values corresponding to the following relation:

$$LUT(k) = round\left[2047 \cdot \sin\left(k\frac{2\pi}{2^r}\right) + 2047\right];\ k = 0, 1, \cdots, 2^r - 1 \tag{11}$$

The fundamental frequency of the output signal is:

$$f_0 = \frac{N}{2^p} f_s \tag{12}$$

We note N_1 and N_2, the parameters which impose the limits f_{01} and f_{02} of the analysis range. They are determined by (12).

The duration between two increments of N equals $d = MT_s$ and the total duration of the sweeping is:

$$D = M(N_2 - N_1)T_s \tag{13}$$

In order to satisfy (8) we must choose:

$$M > M_{min} = \frac{4Q^2}{2^p}\frac{f_s^2}{f_r^2} \tag{14}$$

3.3.2. R_G Driver

The voltage V_D is quantified by a 12 bits ADC and then transmitted to the amplitude detector stage composed of an absolute value operator and a 1st order low-pass filter (Fig. 6).

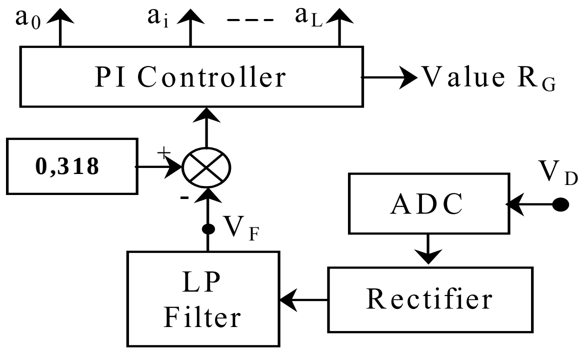


Fig. 6. R_G Controller diagram.

The average value of a rectified unit sinus equals to $\frac{2}{\pi}$. So the output of the rectifier-filter V_F is compared to $\frac{V_G}{\pi} = 0{,}318$. The PI controller delivers the L bits (a_i) of the resistive network.

3.3.3. DSP Builder Model of the Rectifier and LP Filter

The LP digital filter is obtained by bilinear transform of the first order analog function $H_{LP}(p) = \frac{1}{1+\tau_1 p}$. The constant τ_1 respect the condition $\frac{1}{2\pi\tau_1} < \frac{f_{01}}{100}$ to obtain a low ripple voltage. The LP digital filter is described by the transfer function:

$$H_{LP}(z) = \frac{a_1(1+z^{-1})}{1-b_1 z^{-1}} \tag{15}$$

The algorithm is implemented as an entirely parallel IIR direct structure (Fig. 7). The coefficients a_1 and b_1 are coded on 12 bits

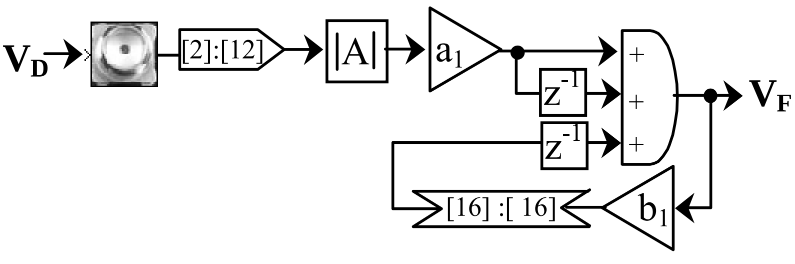


Fig. 7. LP digital filter DSP Builder diagram.

3.3.4. Proportional-integral Controller

The digital PI controller is obtained by bilinear transform of the analog transfer function $H_{PI}(p) = \frac{1+\tau_2 p}{\tau_3 p}$. In order to compensate the delay generated by the LP filter τ_2 is equal to τ_1

The value of τ_3 is the result of a compromise between the rapidity and the stability of the system.

The transfer function of the PI controller has the form:

$$H_{PI}(z) = \frac{a_2 + a_3 z^{-1}}{1 - z^{-1}} \tag{16}$$

We implemented the controller algorithm in an entirely parallel direct IIR structure (Fig. 8) with a 12 bits coding of the coefficients a_2 and a_3 [8][9].

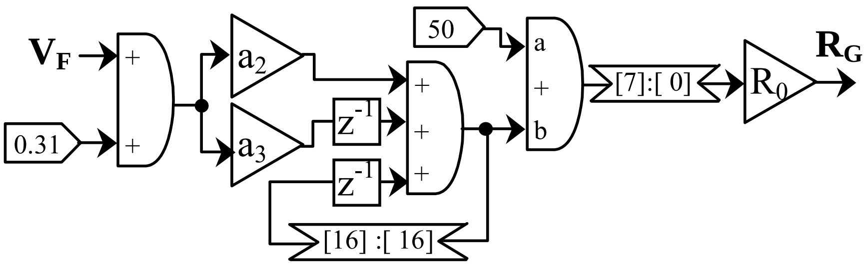


Fig. 8. PI Controller DSP Builder diagram.

3.3.5. R and X Computing Block

The DSPBuilder diagram of R and X computing is shown in Fig. 9.

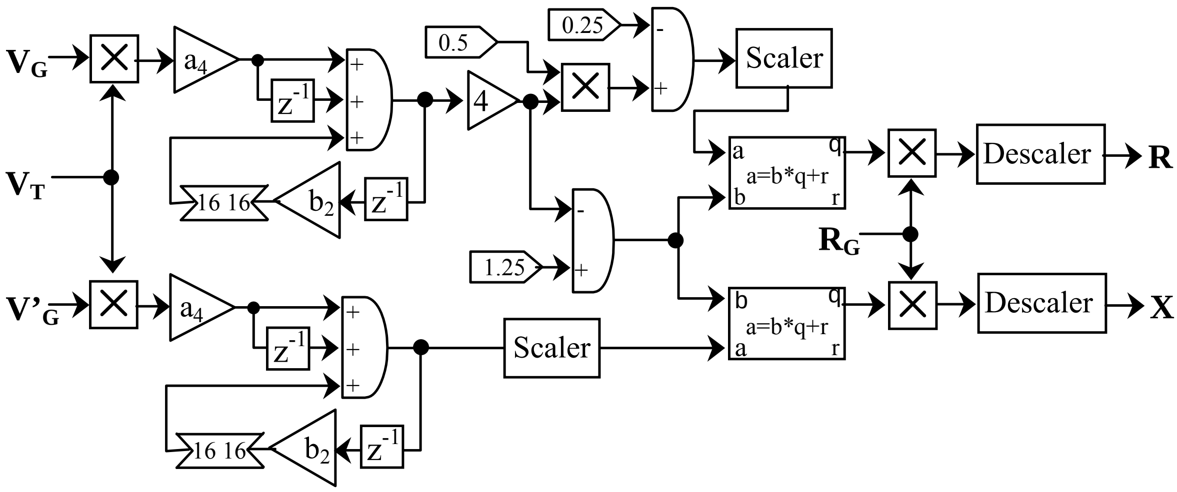


Fig. 9. DSP Builder diagram of the R-X computing block.

3.3.6. FPGA Resources

Table 1 gives the used resources. The maximum working frequency is 102.02 MHz.

Table 1. Resources usage summary.

Combinational ALUTs	Logic registers	Total pins	Memory bits	DSP block 9-bit
496	337	49	448	58

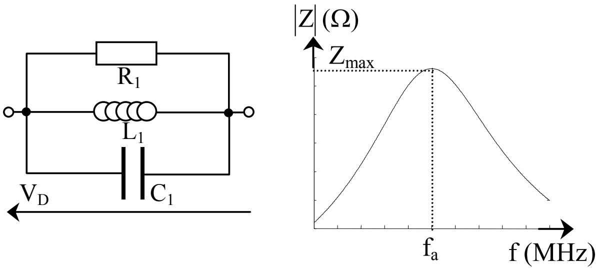
4. Performances

4.1 Experimental conditions

4.1.1 Models of the dipole

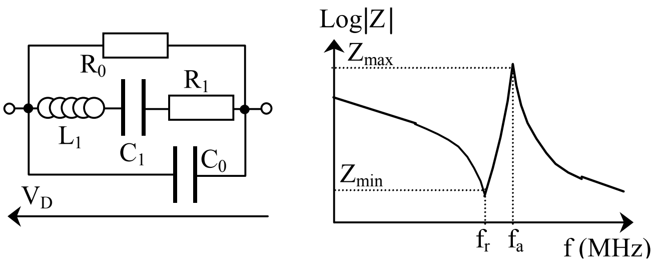
To validate the FPGA architecture we use two different models of a dipole:

- an RLC parallel circuit (Fig. 10),
- a Butterworth Van Dycke structure [16,17,18] modeling a piezoelectric transducer with a quality factor equals to 80 (Fig. 11).



R_1	L_1	C_1	f_a
480 Ω	8 µH	598.54 pF	2.3 MHz

Fig. 10. RLC parallel circuit.



R_1	L_1	C_1	R_0	C_0	f_r
1.22 Ω	8.68 µH	715 pF	1.85 kΩ	3.02 nF	2 MHz

Fig. 11. BVD structure.

4.1.2. Analysis Parameters

- The frequency range is placed between f_{01} = 1.8 MHz (N_1 = 2359) and f_{02} = 2.8 MHz (N_2 = 3670) in order to cover the resonance area of the dipoles.
- The resistive network is controlled by 8 bits data. r_0 is fixed to 5 Ω for the RLC circuit and to 1.5 Ω for the BVD model.
- The binary format p of the adder is fixed to 17 bits. According to (12), this value ensures that the synthesizer has a very narrow frequency resolution (763 Hz).
- For the BVD model, the condition (8) imposes a sweeping speed lower than 156 MHz/s. We have chosen 100 MHz/s, which corresponds to an analysis duration (D) of 10 ms.
- M is fixed at the value equal to 763 in accordance with (13).

The LP filter and controller coefficients are shown in Table 2.

Table 2. LP filter and controller coefficients.

a_1	a_2	a_3	b_1	a_4	b_2
100	-99.75	0.00125	0.9975	0.0004998	0.999

4.2. Results

4.2.1. DDS Output

The signals delivered by the DDS at f_{01} and f_{02} are represented in Fig. 12.

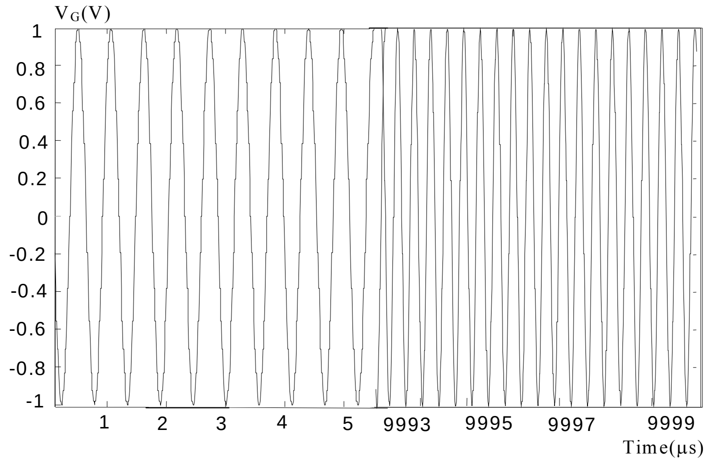


Fig. 12. DDS output signal (start f_{01} = 1,8 MHz ; stop f_{02} = 2,8 MHz).

4.2.2. Test with the RLC Circuit

Fig. 13 and 14 give the theoretical and measured impedance for real and imaginary parts. On these figures, we can note the perfect concordance between the curves of R_G and the impedance modulus $|Z|$ at the resonance frequency 2.3 MHz.

4.2.3. Test with the BVD Model

In our study the electrical behavior of a piezoelectric transducer in a single mode of vibration is described by the traditional Butterworth van Dycke (BVD) structure, in which the influence of the propagation medium is taken into account by the resistive elements [10-12]. $R_G(f)$ and the impedance modulus $|Z(f)|$ are represented in Fig. 15.

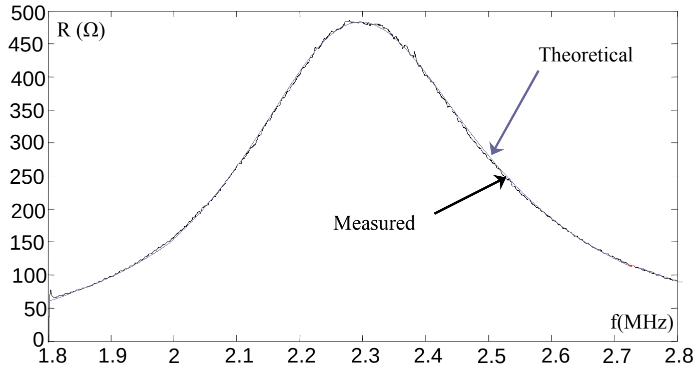


Fig. 13. The impedance real part of the RLC circuit.

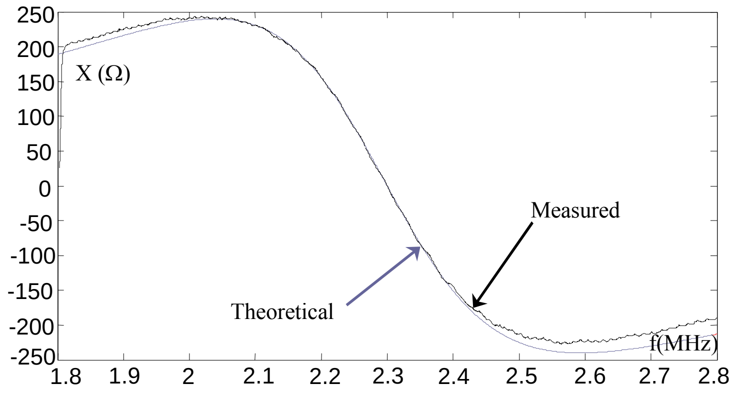


Fig. 14. The impedance imaginary part of the RLC circuit.

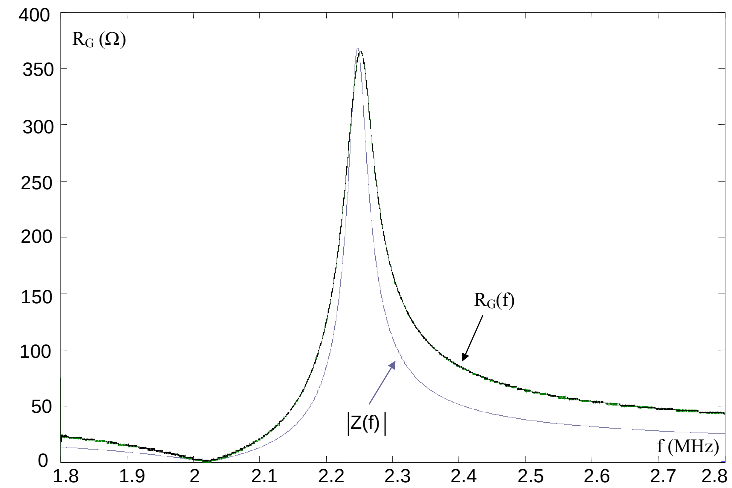


Fig. 15. Electric impedance estimation.

Out of the resonance area, the transducer is capacitive and his impedance is purely imaginary.

In this case, (13) give $V_T = \frac{|X|}{\sqrt{R_G^2 + X^2}} V_G$. The feedback output provides $R_G = \sqrt{3}X$. Therefore $R_G(f)$ is superior to $|Z(f)|$.

4.2.4. Stability of Regulation

The feedback voltage V_F deviates little from the set point amplitude as shown in Fig. 16.

4.3. Reduction of the Analysis Duration

In the previous tests, the sweeping speed is fixed and the analysis duration equals to 10 ms. We can reduce this time by increasing the sweeping speed when the variations of R_G are slow (out of a resonance area for example) [9]. We can carry out this by using a variable parameter M proportional to the R_G variations. The implemented adaptive algorithm corresponds to the following equation:

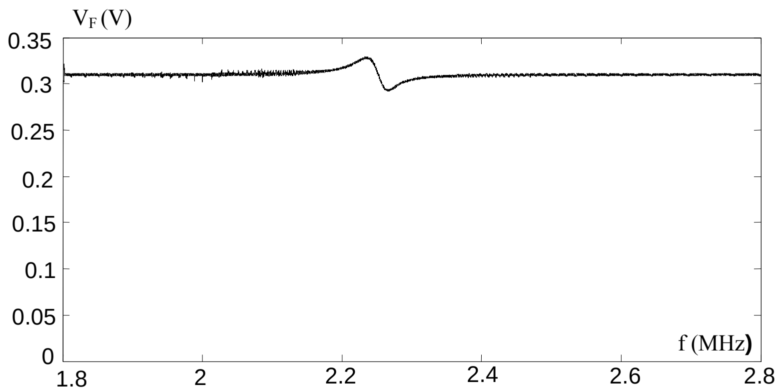


Fig. 16. Variation of the feedback voltage V_F during the spectral analysis.

$$M = k_1\left[R_G(k) - R_G(k-1)\right] + k_2 , \tag{17}$$

where k_1 and k_2 are integer. k_2 determines the minimum value of M.

The DSP Builder diagram of this algorithm is described in Fig. 17.

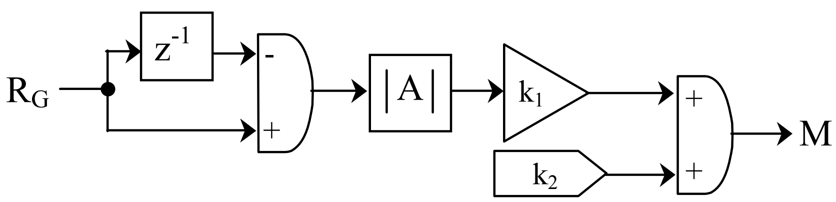


Fig. 17. DSP Builder diagram for M adaptive value.

We have tested the system with k_1 = 150 and k_2 =90. The new duration is reduced to 2 ms.

Fig. 18 represents the R_G curves obtained when M is constant and when M is variable.

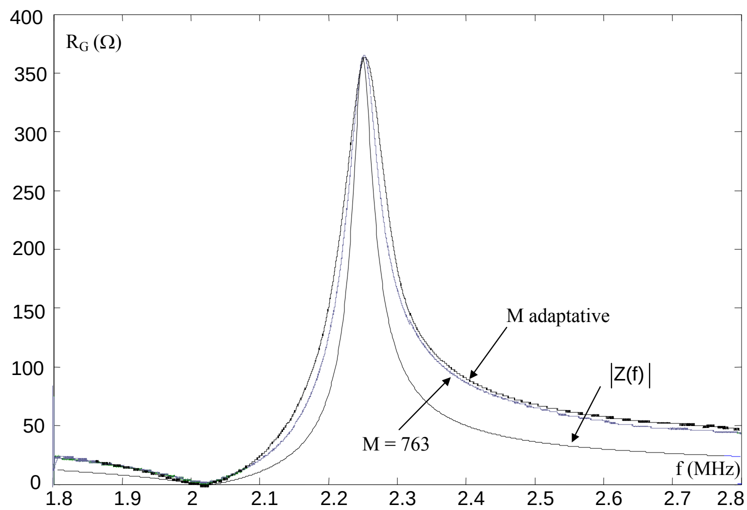


Fig. 18. Electrical impedance estimation for M constant and adaptive.

The use of an adaptive DDS reduces notably the analysis duration by introducing a very low widening of the resonance area.

5 Conclusion

We have developed and implemented a FPGA circuit with an impedance analyser. The device is designed to estimate in real-time the input complex impedance of piezoelectric sensors or transducers. The method of measurement uses a feedback voltage technique and so it is not necessary to measure the current. The second original feature lies in the hardware in the loop simulation of the system, thereby reducing actually the prototyping time. This design strategy also allows the impedance meter setup and calibration without sensor.

The digital architecture is implemented on an Altera Stratix II Board. Its design is done by using SimPowerSystems and Altera-DSP Builder tools. The range of analysis is managed by a high accuracy DDS synthesizer. In the tests, we configure the system to realize impedance measurements above 1 Ω in the range of 0-5 MHz. The measurement accuracy is 1.5 Ω, the duration of analysis is lower than 10 ms. Finally, this architecture is very flexible for the designer. Frequency zoom functions or automatic detection of the resonance can be added. It is also possible to make adaptive the DDS in order to optimize the sweeping rate according to the variations of impedance. The applications of our work concern the conditioning of a sensor array, the monitoring of the propagation medium, the transducer diagnosis... We are currently investigating the integration of the Redwood model [19] or electomechanical model of the sensor using the HIL approach.

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