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A New Wide Frequency Band Capacitance Transducer with Application to Measuring Metal Fill Time

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Abstract: A novel low cost, high frequency circuit for measuring capacitance is proposed in this paper. This new capacitance measuring circuit is able to measure small coupling capacitance variations with high stray-immunity. Hence, it could be used in many potential applications such as measuring the metal fill time in the Lost Foam Casting (LFC) process and Electrical Capacitive Tomography (ECT) system. The proposed circuit is based on differential charging/discharging method using current feedback amplifier and a synchronous demodulation stage. The circuit has a wide high frequency operating range with zero phase shift; hence multiple circuits can work at different frequencies simultaneously to measure the capacitance. The non-ideal characteristic of the circuit has been analyzed and the results verified through LTSpice simulation. Results from the tests on a prototype and a simulation elucidate the practicality of the proposed circuit. *Copyright © 2009 IFSA.*

Keywords: Capacitance measurement, Stray-immune, Circuit analysis, Metal fill time.

1. Introduction

Capacitive sensors are widely used in various industry applications such as those that measure the speed and position of moving objects [1-3], liquid level, flow, pressure, filling time, dielectric properties characterization, and industrial monitoring processes [4-12]. Usually, these sensors are designed in such a way that the variation of the parameter being measured causes a change in the sensor capacitance. In most of these applications the capacitance variations are very small compared to the standing capacitance values. Another challenge is the stray capacitance which is much higher than the capacitance changes. Therefore, the fundamental objectives of the electronic circuits used for

measuring the capacitance are: high sensitivity to extremely small capacitance variations, stray immunity, fast data capture rate, high linearity, and robustness against external noise sources. Some measurement circuits developed to measure small changes in capacitance in Electric Capacitive Tomography (ECT) applications are comprehensively discussed in [4-5], [10-11]. The current paper presents a new low cost, high resolution, wide operating frequency band, a simple interface to measure very small changes of the capacitance in the presences of large stray capacitances.

The measuring circuit uses a high bandwidth current feedback amplifier to produce an AC voltage proportional to the measured capacitance. Fig. 1 shows the circuit diagram of the capacitance measuring circuit using the current feedback amplifier. A second stage based on a synchronous demodulator, low pass filters and an instrumentation amplifier is used to convert the AC voltage to DC voltage representing the measured capacitance while reducing the effect of external noise.

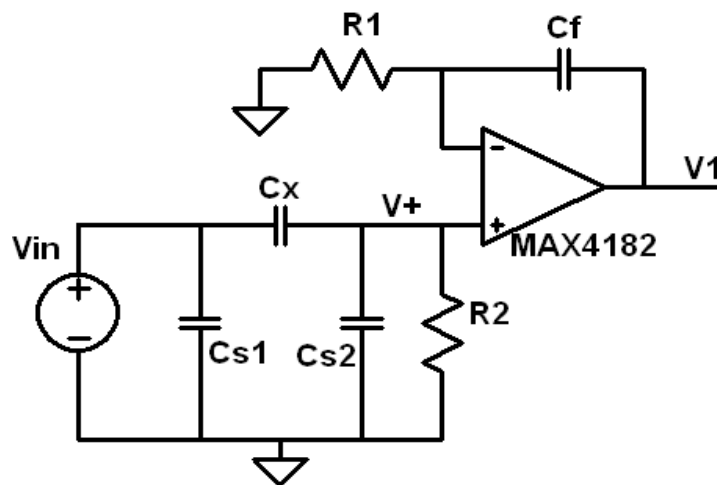


Fig. 1. Schematic diagram of capacitance measuring stage.

The proposed circuit has been developed for the measurement of the metal fill time in the Lost Foam Casting (LFC) application and captures the molten metal characteristics during the casting process [7-8]. A system of such sensors to measure the fill time is a feedback tool to achieve a consistent and controllable process that in turn correlates to improve casting quality.

The proposed circuit can work in a wide range of frequencies which enables the operation of a number of circuits simultaneously each one is operating at a different frequency. The demodulation stage of the circuit is based on synchronous demodulation. Thus, small shifts in the operating frequency among the boards would result in the reduction of the crosstalk and independent operation of the different boards. Using multi-circuits working at different frequencies is especially needed in the metal fill time application to allow the boards to operate simultaneously to precisely measure the fill time. The operating frequency can be selected in the range of (1-10 MHz). This wide range with relatively high frequency allows a high sampling rate of the output voltage while maintaining the noise rejection advantages created by the synchronous demodulation which require averaging over multiple cycles. The capacitance measurement circuit is compact to allow for easy deployment within a casting flask. A wireless version of this circuit is developed using Mote-technology [6] to make the circuit more suitable for use in foundry environment. The non-ideal characteristics of the semiconductor devices used in the circuit are discussed in this paper. The theoretical analysis has been further verified through LTSpice simulation.

The organization of this paper is as follows: Sections 2 and 3 describe the architecture of the capacitance measuring circuit and discuss the methods to overcome the effects of stray capacitances. An accurate analysis of the measuring stage based on the non-ideal characteristics of operational amplifier and the result frequency response of the circuit are presented in Section 4. An application that employs the proposed circuit, namely measurement of metal fill time in lost foam casting, is described in Section 5.

2. Circuit Description

Fig. 2 shows a schematic diagram of the proposed capacitance measurement circuit. This circuit provides high sensitivity to resolve very small capacitance change and has high immunity to the stray capacitances. This circuit consists of two stages: 1. Measuring stage, and 2. Demodulation and amplification stage. The measuring stage consists of square wave generator (V_{in}) working within range of 1-10 MHz, the capacitance to be measured (C_x), two capacitors (C_{s1} , C_{s2}) simulating the stray capacitances, and current feedback operational amplifier MAX4182 working in a wide frequency range.

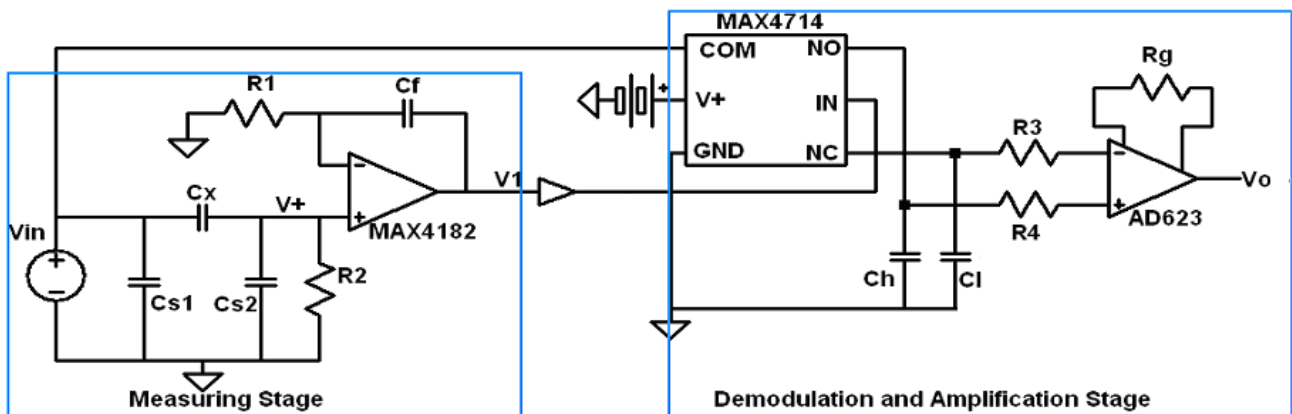


Fig. 2. Schematic diagram of capacitance measurement transducer.

Assuming that the current feedback op-amp is ideal with an infinite gain, infinite input impedance and zero output impedance, the relation between the output of the measuring stage (V_1) and the input (V_{in}) can be described as:

$$\frac{V_1}{V_{in}} = \frac{C_x R_2}{C_f R_1} \frac{1 + s R_1 C_f}{1 + s R_2 (C_{s2} + C_x)} \quad (1)$$

where ($C_{s2} \gg C_x$), equation (1) will be reduced to

$$\frac{V_1}{V_{in}} = \frac{C_x R_2}{C_f R_1} \frac{1 + s R_1 C_f}{1 + s R_2 C_{s2}} \quad (2)$$

To eliminate the stray capacitance effect, angular corner frequencies of the zero $\omega_z = 1/R_1 C_f$ and the pole $\omega_p = 1/R_2 C_{s2}$ should be located far away from the operating frequency range (1-10 MHz) by adjusting the values of parameters R_1 , R_2 , and C_f . A set of possible values is: $R_1 = 10 \Omega$, $R_2 = 10 \Omega$,

$C_f=10$ pF. Stray capacitance is assumed as $C_{s2}=100$ pF. These values result in corner frequencies at $f_z=1$ GHz and $f_p=0.16$ GHz which are very far from the operating frequency range. Therefore, the effect of stray capacitance C_{s2} is diminished and the relationship between voltage V_1 and the measured capacitance C_x is linear as shown (2)

$$V_1 = \frac{C_x R_2}{C_f R_1} V_{in} \quad (3)$$

The values of the resistances R_1 and R_2 are chosen to be equal to reduce the effect of the bias current in both terminals of the op-amp. Since the stray capacitance C_{s1} is driven directly by the excitation source, it does not change the voltage applied on the measured capacitance and thus has no influence on the output voltage.

The measuring stage and demodulation stage are separated by a buffer which is mainly used to drive the capacitive load C_h and C_l and provide a positive offset to voltage V_1 . The offset ensures that the signal is above zero all the time as required by the switch utilized in the current design which accepts only positive inputs.

The second stage in the capacitance measuring circuit is the demodulation and amplification stage. This stage works as a synchronous demodulator stage using a single pole double throw analog switch synchronized to direct the input to one of its two outputs based on the transmitter signal (V_{in}). The signal generated by the measurement stage is running at the same frequency and phase as the synchronization (transmitter) signal. Thus, high level signal passes to one output while the low part of the signal passes to the second output. The capacitor holds that level on each of the outputs as the second output is connected to the measurement stage. Two low pass filters composed of the 'ON' resistance of the multiplexer and one of the two capacitors (C_h, C_l) produce DC signals corresponding to the high and low levels of the output of the measurement stage, respectively. Other signals not synchronized to the transmitter signal produce a common mode voltage on both of the outputs from the analog switch. To remove the effect of the common mode voltage, a low cost instrumentation amplifier AD623 is used in the amplification stage. It amplifies the difference between the two DC levels produced by the low pass filters into the final DC voltage (V_O) that is proportional to the measured capacitance. This is the same principle that allows the operation of multiple boards with slight difference in frequency in the vicinity of each other and is further explained, hereafter.

Assume that two boards are operating at frequencies f_0 and $f_0+\Delta f$. The signal at the output of each of the analog switches will be periodic with a frequency equal to Δf . The two signals at the two switch outputs will have equal DC averages. These two signals are filtered by the low pass filter connected to each output. Selection of the cut off frequency of the low pass filters will determine how small the difference in the operating frequency Δf between the boards can be without much interference between the two boards. A narrow bandwidth of the low pass filters will be effective in reducing interference from other boards operating in the vicinity with close operating frequencies, but will also result in a slower response of the capacitance measurement circuit to changes in the measured capacitance (C_x). Fig. 3 shows a simulated response of the output voltage produced only by interference from a board operating at a frequency $f_0 + 0.1f_0$ ($f_0=1$ MHz). The two signals at the output of the low pass filters have frequencies equal to 100 kHz and are thus slightly filtered by the LPF with cut off frequency less than 100 kHz. As the frequency difference increases the output signal due to the interference signal is further reduced and vice versa.

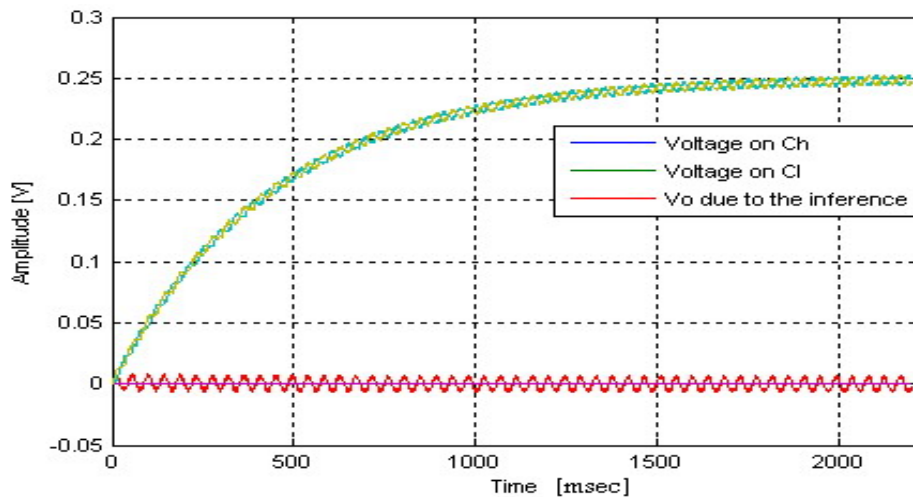


Fig. 3. Output of the demodulation stage for a signal with frequency off by 10 % from transmitter frequency.

3. Stray Capacitance Immunity

The second main advantage achieved by locating the corner frequencies at very high frequency far away from the operating frequency is the elimination of the stray capacitance C_{s2} effect. Equation (3) shows that the output voltage from the measuring stage doesn't depend on the stray capacitance, consequently, there is no effect for the stray capacitance on the output voltage. The other stray capacitance C_{s1} connected between the source and the ground is driven by the excitation source. The current through C_{s1} has no effect on the current through the mutual capacitance C_x assuming the output impedance is negligible. The response of the transducer related to the changes of the stray capacitance has been simulated. The final output has been measured by applying a series of step changes in the stray capacitance C_{s2} . The stray capacitance has been changed in the range of 50 pF to 200 pF with a step of 25 pF, while the measured capacitance is fixed $C_x = 0.35$ pF. The output changes related to the change in the stray capacitance are shown in Fig. 4. When the stray capacitance was changed from 50 pF to 200 pF (maximum value of the stray capacitance), the output changed by 0.42 mV, which implies that the sensitivity of the output of the transducer with respect to the changes of the stray capacitance is negligible compared with the effect of variations in the measured capacitance C_x . The sensitivity to changes in stray capacitance is 2.8×10^7 V/F, while the sensitivity for the measured capacitance is about 2.8×10^{11} V/F [17].

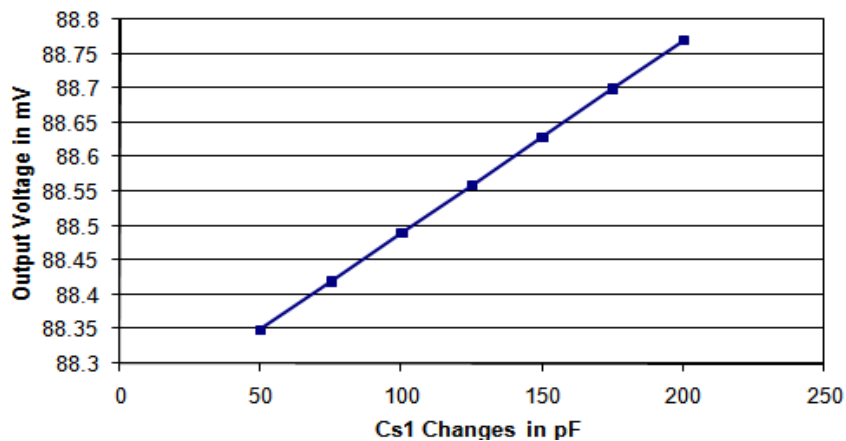


Fig. 4. Final output voltage with changing the stray capacitance.

4. Analysis of the Measuring Stage with Non-Ideal Op-amp

4.1. Frequency Response

Real operational amplifiers do not have the ideal characteristics as assumed in Section 2. The real characteristics of the op-amp are taken into consideration to calculate a more accurate frequency response for the capacitance transducer circuit. To simplify the analysis, the measuring stage shown in Fig. 1 is divided into two sections, the input circuit which is connected to the positive terminal of the op-amp and the current feedback op-amp with the feedback capacitor C_f . The schematic diagram of the equivalent circuit for the current feedback amplifier [16] with feedback is shown in Fig. 5. The non-ideal analysis of the second section is discussed first.

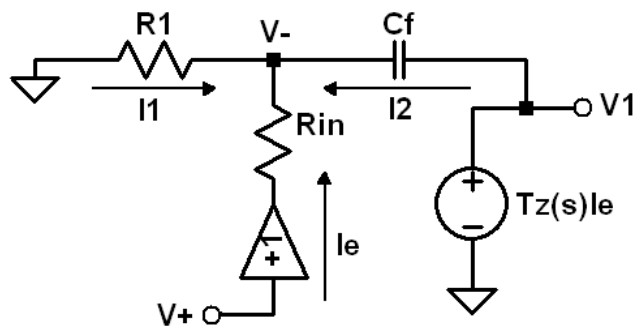


Fig. 5. Non-ideal circuit model of the current feedback amplifier with feedback capacitor.

Ideally the unity gain buffer, between the inputs of the amplifier, causes the non-inverting input impedance to be infinite while the inverting input impedance (R_{in}) to be zero. The buffer allows a current to flow in or out of the inverting input, and the unity gain forces the inverting input to track the non-inverting input. This current is mirrored through the transimpedance and converted to a voltage ($T_z I_e$) at the output [16]. The output is a linear, current-controlled voltage source with zero output impedance. The circuit in Fig. 6 is analyzed as follows:

$$I_1 + I_2 + I_e = 0 \quad (4)$$

$$-\frac{V^-}{R_1} + \frac{V_1 - V^-}{1/sC_f} + \frac{V_1}{T_z(s)} = 0, \quad (5)$$

where V_1 is the output, V^- is the voltage at the inverting terminal and $T_z(s)$ is the frequency dependent transimpedance analogous to the open loop gain in the voltage feedback amplifier.

$$V^- = V^+ - I_e R_{in} = V^+ - \frac{V_1}{T_z(s)} R_{in} \quad (6)$$

After substituting (5) in (4), the closed loop gain of the current feedback circuit is

$$\frac{V_1}{V^+} = \frac{T_z(s)(1 + sC_f R_1)}{sC_f R_1(T_z(s) + R_{in}) + R_{in} + R_1} \quad (7)$$

The transimpedance of the current feedback amplifier can be approximated by:

$$T_z(s) = \frac{T_z}{1 + s / \omega_c} \quad (8)$$

where T_z is the open loop transresistance of the current feedback operational amplifier. The amplifier used here, MAX4182, has a typical value of transresistance equal to $3 \times 10^6 \Omega$ and ω_c is the cut off angular frequency which is dependent on the closed loop gain of the amplifier. The cut-off angular frequency is equal to 10^6 rad/sec at an operating frequency of 1 MHz.

After substituting equations (8) into (7), the closed loop gain of the current feedback op-amp with a feedback capacitor C_f is given by:

$$\frac{V_1}{V^+} = \frac{T_z (1 + sC_f R_1)}{\frac{C_f R_1 R_{in}}{\omega_c} s^2 + \left(\frac{1}{\omega_c} (R_1 + R_{in}) + T_z C_f R_1\right) s + R_1 + R_{in}} \quad (9)$$

Equation 9 shows that the closed loop gain of the feedback current detector of the measuring circuit is characterized by one zero located at angular corner frequency $\omega_z = 1/2\pi C_f R_1$ and two poles at ω_{p1} and ω_{p2} which can be calculated by setting the denominator of equation 9 equal to zero.

The analysis of the input section shown in Fig. 6 is discussed next. The transfer function of the input circuit is obtained by applying a potential divider formed by $R_2 || C_{s2}$ and C_x .

$$\frac{V^+}{V_{in}} = \frac{sC_x R_2}{1 + sR_2(C_{s2} + C_x)} \quad (10)$$

Since ($C_{s2} \gg C_x$) equation 10 can be simplified to

$$\frac{V^+}{V_{in}} = \frac{sC_x R_2}{1 + sR_2 C_{s2}} \quad (11)$$

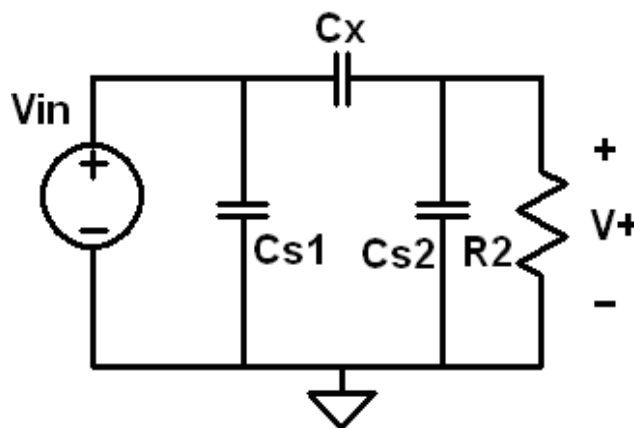


Fig. 6. Circuit diagram of the input section.

The closed loop gain of the measuring circuit is obtained by combining the frequency response of the input and the feedback op-amp circuits. The relation between the output V_1 and the input V_{in} is shown in equation (12).

$$A_{cr}(s) = \frac{V_1}{V_{in}} = T_z C_x R_2 \frac{s(1+sC_f R_1)}{(1+sR_2 C_{s2}) \left(\frac{C_f R_1 R_{in}}{\omega_c} s^2 + \left(\frac{1}{\omega_c} (R_1 + R_{in}) + T_z C_f R_1 \right) s + R_1 + R_{in} \right)} \quad (12)$$

Equation 12 describes the non-ideal closed transfer function of the measuring stage of the capacitance measurement board. As shown in this equation the non-ideal response is characterized by two zeros and three poles. Two of these poles are mainly dependent on the cut off angular frequency ω_c of the op-amp and the feedback capacitor C_f . The other pole depends on the stray capacitance C_{s2} . It may be noticed if the $T_z \rightarrow \infty$,

$$A_{cr} = \frac{C_x R_2}{C_f R_1} \frac{1+sR_1 C_f}{1+sR_2 C_{s2}} \quad (13)$$

4.2. Simulation Results

To verify the theoretical non-ideal analysis, the frequency response of the measuring stage is obtained through circuit simulations using LTSpice. The typical parameters' values have been chosen based on the analysis in Section 2. The values for the feedback capacitor $C_f=10$ pF and the resistor $R_f=10$ Ω are adjusted to eliminate the effect of the zero by locating its corner frequency $f_z = 1/2\pi C_f R_f=1.6$ GHz far from the operating frequency range 1 MHz-10 MHz. The other parameters such as $R_{in}=160$ Ω and the open loop DC gain $A=3 \times 10^6$ are obtained from the MAX4182 op-amp datasheet [15]. The cut-off frequencies of the two poles coming from the non-ideal characteristic of the op-amp are calculated using Equation (8) as $f_{p1}=57.6$ KHz and the other corner frequency is very far at $f_{p2}=4$ GHz. In comparison with the results from the LTSpice simulation, the first corner frequency $f_{p1}=53.5$ KHz is shown very clear in Fig. 7, but the corner frequency of the zero and the other pole are beyond the operating frequency bandwidth of the op-amp. There is another corner frequency coming from the input section and calculated from equation (10) as $f_{p3} = 1/2\pi C_{s2} R_2=159$ MHz using the following typical values $C_{s2} =100$ pF, $C_x =0.35$ pF, $R_2=10$ Ω and $R_f=10$ Ω to eliminate the effect of the offset voltage while the simulation result shows $f_{p3}=158.5$ MHz (see Fig. 7).

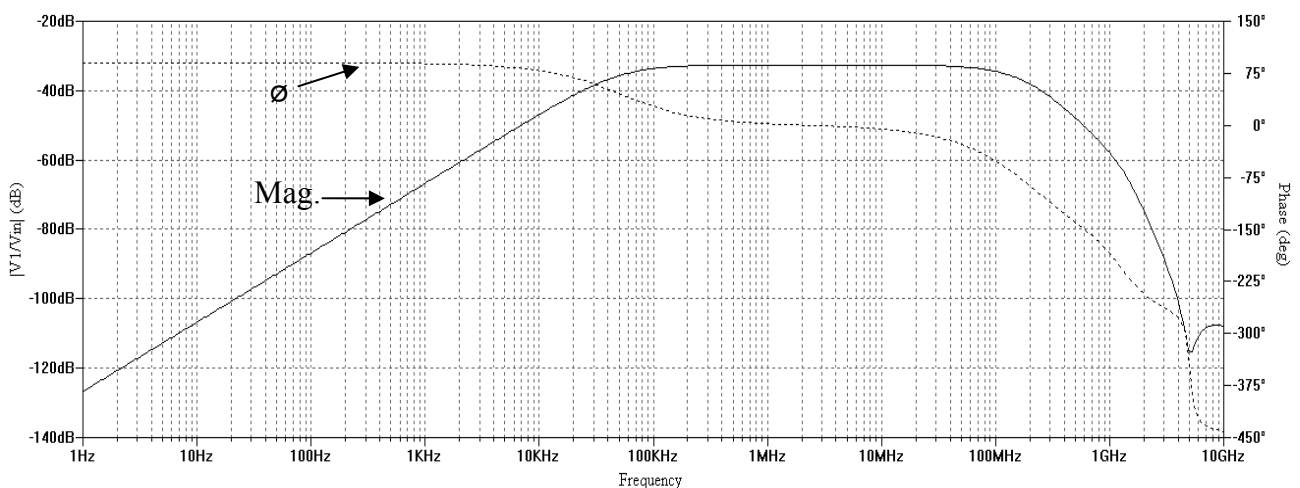


Fig. 7. Frequency response of the measuring circuit.

There are two significant advantages for the developed circuit obvious in the result of the frequency response shown in Fig. 7. In the range between 200 kHz to 20 MHz, it is clear that the gain is constant and the phase shift is almost zero. Thus, the same board can be operated at any frequency within this frequency range. Multiple circuits can be operated simultaneously eliminating the need for time multiplexing. In the following section an application where the capacitance measuring circuit is utilized is explained.

5. Metal Fill Time Application

The metal fill profile in Lost Foam Casting (LFC) plays a significant role among several factors that affect casting quality. The metal fill profile is in turn affected by numerous factors. Several casting defects may result due to an improper metal fill process. It is thus essential to characterize and if possible control the metal fill process in the LFC. Existing methods for monitoring the metal fill pattern are very expensive and invasive. These include the Real-Time X-ray (RTX-Ray) or hundreds of thermocouples [14].

Therefore, developing an in-situ, low cost and ruggedized system for capturing the metal flow profile is a very important application. A simpler parameter that is usually used on the foundry floor is the fill time of a casting. This single parameter is indicative of consistency of the process and a large change in the fill time provides instantaneous and valuable feedback about the process. A simple algorithm for estimating the fill time from capacitive measurement is described hereafter.

5.1. Experimental Procedure

The main concept of the system is capturing the change, in the capacitance between embedded transmitters and receivers electrodes (sensors), corresponding to increasing the molten metal inside the foam pattern. Two capacitive sensor pairs (transmitter and receiver) are distributed around the pattern inside a flask. A flat plate foam pattern (152 mm x 203 mm x 8 mm) was used in the experiment. Fig. 8 shows the schematic diagram for the sensors around the pattern inside the flask. A capacitance measuring circuit is used to measure the mutual capacitance changes between each pair of the transmitter and receiver electrodes. As the amount of the molten metal inside the foam pattern increases, the mutual capacitance measured between the electrodes C_x decreases. Each of the measuring circuits is operated at a different frequency; hence there is no crosstalk between the two sensors.

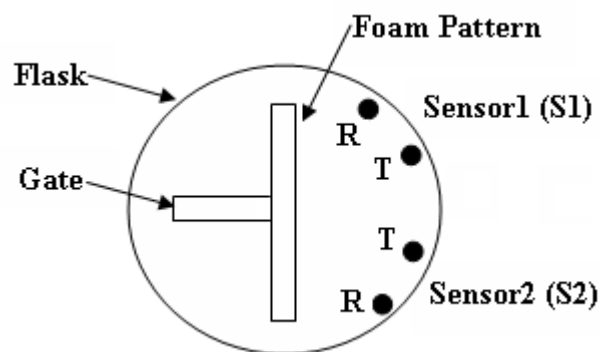


Fig. 8. Schematic diagram of the capacitive sensors arrangement.

Both circuits use Mote-technology to send the data from the sensors to a central station wirelessly [6]. This station is connected to a computer where a signal processing algorithm has been developed to manipulate the data and compute the metal fill time. Using wireless techniques significantly reduces the effect of stray capacitance since the length of the cables used to connect the sensors to the computer is much shorter. The monitored casting process is a special one called counter-gravity casting. A vacuum is applied to the top of the flask through a sealed head and the metal is “sucked” out of the furnace and through a ceramic sprue to the foam pattern from the bottom of the flask. The more the vacuum applied to the system, the higher the metal flow rate and the lower the fill time.

5.2. Fill Time Computing Algorithm

An algorithm implemented using LabVIEW software and consisting of three stages has been developed to analyze the capacitance measurements and compute the fill time. Fig. 9 shows the flow chart of the algorithm. As a first step, the measured signals are filtered using a median filter of rank 10 to smooth the signal and remove any noise. Fig. 10 shows the responses of the capacitance sensors as the metal fills the foam pattern after the filtering.

In the second stage, the slope of each signal is determined by taking the first derivative to identify the sharp transient changes related to the starting and ending of the filling process. The derivative of the first signal is shown in Fig. 11 after passing through a median filter to remove all the small variations related to small changes in the slope. The final stage is measuring the response time of each sensor by identifying and computing the difference between the starting and ending time of the metal fill. A threshold is selected heuristically for determining these times. Fig. 12 shows the start and end time of the response of sensor 1 (S_1). The starting and ending times are 3.9 and 32.6 sec. respectively, and the difference is 28.7 sec. The response time for the second sensor (S_2) is 24.7 seconds shown in Fig. 13. The overall pattern fill time depends on the minimum of the start times and the maximum of the end times for all sensors. In this case it is 28.7 sec.

6. Conclusions

A new capacitance measuring circuit is designed and analyzed for measuring the mutual capacitance between two electrodes. The proposed circuit has many advantages such as stray-immunity, linearity, high sensitivity, and wide range of operating frequency (100 kHz to 20 MHz) with zero phase shift. The latter advantage allows multiple circuits to work simultaneously provided that each board works at a different frequency with a minimum frequency difference. Theoretical analysis has been given to illustrate the behavior of the measuring stage, taking in account the non-ideal characteristic of the current feedback amplifier. LTSpice simulations were carried out to verify the mathematical analysis. An application for the proposed circuit in the estimation of the pattern fill time in LFC process is explained. The suggested method for estimating fill time introduces an inexpensive, stable, and fast sensor for estimating the fill time profile.

Acknowledgments

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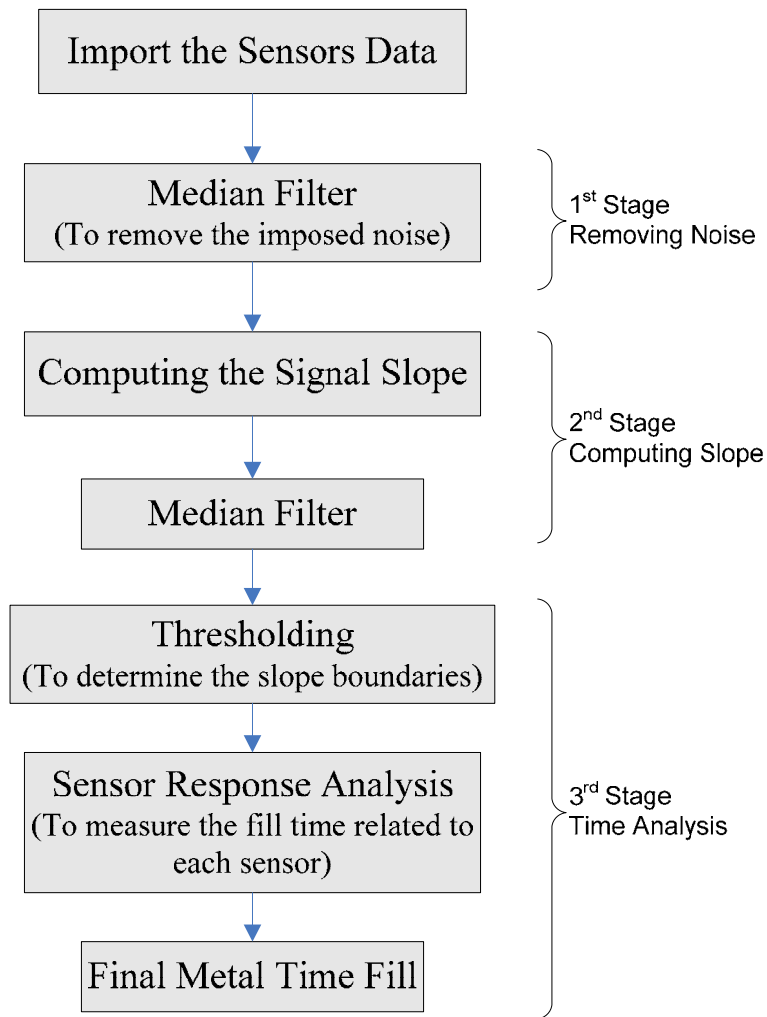


Fig. 9. Flow chart of the metal fill time algorithm.

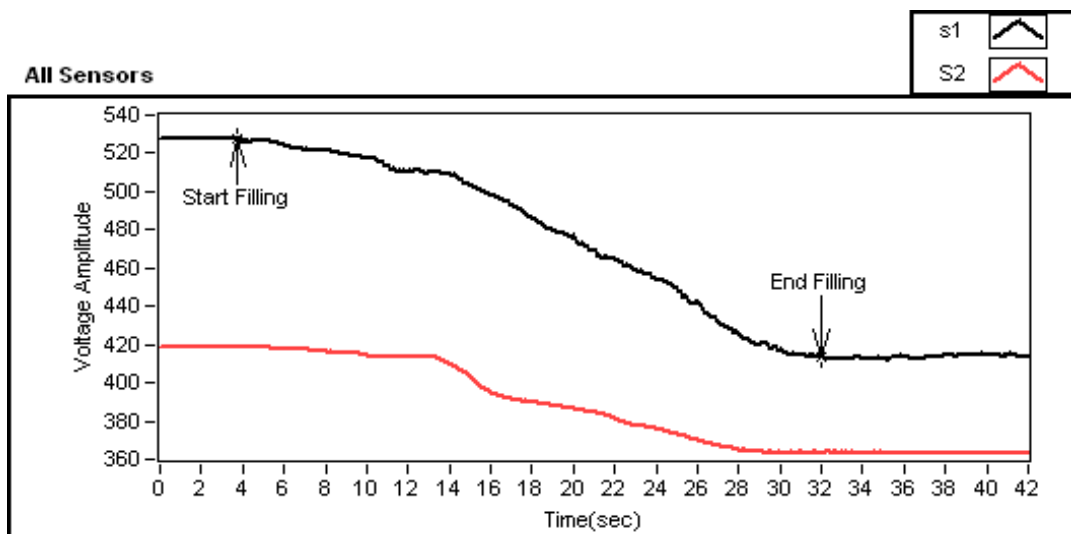


Fig. 10. Metal fill sensors responses.

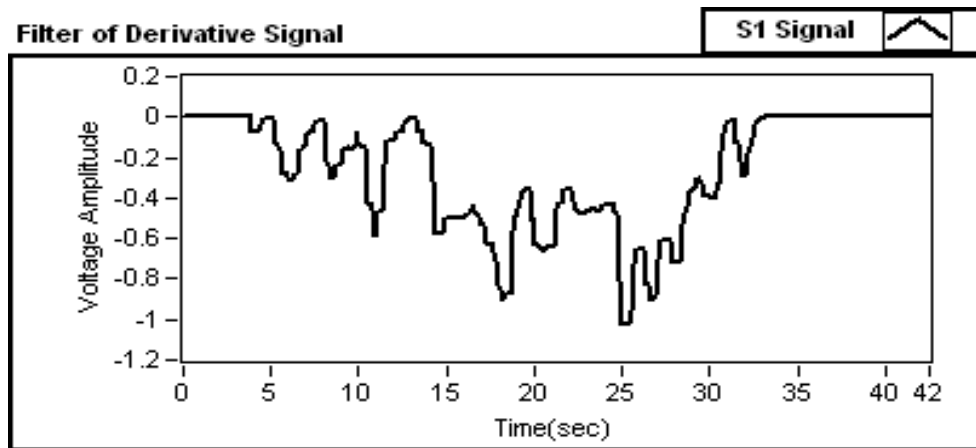


Fig. 11. Derivative signal after filtering by a median filter.

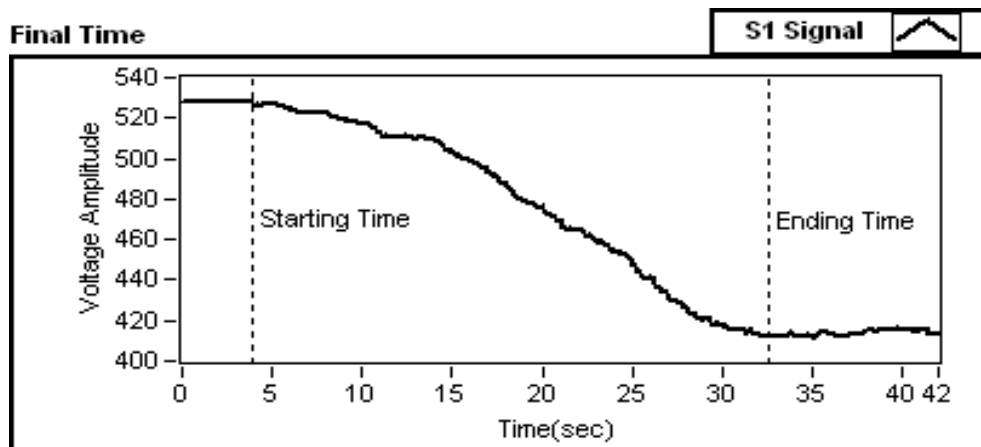


Fig. 12. The final result shows the starting and ending time for S1.

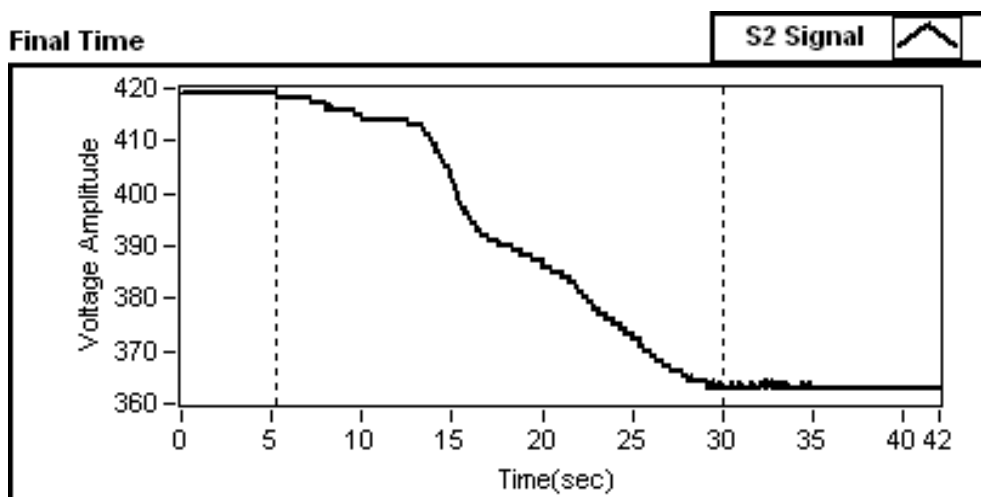


Fig. 13. The final result shows the starting and ending time for S2.

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