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Dynamic Base Current Compensation for Cascaded Bipolar Low Noise Amplifier

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Abstract: Scientific instruments often need an electronic readout system with small input noise, large output signals and small distortion. In order to adapt the newest requirements of an X-ray space mission, several differential low-noise amplifiers have been developed employing diodes as loads, based on a 350 nm SiGe BiCMOS technology. The amplifiers have shown a good performance of AC gain, noise and gain-drift. However, the linearity degrades due to cascaded topology. This work proposes a new design with a dynamic base current compensation system based on the original amplifier topology, appended to the cascaded differential pairs using diodes as loads. The linearity performance is strongly improved according to the dedicated simulation results. The mismatch issue has been further verified by Monte-Carlo simulations.

Keywords: Non-linearity, Low-noise amplifier, Differential amplifier, BiCMOS technology, Hetero-junction bipolar transistor.

1. Introduction

Thanks to the advancing technology, scientific instruments have been quickly developed and turn to be more and more precise in decades. It leads to harsher requirements for electronic readout systems: the quality of detected signals could be degraded by input noise, gain-drift, non-linearity, etc.

Several Low-Noise Amplifiers (LNA) using a SiGe BiCMOS 350 *nm* technology have been developed, trying to reach the requirements such as an equivalent input voltage noise$< 1\ nV/\sqrt{Hz}$, a voltage gain at the order of a hundred *V/V*, with a gain drift ≤200 $\mu V/V$, a large output signal with about 1 V_{pp} amplitude and still keeping a good linearity [1].

The LNAs use a common emitter topology with hetero-junction bipolar transistors (HBT) for the differential pair and diodes as loads, as shown in Fig. 1. Amplifier A_1 has one single differential stage with three diodes in series as loads; Amplifier A_2 has three differential stages cascaded where each stage with two diodes in series as loads. Theoretically, according to Eq. (1), all the variables could be cancelled, and the gain just equals to the number of the diode loads n_D in series, which produces a very stable gain. In addition, differential topology suppresses even order harmonics, improving the linearity. Moreover, the HBT provided by the technology has a good noise performance comparing to MOS.

$$|Gain| = g_m \times r_D \times n_D \approx \frac{qI_C}{k_B T} \times \frac{k_B T}{qI_D} \times n_D = n_D, \quad (1)$$

where g_m is the HBT transconductance, r_D is the small signal resistance of diodes, k_B is the Boltzmann constant, T is the temperature in Kelvin, q is the electron charge in absolute value, I_C is the collector current, I_D is the diode current and $I_C = I_D$ [2].

Table 1 compares the measurement results of these two LNAs, both biased with I_C = 2 *mA* and power supplied by V_{CC} = 3.3 *V*. The gain performance of

LNA A_1 is very close to the theoretical analysis and simulations (2.97 *V/V* comparing to 3 *V/V*). In contrast, LNA A_2 with three stages cascaded has the results less satisfying. Especially, when the output signal amplitude is larger than 227 *mV*, the gain's non-linearity largely degrades (7.57 *V/V* comparing to 8 *V/V*).

Table 1. Measurements of the 2 LNAs with diodes loads.

LNA	AC gain	Dynamic Range
A_1	2.97 *V/V*	$V_{in} \approx \pm 200\,mV$, $V_{out} \approx \pm 594\,mV$
A_2	7.57 *V/V*	$V_{in} \approx \pm 30\,mV$, $V_{out} \approx \pm 227\,mV$

However, for having a larger gain, it is necessary to cascade several such stages. The new topology presented in this article, is a dynamic base current compensation system appended to the cascaded differential pairs using diodes as loads, aiming to solve the non-linearity problem found from the measurements of the amplifier A_2. In the first published paper, we showed that the new topology could well improve the linearity performance according to the results of AC, DC, transient and noise simulations [3]. In this paper, the linearity performance has been further proved by pss simulation. Monte-Carlo simulations have also been done to verify the mismatch issue.

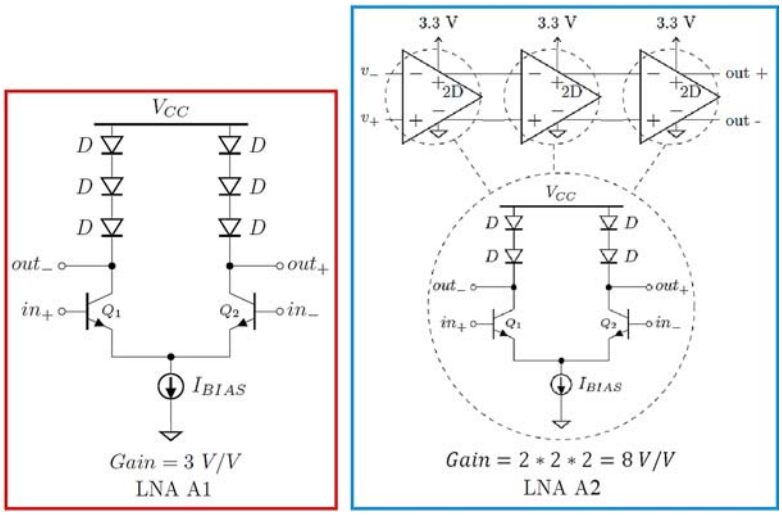

Fig. 1. Differential pair with 3 diode[1] loads – LNA A_1 (left); LNA A_2 with 3 differential stages cascaded where each stage with two diodes in series as loads (right).

2. Linearity Analysis of Differential Pairs

2.1. Differential Pair with Resistive Loads

Resistance is a linear component, but bipolar transistor is non-linear. For a differential pair with resistive loads R_C (Fig. 2), in the small signal analysis, its characteristics could be considered linear. But in the large signal analysis, the non-linear characteristics could not be neglected.

Considering a large differential signal applied to the differential inputs, $\pm\Delta V$ represent a change of the differential signal respectively at the two inputs during the same period, then $V_{in} = 2\Delta V$. On the other hand, V_{out} can be deducted as:

$$\begin{aligned} |V_{out}| &= V_{out}^{+} - V_{out}^{-} \\ &= \left(V_{CC} - I_{C_{Q1}} R_c\right) - \left(V_{CC} - I_{C_{Q2}} R_c\right) \\ &= R_c\left(I_{C_{Q2}} - I_{C_{Q1}}\right) \end{aligned} \quad (2)$$

ΔV is introduced with Taylor expansion, as shown in Eq. (3), where $V_T = \frac{k_B T}{q}$ and I_S the saturation current [4].

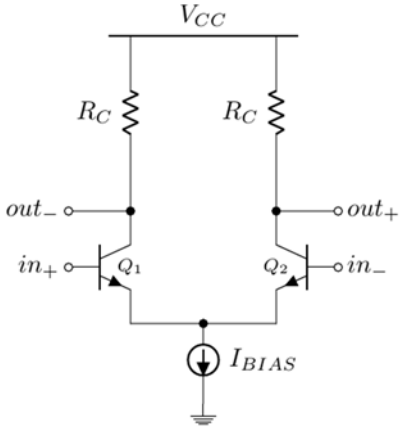

Fig. 2. Differential pair with resistive loads.

[1] The diode is realized by connecting the base and the collector of a HBT.

$$
\begin{aligned}
I_{C_{Q2}} - I_{C_{Q1}} &= \left(I_S e^{\frac{V_{BE}+\Delta V}{V_T}} - I_S e^{\frac{V_{BE}-\Delta V}{V_T}}\right) \\
&= I_S e^{\frac{V_{BE}}{V_T}} \left(e^{\frac{\Delta V}{V_T}} - e^{-\frac{\Delta V}{V_T}}\right) \\
&= I_S e^{\frac{V_{BE}}{V_T}} \left\{1 + \frac{\Delta V}{V_T} + \frac{1}{2!}\left(\frac{\Delta V}{V_T}\right)^2 + \frac{1}{3!}\left(\frac{\Delta V}{V_T}\right)^3 + \right. \\
&\cdots - \left[1 + \left(-\frac{\Delta V}{V_T}\right) + \frac{1}{2!}\left(-\frac{\Delta V}{V_T}\right)^2 + \right. \\
&\left.\left. \frac{1}{3!}\left(-\frac{\Delta V}{V_T}\right)^3 + \cdots\right]\right\} \\
&\approx I_S e^{\frac{V_{BE}}{V_T}} \left[\frac{2\Delta V}{V_T} + \frac{1}{3}\left(\frac{\Delta V}{V_T}\right)^3\right] \qquad (3)
\end{aligned}
$$

Substituting Eq. (3) into Eq. (2), the gain can be expressed by Eq. (4). It is noticeable that the standard differential topology improves the linearity performance of an amplifier by cancelling all the even-order harmonics. It is the remaining odd-order harmonics that introduce the main non-linearity [5].

$$
\begin{aligned}
|Gain| &= \frac{V_{out}}{V_{in}} = \frac{R_C\left(I_{C_{Q2}} - I_{C_{Q1}}\right)}{2\Delta V} \\
&= I_S R_C e^{\frac{V_{BE}}{V_T}} \left[\frac{1}{V_T} + \frac{1}{6}\frac{(\Delta V)^2}{V_T^3}\right]
\end{aligned} \qquad (4)
$$

2.2. Differential Pair with Diode Loads

Although diode and bipolar transistor are both non-linear components, bipolar transistor differential pair with diode loads has a better linear performance. With the same method, $V_{\text{in}} = 2\Delta V = 2\Delta V_{\text{BE}}$, and V_{out} can be calculated by Eq. (5), with n_{D} the number of diodes in series as loads.

$$
\begin{aligned}
|V_{out}| &= V_{out}^{+} - V_{out}^{-} \\
&= \left(V_{CC} - n_D(V_D - \Delta V_D)\right) - \left(V_{CC} - \right. \\
&\left. n_D(V_D + \Delta V_D)\right) \\
&= 2n_D \Delta V_D
\end{aligned} \qquad (5)
$$

Assuming the diodes and bipolar transistors always work in the ideal regime, then they have the similar transfer functions: $I_D = I_S(e^{\frac{V_D}{V_T}})$ and $I_C = I_S(e^{\frac{V_{BE}}{V_T}})$. The diodes and bipolar transistors of the same branch of a differential pair are crossed by the same current $I_{\text{D}} = I_{\text{C}}$. The variation at input causes the same current variation in the diodes and bipolar transistors of the same branch, which gives:

$$
\begin{aligned}
I_S e^{\frac{V_{BE}+\Delta V_{BE}}{V_T}} &= I_C + \Delta I_C = I_D + \Delta I_D \\
&= I_S e^{\frac{V_D+\Delta V_D}{V_T}}
\end{aligned} \qquad (6)
$$

Then $\Delta V_{\text{D}} = \Delta V_{\text{BE}}$. So the gain simply equals to $\frac{2n_D \Delta V_D}{2\Delta V_{BE}} = n_D$. However, the gain could not keep linear with such large amplitude at input, as the measurements have shown. More details will be discussed in the following sections.

2.3. Cascaded Differential Pair with Diode Loads

Take another look at Table 1, Amplifier A_1 has a smaller gain, but keeps its good linearity until V_{out} reaches ±600 mV; in contrast, amplifier A_2 has a larger gain, but only keeps its good linearity until a much smaller V_{out} around ±220 mV. The comparison suggests that the cascade of the stages leads to the degradation of the linearity performance; otherwise, the V_{out} of A_2 should at least as large as the V_{out} of A_1.

Indeed, for a large (comparable to the biasing voltages) instantaneous output voltage, the two sides of the differential pairs are very unbalanced. While one side's input signal reaches its maximum value, almost all of the 4 mA, the biasing current of the whole differential pair flows in the corresponding branch. At the same time, it only remains a few tens of microamperes in the other side. Indeed, in the architecture of amplifier A_2, the outputs of one stage are directly connected to the inputs of the next stage, namely the bases of the next differential pair, so the diode current is equal to the collector current plus the base current of the next stage. Since the gain of one stage is negative ($-g_m r_D$), the base current of the bipolar transistor increases at the same time as the collector current I_C of the connected previous stage decreases, so the base of the bipolar transistor of the second differential pair with increasing current will extract more and more current from the branch of the first differential pair whose current is in fact decreasing. With nearly all of 4 mA biasing current passing through one branch, the bipolar transistor will extract $\frac{4\ mA}{230} \approx 17\ \mu A$ from the branch of the first stage that has only a few tens of microamperes current left. This means that the extraction of the current by the second stage makes the first stage more unbalanced and makes false the Eq. (1) which needs to have I_C=I_D, decreasing its gain in large signals compared to $Gain = n_D$ (Eq. (1)), thus causes larger non-linearity worsen by the cascaded amplifier [1].

3. Dynamic Base Current Compensation System

3.1. Concept

In order to dynamically compensate the base current and improve the linearity, a new dynamic base current compensation system adapting to the LNA using diodes loads has been designed (Fig. 3). In this system, a dummy differential pair P_3 is added to the cascaded amplifier, with similar topology and same dimensions as the differential pair P_1 and P_2. Assuming the biasing conditions of the components of P_3 are very close to those of P_2, the base of Q_5/Q_6 will extract the same current as the base of Q_3/Q_4 does from P_1. Until this step, twice the current is extracted as Q_5/Q_6 does from P_1. Q_7 and Q_8 also have the same dimensions as Q_5 and Q_6. If they are also identically

biased as Q_5 and Q_6, there will be the same amount of current passing through their bases as Q_5 and Q_6. Then the two current mirrors CM_1 and CM_2, with $\frac{W_2}{L_2} = \frac{2W_1}{L_1}$, $\frac{W_4}{L_4} = \frac{2W_3}{L_3}$, permit to provide the currents back to P_1, that always equal to the instantaneous current losses following the amplified signal. In consequence, there will be no extraction of current from the first stage, and the linearity performance of the whole topology could be maximized.

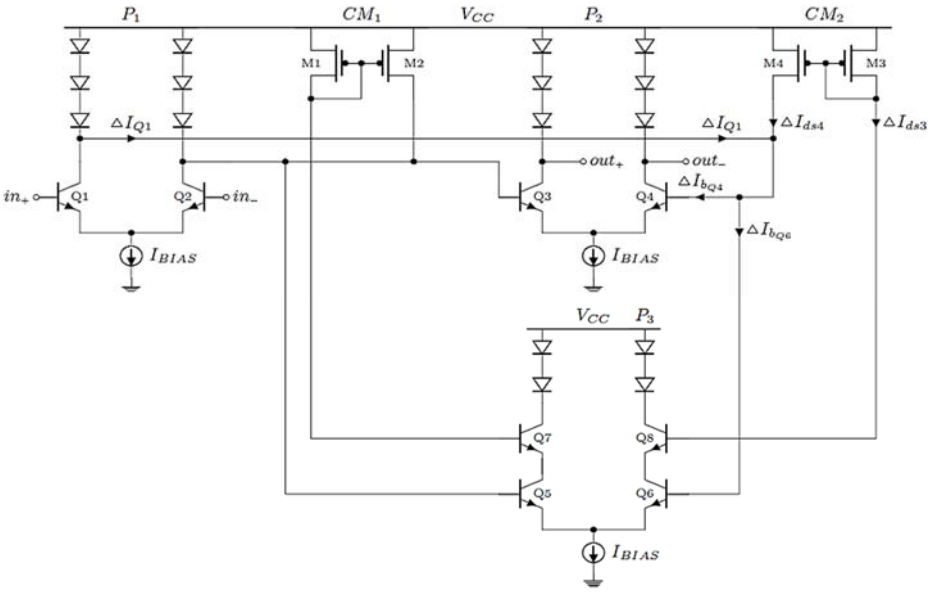

Fig. 3. Dynamic base current compensation system for two stages cascaded bipolar amplifier P_1 and P_2. P_3 operates as a dummy stage used to "monitor" the second stage base current without any degradation of the performances of the second stage itself. Current mirrors (CM_1 and CM_2) dynamically replicate 2 times the measured base current.

3.2. Tuning

For the transistors and diodes of the amplifiers, $L = 400\ \mu m$ and $W = 0.4\ \mu m$are chosen as constants for emitter in order to reach a current gain $\beta \approx 230$, close to its maximum value [6]. For the measurement of amplifier A_1, $V_{in\text{CM}}$ = 1.1 V is used as the input voltage in common-mode between supply voltage 3.3 V and the ground 0 V, which permits a reasonable dynamic range and also lets the input voltage in common-mode very close to the output voltage in common-mode ($V_{out\text{CM}} \approx 1.1\ V$). $I_C = 2\ mA$ is provided as biasing current for each branch of the differential pairs, in order to have an equivalent input noise lower than $1\ nV/\sqrt{Hz}$ [2], at the same time having a large input resistance of the differential pair h_{11}. In order to do a better comparison, it is more interesting to keep the same values mentioned above for the simulations. In consequence, the only parameters left are the channel's length and width of the PMOS: M_1, M_2, M_3 and M_4.

3.2.1. Determination of the Channel's Length for PMOS

The two current mirror CM_1 and CM_2 play a key role in the system. Since it is hoped that twice the extraction current can be given back to the first stage, it is important to well define the dimensions of PMOS. For the two PMOS of one current mirror have a large but different V_{DS}, the channel-length modulation effect becomes quite noticeable, and their channel-length modulation coefficient λ could not be the same. In this situation, the currents could not be well regulated. In order to limit the channel-length modulation effect, it is better to use a longer length, so that the correction coefficient $(1 + \lambda V_{DS})$ in Eq. (7) is negligible, and the equation becomes the general expression of g_m Eq. (8) [5]. Because the two PMOS of one current mirror have the same ΔV_{GS}, ΔI_{DS} will be proportional to W/L. According to the simulation, $L = 25\ \mu m$ is enough to well limit the channel-length modulation effect and double the AC current by the current mirrors, namely $i_{DS2} \approx 2i_{DS1}$, $i_{DS4} \approx 2i_{DS3}$.

$$g'_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_p C_{ox} \frac{W}{L}(V_{GS} - V_{th})(1 + \lambda V_{DS}) \quad (7)$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \mu_p C_{ox} \frac{W}{L}(V_{GS} - V_{th}) \quad (8)$$

3.2.2. Determination of the Channel's Width for PMOS

In order to well return twice the extraction AC current, it is also necessary that Q_5 and Q_6 in P_3 have the similar biasing conditions to Q_3 and Q_4 in P_2, so that they could have very close value of β. Then

according to Eq. (9), they could extract the same i_b [7]. Similarly, Q_7 and Q_8 should have the similar biasing conditions to Q_5 and Q_6, thus they could well copy the current and provide it to the current mirrors.

$$\frac{dI_B}{dV_{BE}} = \frac{qI_C}{\beta k_B T} \tag{9}$$

The V_B of Q_5/Q_6 is fixed by the output of P_1. The V_E of Q_5/Q_6 follows its V_B by the difference around 0.72 V. The V_C of Q_7/Q_8 is fixed by the voltage drop across the diode loads. However, the V_B and V_E of Q_7/Q_8 are free (the V_C of Q_5/Q_6 equals to the V_E of Q_7/Q_8), which need to vary the width of M_1 and M_3 to adapt. According to the simulation, with channel's width of PMOS W_1=W_3=25 μm, $i_{bQ5} \approx i_{bQ7} \approx i_{bQ3}$, $i_{bQ6} \approx i_{bQ8} \approx i_{bQ4}$.

3.3. Simulation Results

Different types of simulation, such as DC, AC, noise, transient, pss, and Monte-Carlo simulations were run in order to check many aspects of the performance. Fig. 4 shows the good performances of AC gain and noise, with a bandwidth > 200 *MHz* and an equivalent input voltage noise $\approx 700\, pV/\sqrt{Hz}$. The comparison of simulation results in Fig. 5 illustrates that the dynamic is strongly improved, up to $V_{in} \approx \pm 103\ mV$ and $V_{out} \approx \pm 920\ mV$. The linearity performance was further proved by pss simulation, which is suitable for large signal analysis. Fig. 6 traces the Total Harmonic Distortion (THD) evolved with frequency, obtained from pss simulation. The design can keep its THD lower than 1 % until nearly 400 *kHz*, and lower than 10 % (corresponding to -1 *dB*) up to 8 *MHz* with 1 V_{pp} output signal.

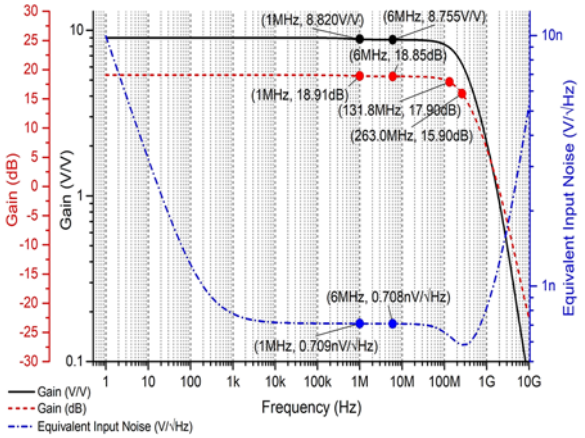

Fig. 4. AC gain and noise simulation for 2 cascaded stages of differential pair with the dynamic base current compensation system.

Fig. 7 shows that the current extracted from Q_1 is significantly reduced. Indeed, when I_C reaches its minimum value in the corresponding branch of the differential pair, the instantaneous extraction current is dramatically reduced from original about 17 μA to now 10 *nA*. However, two small negative peaks of about 150 *nA* remain, but only when the I_C is large as 3 *mA*.

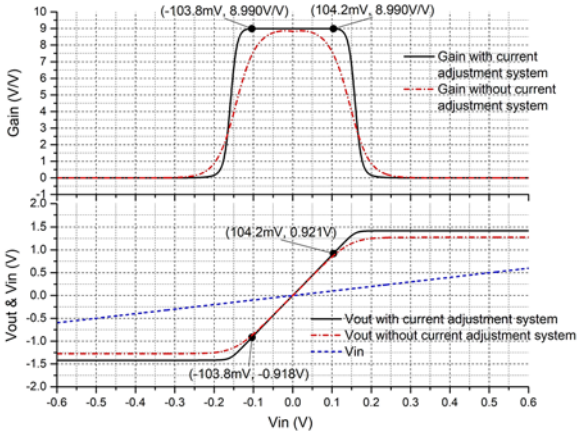

Fig. 5. Simulation – Comparison of linearity performance between 2 cascaded stages of differential pair with and without the dynamic base current compensation system.

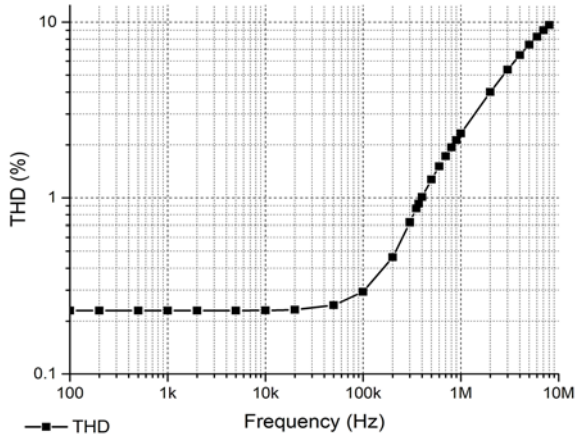

Fig. 6. Pss Simulation – Total Harmonic distortion of dynamic base current compensation system at different frequency.

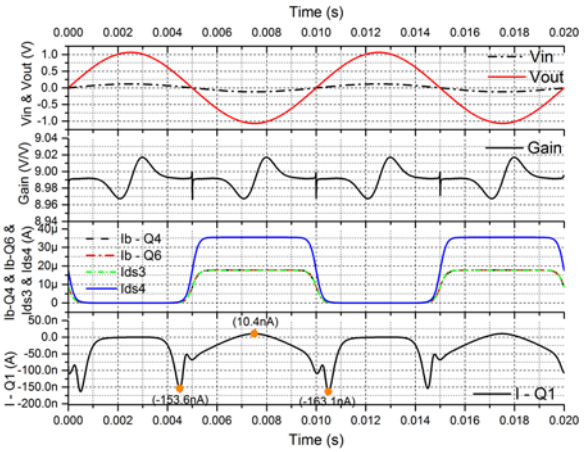

Fig. 7. Dynamic base current compensation performance simulation for 2 cascaded stages of bipolar differential pair with three diodes as loads.

In any cases, this little fluctuation will not influence the differential pair's normal operation at all.

Fig. 8 illustrates the verification of the linearity performance considering mismatch by Monte-Carlo simulations. The gain is not significantly degraded up to 100 *mV* input. Another Monte-Carlo simulation with 5000 iterations shows the distribution of the gain at 300 *kHz* considering mismatch of parameters, as shown in Fig. 9. The gain has a Gaussian-like distribution with mean value around 8.946 *V/V* and standard deviation of about 1 *mV/V*. Indeed, in the design, each transistor/diode is composed by 8 transistors in parallel, which improves the matching. Moreover, a differential pair of transistors or diodes in the design comprises 16 transistors, which could easily form a common centroid pattern while realising layout, thus it could further reduce any mismatching.

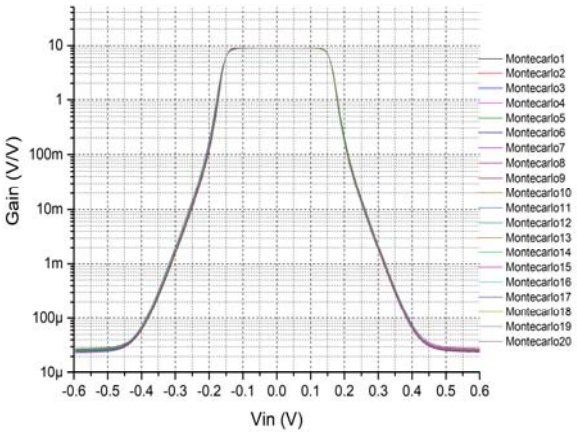

Fig. 8. Monte-Carlo mismatch simulation showing the linearity performance obtained with dynamic base current compensation system.

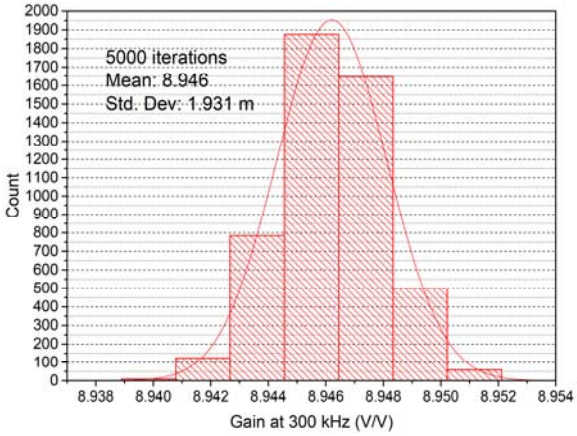

Fig. 9. Gain distribution from Monte-Carlo mismatch simulation with the dynamic base current compensation system.

4. Discussions

4.1. Trade-off Between Noise, Input Impedance and Gain Drift Regarding Temperature Variation

The choice of the biasing current I_C's value is not only important for the noise performance, but also critical for the input resistance and the gain drift with regard to the temperature variation. In general, the equivalent input noise can be expressed as Eq. (10). For a stage with diodes as loads, the last term under the root of Eq. (10) needs to be replaced by diodes' shot noise, as shown in Eq. (11), where $Gain = n_D$, according to Eq. (1). The simplification of the equivalent input noise Eq. (11) gives Eq. (12), which is useful to estimate the biasing current to optimize the noise [2]. With n_D=3, and with a source impedance $R_S \approx 200\ \Omega$ for the differential inputs, namely $\frac{1}{2}R_S = 100\ \Omega$ for each input of the differential pair for the calculation, we could get $I_{C\text{-opt}} \approx 4.5\ mA$. This approximated value is still very close to the one obtained with simulations.

$$\sqrt{S_v} = \sqrt{2} \times \sqrt{4k_B T R_{bb'} + 2qI_B \left(\frac{\left(R_{bb'}+\frac{R_S}{2}\right)h_{11}}{R_{bb'}+\frac{R_S}{2}+h_{11}}\right)^2 + \frac{2qI_C}{g_m^2} + \frac{4k_B T/R_L}{g_m^2}}, \quad (10)$$

$$\sqrt{S_v} = \sqrt{2} \times \sqrt{4k_B T R_{bb'} + 2qI_B \left(\frac{\left(R_{bb'}+\frac{R_S}{2}\right)h_{11}}{R_{bb'}+\frac{R_S}{2}+h_{11}}\right)^2 + \frac{2qI_C}{g_m^2} + \frac{2qI_D \times r_D^2 \times n_D}{Gain^2}}, \quad (11)$$

$$\sqrt{S_v} \approx \sqrt{2} \times \sqrt{2q\frac{I_C}{\beta}\left(\frac{R_S}{2}\right)^2 + \frac{2(k_B T)^2}{qI_C} \times \left(1 + \frac{1}{n_D}\right)} \quad (12)$$

However, the input resistance of the differential pair h_{11} is inversely proportional to I_C: $h_{11} = \frac{\beta k_B T}{qI_C}$. With $I_{Copt} = 4.5\ mA$, $\beta \approx 230$ at 300K, $h_{11} \approx 1300\ \Omega$, which is not greatly larger than $\frac{1}{2}R_S = 100\ \Omega$.

The ratio between h_{11} and $\frac{1}{2}R_S$ does not only affect the ratio of the input signal recovered by the amplifier, but also degrades the gain drift with regard to the temperature variation. It is due to the fact that h_{11} is proportional to T, and changes the ratio of the input voltage bridge divider. Supposing that V_{in} is the signal given by the previous stage, and V'_{in} is the voltage delivered to the input of the amplifier, then $Gain_T = \frac{V_{out}}{V_{in}}$, $Gain_A = \frac{V_{out}}{V'_{in}}$. Eq. (13) puts $Gain_T$ and $Gain_A$ together:

$$\begin{aligned} Gain_T &= Gain_A \times \frac{V'_{in}}{V_{in}} \\ &= Gain_A \times \frac{h_{11}}{h_{11} + \frac{1}{2}R_S} \\ &= Gain_A \times \frac{1}{1 + \frac{R_S q I_C}{2\beta k_B T}} \end{aligned} \quad (13)$$

Here we only focus on the variation of gain caused by h_{11} and consider the gain of amplifier $Gain_A$ as a constant. Then from Eq. (13), we get Eq. (14), where $X = \frac{R_S q I_C}{2\beta k_B}$.

$$\frac{dGain_T}{dT} = Gain_A \times \frac{X}{(T+X)^2} \quad (14)$$

With R_S = 200 Ω, β ≈ 230 at 300 *K*, a gain drift of about 200 μ*V*/*V* results in I_{Cmax} ≈ 3.4 *mA*, only considering the input voltage divider. In fact, because $Gain_A$ also fluctuates with temperature, and normally fluctuates more for a system with more stages, it is necessary to choose a smaller current. With I_C = 2 *mA*, the equivalent input noise ≈ 730 $pV/\sqrt{Hz}$, which still leaves room for more possible compromise.

4.2. Four Stages Cascaded of Differential Pair with Diodes Loads

Because the input and output common-mode voltage of each stage are very close (1.1 *V*), it is easy to reach a higher gain by cascading more stages. The dynamic base current compensation system is essential for each stage to have a better linearity performance. The simulation shows that, using the topology with the dynamic base current compensation system, the 4 stages amplifier could reach a gain ≈ 80 *V*/*V* with V_{in} ≈ 12 *mV* and V_{out} ≈ 1 *V*, and still keep a good linearity (Fig. 10).

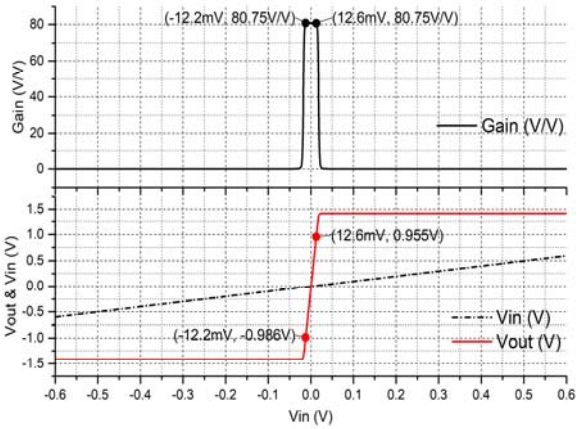

Fig. 10. Linearity simulation for 4 cascaded stages of differential pair with dynamic base current compensation system.

4.3. Perspective

In spite of the improvement realised by the dynamic base current compensation system presented in this paper, dynamic range, and thus linearity performance, of an amplifier is naturally limited by the power supply level. An amplifier with a 3.3 *V* power supply can never have an output amplitude over 3.3 *V*, and even less for good linearity performance. If larger output amplitude is desired, increasing the power supply to a higher level, such as 5 *V*, is also required. Moreover, a larger voltage margin makes it possible to increase the number of diodes in series as load from 3 (Fig. 1, left) to 4. Having more diodes in series means getting a larger gain per stage, as Eq. (1) shows. This therefore leads to a smaller equivalent input noise, as shown in Eq. (11) and Eq. (12), if n_D increases, the last term representing the equivalent diodes' short noise at input decreases, so does the total noise.

On the other hand, higher power supply directly leads to higher consumption. Transistors also endure a larger V_{CE}, which needs to be maintained under their maximum value.

Because the appended dynamic base current compensation system use the same amplifier topology as each stage, it can easily manage the change of power supply and the number of diodes in series, so that the dynamic range and the linearity performance could be further improved with 5 *V* power supply comparing to the 3 diodes topology discussed in this paper and biased with 3.3 *V*.

5. Conclusions

Cascading bipolar differential pairs with diodes loads is a simple and efficient way to reach a higher gain with very low drift. However, opposite phase of base current of the next stages degrades dramatically the linearity. The dynamic base current compensation system proposed in this paper could significantly improve the linearity performance of the amplifier with such cascaded differential pairs. With careful tuning, the amplifier could still keep good performance on noise, input impedance and gain drift.

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References

[1]. S. Chen, *et al.*, Development of the WFEE subsystem for the X-IFU instrument of the ATHENA space observatory, in Space Telescopes and Instrumentation 2018: Ultraviolet to Gamma Ray, *SPIE*, Vol. 10699, 2018.

[2]. D. Prêle, *et al.*, Gain drift compensation with no feedback-loop developed for the X-Ray Integral Field Unit/ATHENA readout chain, *Journal of Astronomical Telescopes, Instruments, and Systems*, 2016.

[3]. S. Chen, *et al.*, Analysis and Improvement of Linearity Performance of Low Noise Amplifier with Diode Loads, in *Proceeding of the 2nd International Conference on Microelectronic Devices and Technologies (MicDAT' 2019)*, Amsterdam, The Netherlands, 22-24-May 2019, pp. 36-42.

[4]. A. S. Sedra, K. C. Smith, Microelectronic circuits, *Oxford University Press*, New York, Vol. 1, 1998.
[5]. Behzad Razavi, Design of Analog CMOS Integrated Circuits, *McGraw-Hill, Inc.* New York, NY, USA, 2001.
[6]. AMS 0.35 um HBT BiCMOS Process Parameters Rev.5.0, *Austriamicrosystems AG*, 2009.
[7]. S. M. Sze, K. K. Ng, Physics of semiconductor devices, *John Wiley & Sons*, 2006.