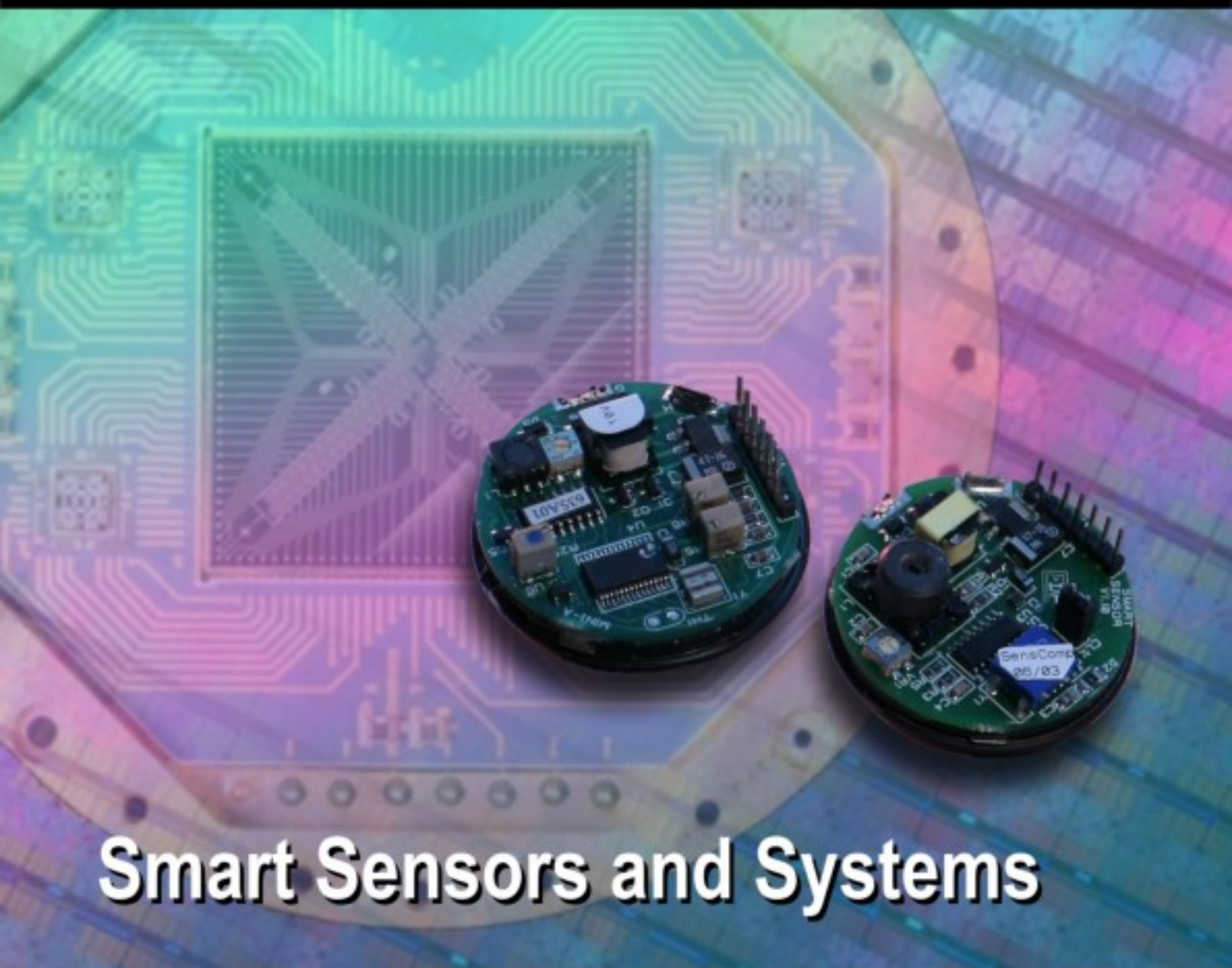


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## IEEE 1451.0-2007 Compatible Smart Sensor Readout with Error Compensation Using FPGA

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**Abstract:** This paper deals with effective usage of user TEDS for developing smart sensor readout which is suitable to estimate and compensate the disturbances occurring in the system. The system parameters are incorporated along with other transducer data. Appropriate processing capabilities are built in Transducer Interface Module TIM for disturbance estimation and compensation. A Verilog based single chip module of IEEE 1451.0 smart sensor is proposed incorporating the above mentioned features. The architecture enables reliable and smart readout for sensors at low cost for a given application. The programmable nature of the proposed architecture enables wide usage of the smart sensor for various applications. *Copyright © 2009 IFSA.*

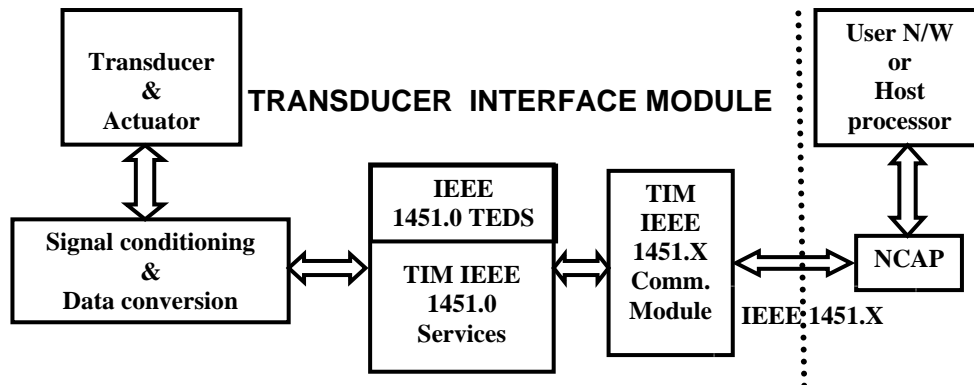
**Keywords:** Estimator, FPGA, Synthesis, Transducer interface model, Transducer electronic data sheet

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### 1. Introduction

IEEE 1451.0 2007[1] is the IEEE standard for a Smart Transducer Interface for Sensors and Actuators. It includes certain Common functions, Communication Protocols and Transducer Electronic Data Sheet (TEDS) Formats. Use of IEEE 1451 Standard reduces the complexities in establishing digital communication with transducers and actuators. The standard defines the bus architecture, addressing protocols, wiring, calibration and error correction and enables a building block approach to system design with plug-and-play models.

The main functional blocks, the Transducer Interface Module (TIM) and the Network Capable Application Processor (NCAP) which communicate through any IEEE 1451.X interface. A generalized TIM structure is shown in Fig. 1.



**Fig. 1.** General TIM structure.

It consists of transducer and actuator interface with necessary signal conditioning and data conversion, TEDS structure, TIM service block and the TIM communication module. The normal activities carried out by TIM are listed as follows:

- Execution of commands specified in the IEEE 1451 standard
- Enabling and controlling analog and digital interfaces and other peripherals.
- Accessing and updating of TEDS data
- Accessing and processing of actuator and sensor signals.
- Providing a reliable and accurate information

Several architectures have been developed for the implementation of Smart Transducer Interface Module (STIM) and TEDS based on IEEE1451.2 using microprocessors and microconverters [2-5]. Y. Wang and et. al have formed the TEDS with online calibration and global access of STIM through internet [2]. A health management system for sensors through self diagnostic is developed using IEEE 1451 standard for a rocket system by John Schmalzel and et. al. [3]. Lee and Y. Song developed an object oriented application framework for IEEE 1451.1 standard with reference implementations applicable to a waste water treatment system [4]. A. Depari and et. al described a VHDL Model of an IEEE 1451.2 smart sensor embedded in a single chip with Universal Serial Bus [5]. Microconverter ADuC812 have been used to implement the STIM accessed through the graphical user interface of NCAP [6]. Low cost Internet enabled smart sensors [7] and networked sensor prototype integrated with standardized CAN bus interface [8, 9] have been developed using microcomputers and microconverters.

The Transducer Independent Interface (TII) [10] has the drawback of 10 wire serial connection. The recent version of IEEE 1451 standard developed in the year 2007 facilitates the user to choose any standard interface like serial peripheral interface, USB etc. Based on the TIM structure new architectures arrive for the purpose of smart readout [11]. A novel architecture is proposed in this paper for smart sensors based on 2007 standard with appropriate user defined component module to enhance the system performance. The architecture proposed in this paper introduces a user defined TEDS structure along with additional user defined service module to enhance the performance of the readout.

A complete description of the TEDS is illustrated in the following section II. The proposed architecture with all its component modules is illustrated in section III. The details of command

generation between NCAP and TIM are illustrated in section IV. Section V illustrates a design example of an electrical network to demonstrate the features of the proposed readout. Section VI provides a synthesis report on implementation of smart readout on a FPGA platform. Section VII concludes with advantages of the proposed architecture and applicability.

## 2. Transducer Electronic Data Sheets

TEDS is a set of non volatile memory locations used to store information about sensors and actuators. The information includes calibration data, make and part number, tolerance, sensitivity, history, timing characteristics etc. The use of TEDS provides the following features [12].

- Elimination of manual configuration
- Reduction in time for configuration
- Better storing and tracking of electronic data sheets
- Improved accuracy in calibration
- Identification of sensor location through global connectivity

The TEDS can also be located in other parts of the user system, in case it is not possible to accommodate within the TIM structure. Such TEDS are called virtual TEDS. As a general rule, TEDS is not changed once the manufacturer or the user establishes the contents of TEDS. However, it is possible to design Transducer Channels that can change the contents of a TEDS during operation, by making the TEDS attribute bit as adaptive. TEDS are formed according to Type/Length/Value (TLV) data structure specified in the standard. Type is used to identify the field, Length indicates the number of octets in TEDS, and Value provides the TEDS information. Four TEDS are required for all TIMs and others are optional. TEDS formation is shown for a current sensor. They are detailed as follows.

Meta-TEDS: It gives some worst-case timing parameters to set time-out values in the communication software to determine when the TIM is not responding. It is stored in a memory of size 320 bits (Table 1).

**Table 1.** Meta TEDS – 320 bits.

00 00 00 22	Length
03 04 00 01 01 01	META TEDS Identifier
04 0A 81 C0 F9 74	UUID
48 82 1D C2 2E 78	
0A 04 3F 00 00 00	Time out operation 0.5 seconds
0C 04 C0 A0 00 00	Self-test time out operation 0.5s
0D 02 00 02	No. of transducer channels
F8 FA	Check sum

Transducer Channel TEDS: It gives detailed information about a specific transducer regarding the physical parameter being measured or controlled, the operating range, characteristics of digital I/O, operating modes and timing information. It occupies a memory space of 768 bits (Table 2).

User's Transducer Name TEDS: It provides a place for the user of the transducer to store the name by which the system will know the transducer.

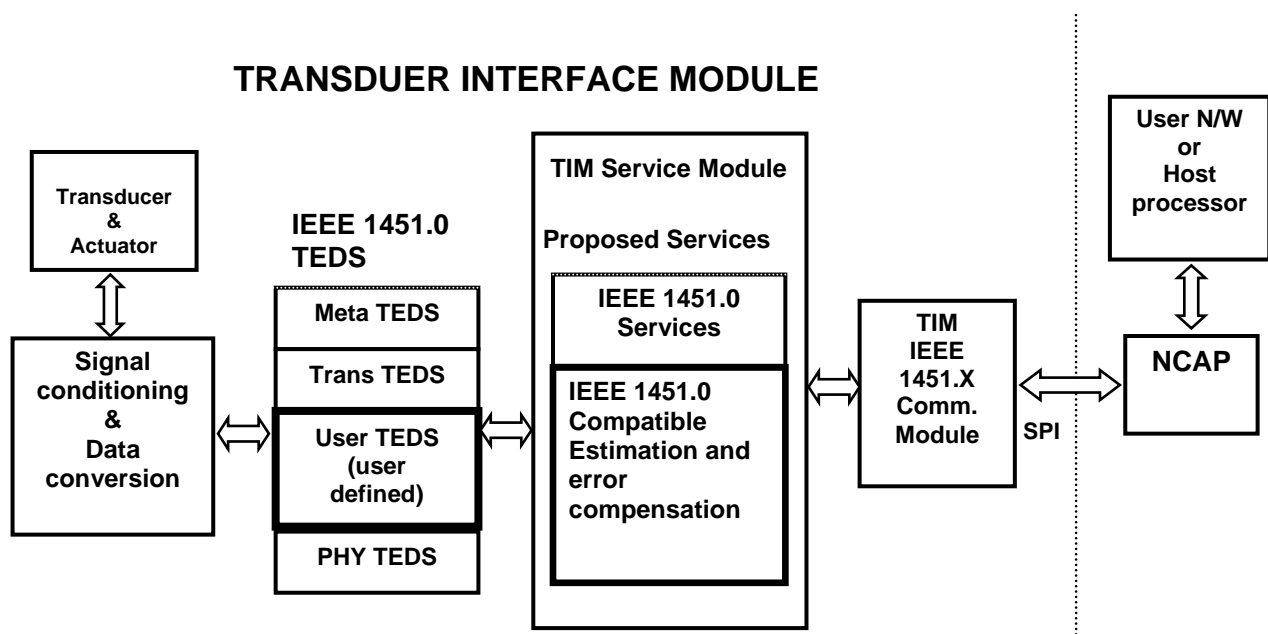
PHY TEDS: It is dependent on the physical communication media used to connect the TIM to the NCAP and is not defined in the standard although the method of accessing it is defined.

**Table 2.** Transducer Channel TEDS – 768 bits.

00 00 00 5F	Length
03 04 00 03 01 01	Transducer channel TEDS Identifier
0B 01 00	Calibration key
0C 06 32 01 00 38 01 80	Physical units
0D 04 F1 F8 00 00	Design operational lower limit -9A
0E 04 71 F8 00 00	Design operational upper limit +9A
0F 04 44 C0 00 00	Worst case error +/-5
10 01 00	No self test
12 09 28 01 00 29 01 01 2A 01 08	Sample definition 8-bit ADC
14 04 3D CC CC CD	Update time – 10 samples/s
16 04 37 D1 B7 17	Read set-up time – 25 $\mu$ S
17 04 3D CC CC CD	Sampling period – 0.1S
18 04 41 F0 00 00 19 04 37 D1 B7 17	Warm-up time – 25 $\mu$ S
1A 04 00 00 00 00	Self test time – 0S
1F 03 30 01 02	Sampling mode – immediate
EE 31	Check sum

### 3. Proposed Architecture for TIM

The proposed architecture is shown in Fig. 2, which includes a processor to perform IEEE 1451.0 services and IEEE 1451.0 compatible user defined and restructured required number of TEDS. The proposed architecture considers the sensors, actuators and the system as a whole than considering the sensors/actuators alone. The model of the system is incorporated along with the sensor and actuator information in this smart interface module. The newly proposed service provider makes use of the system information and estimates unmeasured and measured states to provide additional information.



**Fig. 2.** TIM Structure with Disturbance estimation.



Appropriate use of generated information leads to improve sensor measurement and system performance. The novelty of the architecture lies in the use of existing command and register structures to provide additional function to achieve in improved reliability. Highlighted blocks of proposed TIM architecture are redefined as detailed in Fig. 3.

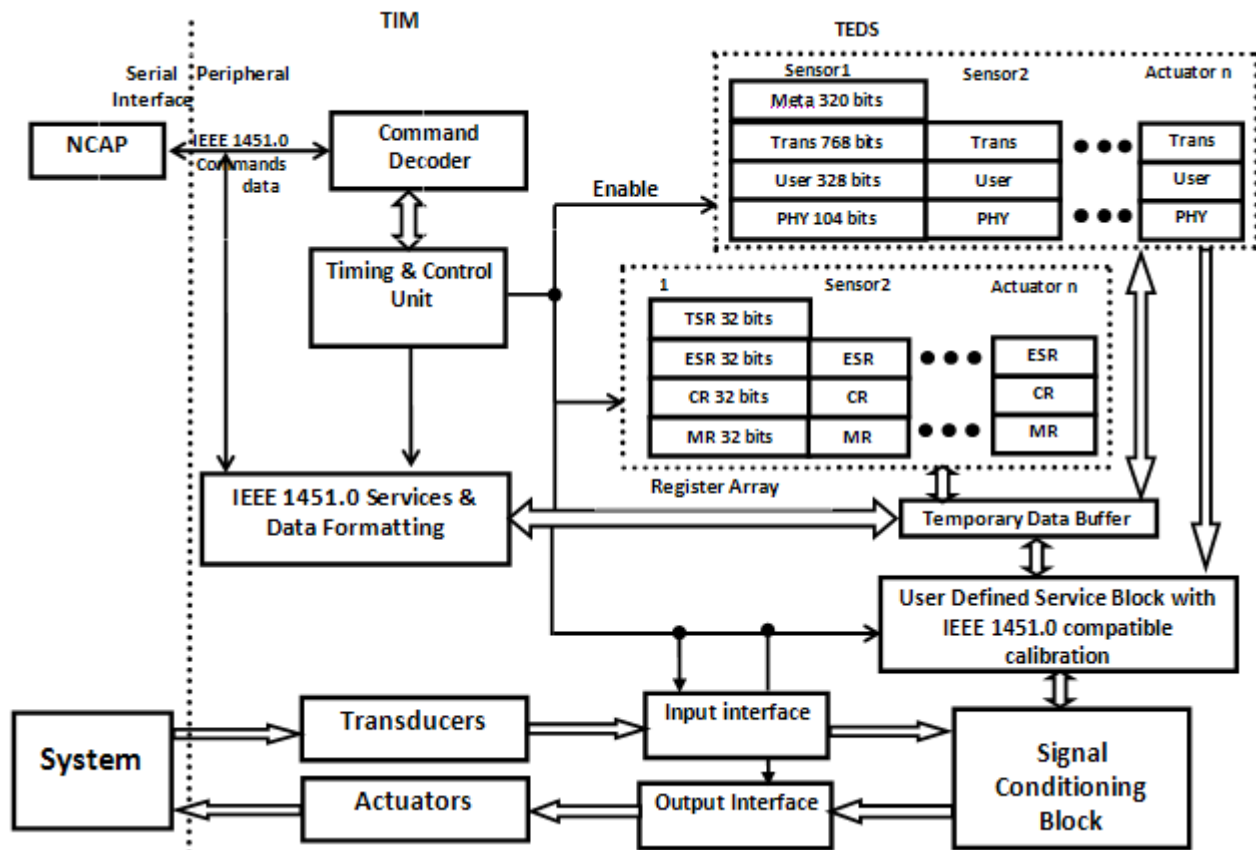


Fig. 3. Redefined TIM Architecture

### 3.1. Command Decoder and Status Registers

The architecture ensures processing of commands with appropriate time tags through command decoder and Timing and Control unit. The commands are of 56 bits in length as per the IEEE 1451.0-2007 standard received serially from a user network or host processor. The command message structure is grouped into octets consists of 8 bits. Totally there are seven octets, out of which two are reserved for destination transducer channel number, one for command class, one for command function, two for the length of command message and the final is command dependent octet in this application. The control function allows commands to be sent to the TIM as a whole or to each Transducer Channel. All unimplemented commands lead to the setting of the TIM invalid command bit in the status register. The commands and the data are transferred through the din and dout lines of Serial Peripheral Interface as shown in Fig. 3. Serial bits received in din are checked for a valid command, accordingly further triggering of a sensor or accessing TEDS/data's are carried out. Various registers used in the architecture are TSR – TIM Status Register, ESR – Event Status Register, CR – Condition Register, and MR - Mask Register. All registers are 32 bit wide and the status registers shall be implemented for each transducer. Condition register contains the current state of the attributes being reported. Status event register provides information about the validity of commands, hardware error, service request, change of TEDS, calibration and self test of transducers. Both registers can be accessed by read command and the contents are updated after each command execution. The TIM shall

contain a service request mask register for the TIM and for each sensor/actuator connected to it. The service request bit positions correspond one-to-one with the bit positions in the status event register.

### 3.2. User Defined TEDS

As per the standard the user defined TEDS can be of any length which suits the proposed architecture. The parameters of the system are stored in this module in state space form. In the proposed TIM structure the elements of F, G, L and C given by equations 1 and 2 are stored in User Transducer Name TEDS (Table 3).

**Table 3.** User Transducer Teds – 328 bits.

00 00 00 13	Length
03 04 00 0C 01 01	User transducer TEDS
04 0A 00	Identifier
10 00 F9 99 03 33 06 66	<i>User defined System</i>
06 66 00 00	<i>Parameters F, G ,L, C,</i>
D8 00 1B 33 22 8F	<i>and G<sub>d</sub></i>
00 00 10 00	
10 00 10 00	
FB 12	Check sum

### 3.3. Estimation and Error Compensation

The proposed architecture consists of a standard state estimator [13] along with decision making block to provide suitable compensation. Let the system be considered in Linear Time Invariant form represented by the following equation.

$$x_{k+1} = Fx_k + GU_k + G_d w_k \quad (1.1)$$

$$Y_k = Cx_k \quad (1.2)$$

$u_k \in \mathbb{R}^m$ ;  $w_k \in \mathbb{R}^{m^1}$ ;  $x_k \in \mathbb{R}^n$ ; and  $Y_k \in \mathbb{R}^p$ ; are the control input, unknown input, state and output of the system respectively. Let F, G, G<sub>d</sub> and C be compatible constant real matrices. Estimator can be configured to estimate all unmeasured states and also unknown inputs including disturbance whose model is known, using equation (2) and (3). Let the  $x_{dk}$  be the augmented state to estimate unknown input or disturbance  $w_k$ .

$$\begin{bmatrix} x_{k+1} \\ x_{dk+1} \end{bmatrix} = \begin{bmatrix} F & G_d \\ 0 & F_{dd} \end{bmatrix} \begin{bmatrix} x_k \\ x_{dk} \end{bmatrix} + \begin{bmatrix} G \\ 0 \end{bmatrix} U_k \quad (2.1)$$

$$Y_k = \begin{bmatrix} C & 0 \end{bmatrix} \begin{bmatrix} x_k \\ x_{dk} \end{bmatrix} \quad (2.2)$$

The estimated states provide information about the system, which can be appropriately used to modify the sensor and actuator information.

$$\hat{x}_{k+1} = F\hat{x}_k + G_d\hat{x}_{dk} + GU_k + L_1(Y_k - \hat{Y}_k) \quad (3.1)$$

$$\hat{x}_{dk+1} = F_{dd}\hat{x}_{dk} + L_2(Y_k - \hat{Y}_k) \quad (3.2)$$

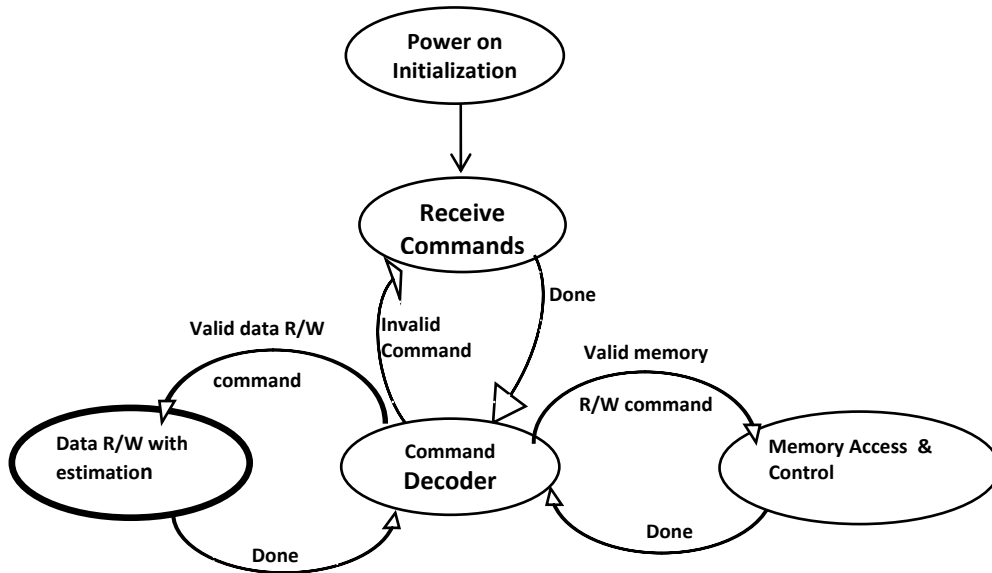
$$\hat{Y}_k = C\hat{x}_k, \quad (3.3)$$

where  $F_{dd}$  and  $L = \begin{bmatrix} L_1 \\ L_2 \end{bmatrix}$  are appropriately chosen for the defined model of disturbance and error for convergence. L matrix is chosen such that  $\begin{bmatrix} F & G_d \\ 0 & F_{dd} \end{bmatrix} - \begin{bmatrix} L_1 \\ L_2 \end{bmatrix} \begin{bmatrix} C & 0 \end{bmatrix}$  has all its eigen values inside unit circle [14].

This completes the definition of all the blocks of TIM.

#### 4. Commands Issued Between NCAP and TIM

The state flow diagram of the TIM is shown in Fig. 4. The commands are received from NCAP and stored in a temporary data buffer to check for validity. Valid commands are decoded to provide control signal for various blocks. After executing a command, the TIM enters receive mode again to accept next command. The user defined service routine for estimation and error correction is incorporated by modifying data read/write block.



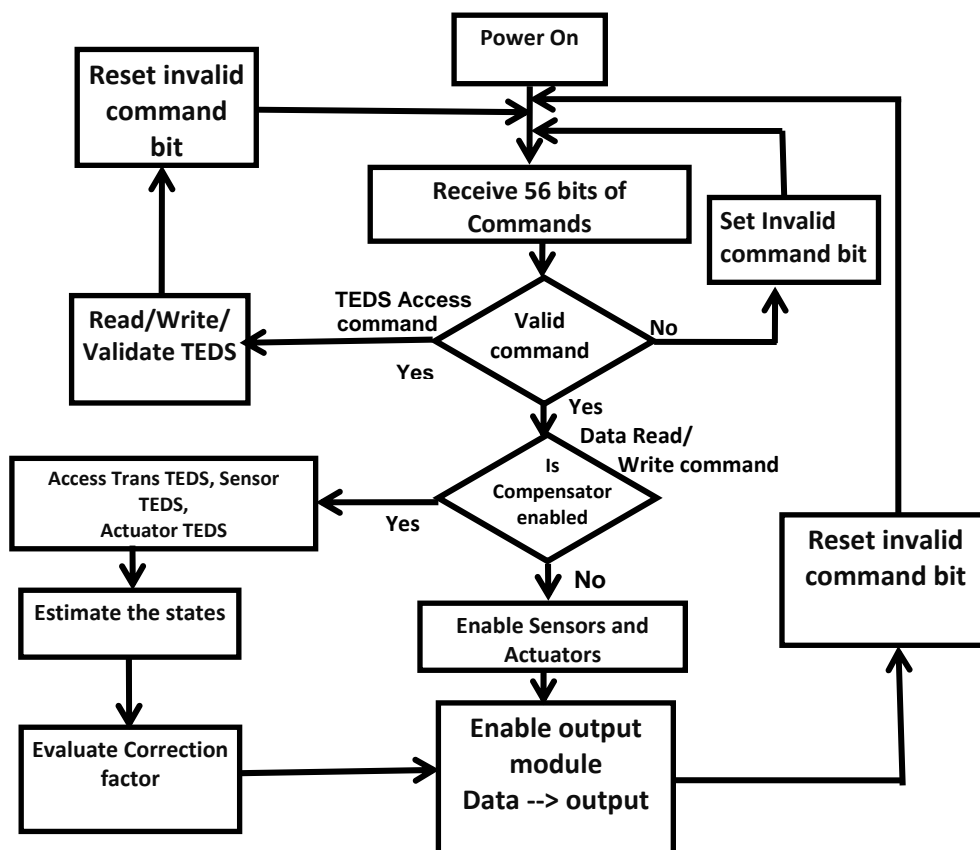
**Fig. 4.** State flow Diagram.

The proposed architecture is programmed to perform the required commands, with five command classes, and totally 17 commands subclasses. Table 4 illustrates the commands implemented in the proposed architecture.

The flow chart representation is shown in Fig. 5, in which the proposed user defined service routine is invoked every time a valid data read/write command is evoked.

**Table 4.** Commands Implemented in the Architecture.

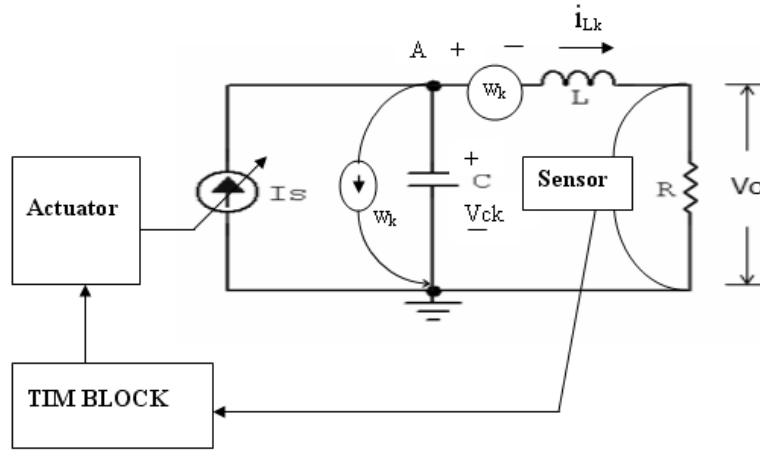
Standard Command classes	Execution of Commands
CommonCmd (Common commands)	Query TEDS, read TEDS, write TEDS, read service request mask, write service request mask, read status event register, write status event register, clear status event register.
XdcrIdle (Transducer Idle State)	Address Group definition
XdcrOperate (Transducer Operating state)	Read Transducer channel data-set segment.
XdcrEither (Transducer either state)	Transducer channel operate, Transducer channel idle, Read transducer Channel trigger state.
TIM Active (TIM Active state)	Read TIM version, Store operational setup, Read IEEE1451.0 Version, Recall operational setup,



**Fig. 5.** Flow chart.

## 5. Simulation

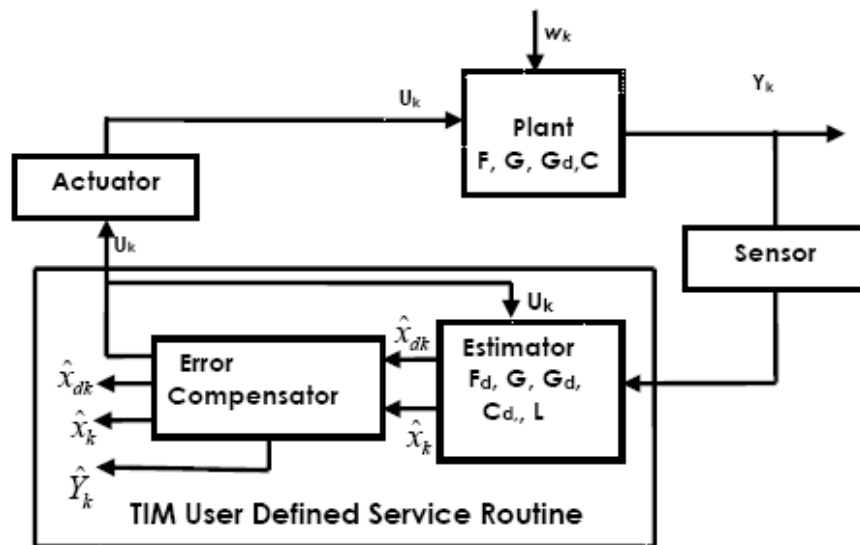
A second order system [15] shown in Fig. 6 is chosen to illustrate the working of the proposed algorithm. The inductor current and capacitor voltages are the state variables of the system. The input current  $I_s$  is varied through an actuator and output voltage across is measured by sensors, which are connected to the TIM through signal conditioning and Data conversion blocks. The disturbance enters the circuit in the form of a current injected at node A and voltage injected in the path of the inductance of same magnitude.



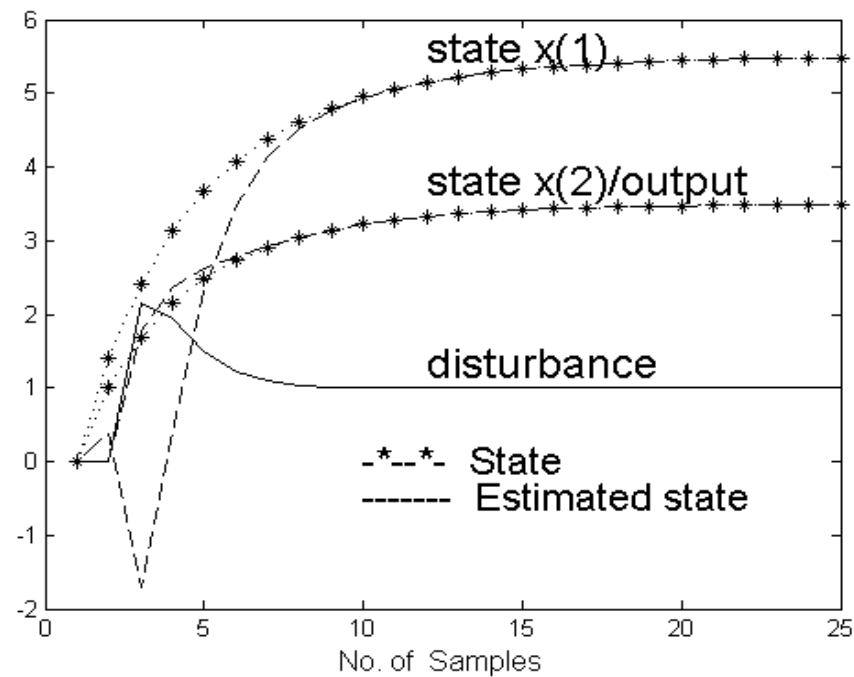
**Fig. 6.** RLC Network with  $R = 3\Omega$ ,  $L = 1H$ ,  $C = 0.5F$ , the corresponding  $F$ ,  $G$ ,  $G_d$  and  $C$  are given by

$$F = \begin{bmatrix} 1 & -0.4 \\ 0.2 & 0.4 \end{bmatrix} \quad G = \begin{bmatrix} 0.4 \\ 0 \end{bmatrix} \quad C = [0 \quad 1] \quad G_d = \begin{bmatrix} 1 \\ 1 \end{bmatrix}$$

The TIM structure applicable for system shown in Fig. 6 is described in Fig. 7. A disturbance of constant magnitude enters the system. The convergence of estimation error is ensured with the choice  $L = [-2.5 \ 1.7 \ 2.16]$ . The estimated states and disturbances simulated using MatLab software is shown in Fig. 8.



**Fig. 7.** Estimator block diagram.



**Fig. 8.** Estimator output.

## 6. FPGA Implementation

The architecture shown in Fig. 3 is synthesized with Xilinx Virtex II Pro FPGA. The synthesis reports are presented for TIM including the three blocks namely command decoder, TEDS storage and user defined service routine namely estimation and error compensation block.

### 6.1. Estimator

All data are represented in 2's complement 16-bit fixed point format with 4 bits for integer part and 12 bits for fractional part. The output is truncated to 16 bits with 8 bits for integer part and 8 bits for fractional part, as the algorithm is having repeated addition and multiplications. The hardware requirements of the estimator are shown in Table 5.

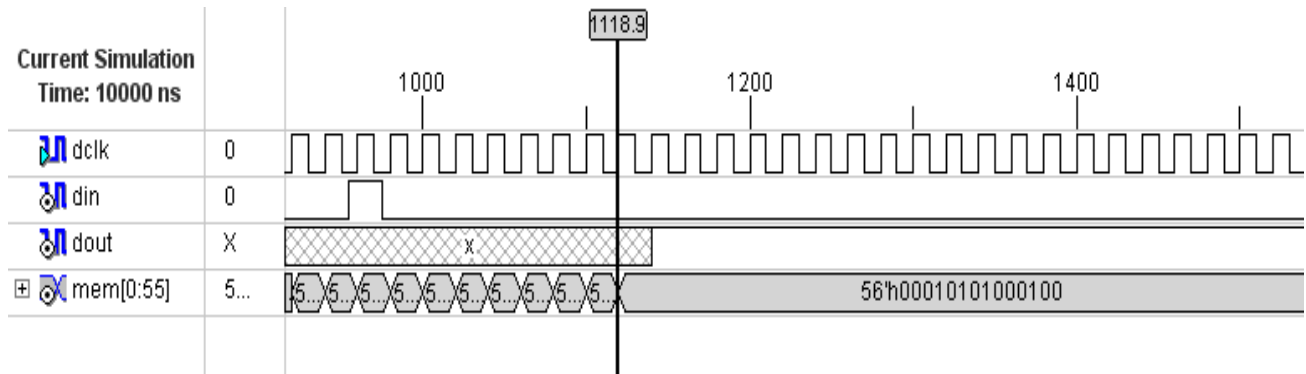
**Table 5.** Hardware Requirements of Estimator.

Counters and Registers	Arithmetic Blocks
32 Bit up counter ----- 1 No.	16 X16 Multipliers ----- 4 Nos.
16 Bit register ----- 4 Nos.	17 X 17 Multipliers ----- 3 Nos.
34 Bit register ----- 3 Nos.	32 Bit Adder ----- 2 Nos.
33 Bit Comparator less ----- 1 No.	33 Bit Adder ----- 2 Nos.
	34 Bit Adder ----- 5 Nos.

### 6.2. IEEE 1451.0 Service Routine

The simulation of the command in input line 'din', is shown in Fig. 9. The 56 bits Query TEDS command is shown in hexadecimal format. The contents of the query are placed on 'dout' line serially at the rising edge of each clock signal after receiving all the 56 bits.





**Fig. 9.** Simulation result for the command: Query TEDS.

### 6.3. Synthesis Report

The Design Entry, Synthesis, and Simulation are done using Xilinx tool [16], which produces the following synthesis report (Table 6). The architecture is synthesized in Xilinx Virtex II Pro FPGA [17] which features, flexible logic resources, dedicated 18 X 18 multiplier blocks, high performance clock management circuitry etc. The synthesis report shows that a maximum of 91 % of hardware is utilized to implement the architecture. The FPGA is capable of operating at higher sampling rates, which can be used for systems with wide bandwidth.

**Table 6.** Synthesis Report.

Device utilization summary			
Logic utilization	used	available	utilization
number of slices	2740	3008	91 %
number of slice flip flops	2904	6016	48 %
number of 4 i/p LUTs	4978	6016	82 %

## 7. Conclusion

This paper presented a novel method of utilizing the user defined TEDS and service routine for effective and accurate monitoring and control of the given system. The complete architecture and its implementation are discussed. The user defined services are obtained without violating the IEEE 1451.0-2007 standard and command formats. The architecture proposed is implemented in a FPGA platform for a chosen illustrated example, up to 17 sub commands are successfully implemented on Xilinx Virtex II pro FPGA with all the TEDS inclusive. However implementation of all the optional commands and optional TEDS may require use of additional external memory or higher version FPGA. Communication with other networks can be implemented by adding external interfacing circuit with NCAP, with that it is possible to read and display the TEDS over World Wide Web [18]. This methodology is suitable for high performance IEEE standard 1451.0-2007 based sensors.

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## Guide for Contributors

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### Aims and Scope

*Sensors & Transducers Journal* (ISSN 1726-5479) provides an advanced forum for the science and technology of physical, chemical sensors and biosensors. It publishes state-of-the-art reviews, regular research and application specific papers, short notes, letters to Editor and sensors related books reviews as well as academic, practical and commercial information of interest to its readership. Because it is an open access, peer review international journal, papers rapidly published in *Sensors & Transducers Journal* will receive a very high publicity. The journal is published monthly as twelve issues per annual by International Frequency Association (IFSA). In addition, some special sponsored and conference issues published annually.

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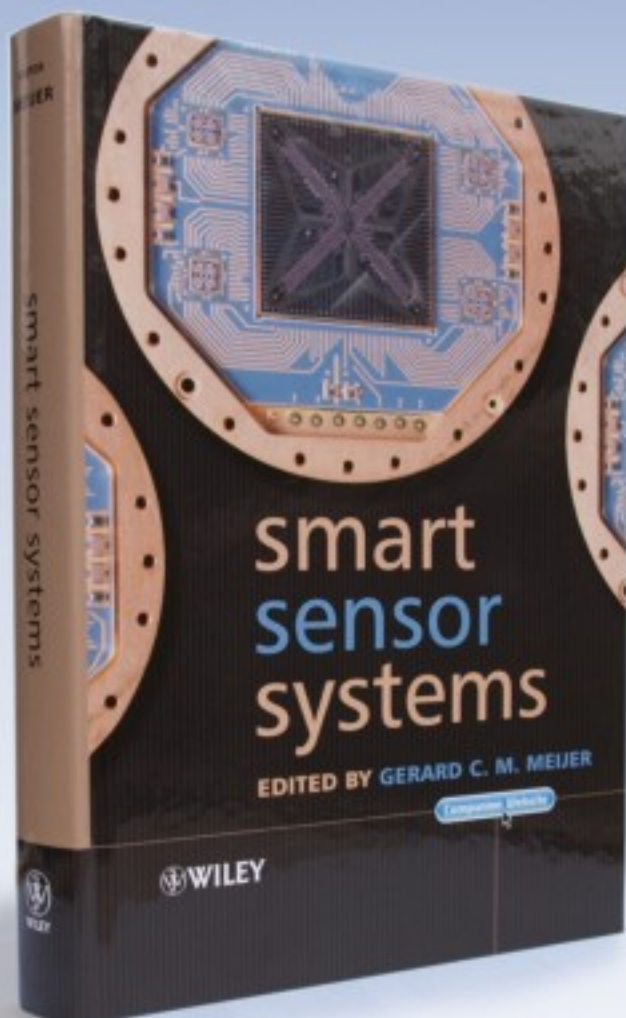
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