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Real Time In-circuit Condition Monitoring of MOSFET in Power Converters

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Abstract: This paper presents simple and low-cost, real time in-circuit condition monitoring of MOSFET in power electronic converters. Design metrics requirements like low cost, small size, high power factor, low percentage of total harmonic distortion etc. requires the power electronic systems to operate at high frequencies and at high power density. Failures of power converters are attributed largely by aging of power MOSFETs at high switching frequencies. Therefore, real time in-circuit prognostic of MOSFET needs to be done before their selection for power system design. Accelerated aging tests are performed in different circuits to determine the wear out failure of critical components based on their parametric degradation. In this paper, the simple and low-cost test beds are designed for real time in-circuit prognostics of power MOSFETs. The proposed condition monitoring scheme helps in estimating the condition of MOSFETs at their maximum rated operating condition and will aid the system designers to test their reliability and benchmark them before selecting in power converters.

Keywords: Accelerated aging test, In-circuit condition monitoring, Inverter, On-state drain source resistance, Unclamped inductive switching, Wear-out condition.

1. Introduction

Power electronic systems are used for various consumers, industrial and military applications. In recent times, accelerated aging tests are used in reliability domain and in semiconductor industry to estimate the expected lifetimes of the devices as well as to determine their operating conditions. Recently [1-2], the in-circuit condition monitoring of critical components of systems are done by using the sensors interfaced with on-chip analog to digital conversion (ADC) circuit of microcontroller based data acquisition systems and algorithms are implemented at host computer for signal conditioning and data logging. To prevent structural failure of the system, the real time embeddable prognostic techniques are employed that enables efficient, low cost and remote in-circuit condition based maintenance of systems. Failures of the power converters deployed for critical applications are attributed largely by parametric degradation of switching transistors [3-4]. Metal-oxide semiconductor field-effect Transistors (MOSFETs) are preferred switching transistors at high power density and high switching frequencies due to their low gate drive power, fast switching speed, low switching loss and superior paralleling capability. MOSFETs are selected based on their reliability and endurance data given in datasheet of manufacturer in power electronic system design. Their useful life actual in-circuit conditions are much

different than stated by manufacturer in the datasheet. It is assumed that the switching device can tolerate a maximum junction temperature (T_{jmax}) mentioned in datasheet but practically due to the localized hot spot temperature in MOSFET [5], the failure mechanism at the maximum junction temperature occurs faster that is verified in this paper. Thermal problems arise inside of the MOSET because it consumes power and transforms it into heat that decides its switching frequency [6]. Therefore, the real time in-circuit prognostics of MOSFETs need to be done before selecting them for power system design. Analysis for the aging process of switching transistors is done in based on the electrical stress based accelerated aging [7-8] and thermal stress based accelerated aging [9-10].

2. Characterization of Aging in MOSFET

Use of higher switching frequency reduces the size of reactive components both at filter and output stage. At the high power densities and high switching frequencies, MOSFETs are preferred switching device in different power converter circuits like PFC (power factor correction), Boost converter, Buck converter, DC choppers, inverter etc. The on-state drain source resistance (R_{dson}) is an important parameter to determine the wear-out condition of power MOSFET and its value increase with the aging of MOSFET [11]. Lower value of R_{dson} reduces the conduction loss in MOSFET and enables them to work at a lower junction temperature and therefore reduces the number of parallel MOSFETs in high power density applications [12].In this paper, parametric degradation at end of life or at wear-out condition is analyzed using accelerated aging for power MOSFETs in different operating conditions. For this purpose, the wear-out condition of power MOSFETs is determined by performing two different accelerated aging tests. In first test, a target MOSFET is subjected to the repetitive unclamped inductive switching at variable frequencies. In the second test a pair of power MOSFETs is operated at high power stress condition in half bridge inverter circuit. The proposed on-line condition monitoring technique will aid the system designers to test the reliability and benchmark MOSFETs before selecting them in system design.

3. Accelerated Aging of MOSFET Due to Repetitive UIS

The aging condition of target power MOSFETs is obtained by subjecting them to repetitive unclamped inductive switching (UIS) pulses. Equivalent circuit of power MOSFET consists of a parasitic BJT, a diode path in reverse direction across the main switch and stray capacitances between the junctions. Peak reverse current of body diodes in power MOSFET is much greater than that of the conventional diodes for the same operating conditions because the carrier lifetime in case of body diode is more than that for conventional diode so the reverse recovery time, t_{rr} for body diode is more as compare to fast recovery diodes. With the application of repetitive unclamped inductive switching (UIS) pulses, the avalanche energy in MOSFET causes the increase in the average power dissipation and junction temperature over a period of time. Due to increase of junction temperature the charge carriers in body diode increases up to a limit such that the parasitic BJT starts to conduct and cause failure of MOSFET. The aging process of MOSFET STP 7NK60Z due to repetitive unclamped inductive switching is analyzed practically by subjecting the repetitive UIS pulses to the MOSFET as shown in Fig. 1. Average power [13-14] for single UIS pulse is given by Relation (1),

$$P_S = 0.5 \times I_{pk}^2 \times L \times f_{SW}\,, \tag{1}$$

where, P_s is the average power for single unclamped inductive switching pulse, I_{pk} is the peak current, L is the inductance value; and f_{sw} is the switching frequency.

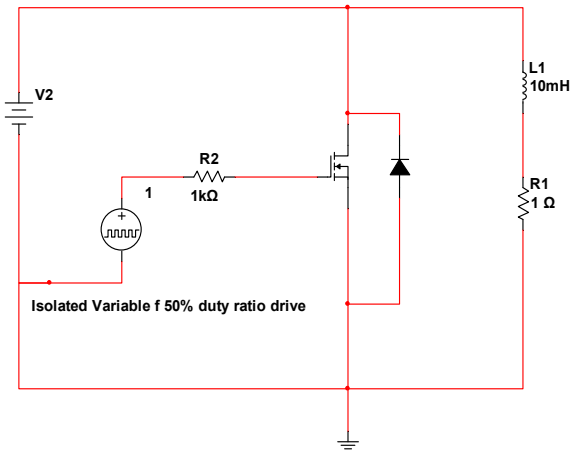

Fig. 1. Test bed for subjecting repetitive UIS to MOSFET.

Accelerated aging test of MOSFETs due to repetitive UIS pulses is conducted at the different switching frequency (4 kHz, 8 kHz, 10 kHz and 15 kHz) square pulses of 50 % duty ratio.The drain source current (I_{DS}) and voltage (V_{DS}) waveforms of test at the 4 kHz switching frequency is shown in Fig. 2 and Fig. 3.

The repetitive UIS pulse energy applied to MOSFET over a period of time will result in increase in the active power loss in MOSFET causing increase of junction temperature that is obtained by monitoring the case temperature [15] from Equation (2),

$$T_{j\max} = \mathrm{T}_{\mathrm{case}} + I_{DS} \times V_{DS} \times R_{\theta JC}\,, \tag{2}$$

where, T_{jmax} is the maximum junction to case temperature, T_{case} is the case (flange) temperature of the transistor, $R_{\theta JC}$ is the thermal resistance for the junction-to-case given in datasheet of STP 7NK60Z, I_{DS} is the drain-source current, and V_{DS} is the drain-source voltage.

I_{DS} and V_{DS} values are obtained experimentally using digital oscilloscope.

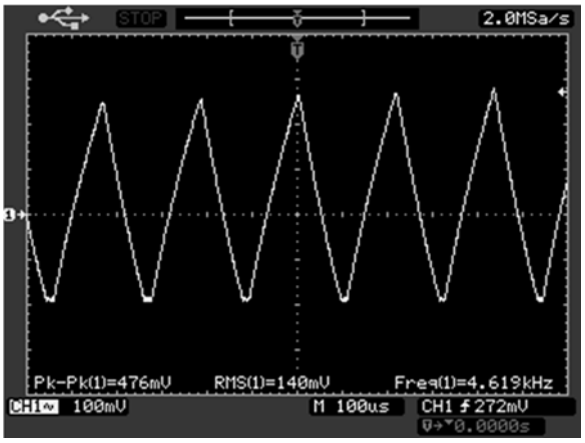

Fig. 2. I_{DS} at Repetitive UIS at 4 kHz.

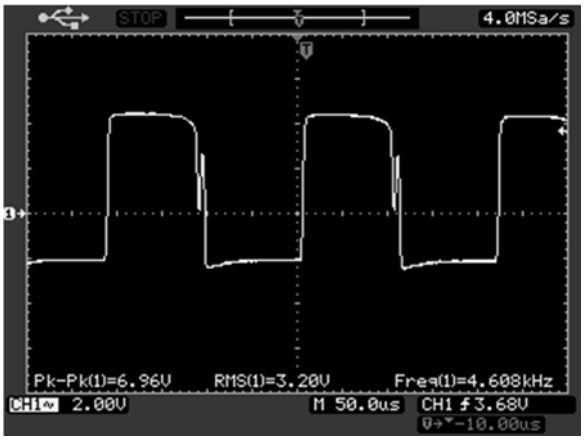

Fig. 3. V_{DS} at Repetitive UIS at 4 kHz.

Thermal data for the case temperature is acquired precisely using the linear integrated-circuit based centigrade temperature sensors LM35 and digital form of data values are acquired using on-chip ADC of the microcontroller. Data points are acquired after every minute by using delay loop programming in microcontroller. The temperature data values are logged by displaying them continuously on LCD and the values are stored as text file by serially transmitting them from microcontroller to the HyperTerminal application program of Windows installed on host computer. From the data arrays, the junction temperature as per Equation (2) is calculated for UIS pulses of different frequencies (4 kHz, 8 kHz, 10 kHz and 15 kHz) supplied to the MOSFET and the aging is done till the maximum rated junction temperature of 150 °C is obtained.The snap shot for implementation of simple and low cost real time monitoring of test parameters is shown in Fig. 4.

Fig. 4. Monitoring of Test Parameters.

From results of Table 1, increase in junction temperature occurs faster at low frequencies due to release of inductive energy through body diode during turn-off period. The test can similarly be done on power MOSFETs of other manufacturers of similar I_{DS}, V_{DS} and R_{dson} ratings to compare their reliability due to repetitive UIS at wear out condition.

Table 1. Accelerated Aging Results due to repetitive UIS for MOSFETs at different frequencies.

UIS Pulse Frequency	MOSFET-1 wear-out period (in min.)	MOSFET-2 wear-out period (in min.)
4kHz	21	23
8kHz	25	26
10kHz	32	30
15 kHz	43	41

4. Accelerated Aging Test of MOSFET Due to Power Stress

In this section, the wear-out condition of two MOSFETs, STP 7NK60Z is monitored at the output of half bridge inverter circuit. For this purpose a voltage fed half bridge inverter circuit is designed [16] with overload protection and isolated gate drive switching circuit as shown in Fig. 5.

Accelerated aging test (ALT) for the upper and lower leg power MOSFETs at high power stress condition is done using variable resistive load. The resistive load is reduced till both the MOSFET at upper and lower legs are subjected to high power stress. Inverted isolated gate drive pulses for both MOSFETs at the running state switching frequencies of 85 kHz are supplied using tiny family of AVR microcontroller. Rated maximum current I_{dsmax} for STP 7NK60Z is 5.2 A and blocking voltage is 600 V. Load is reduced till both the MOSFET at upper and lower legs are stressed to maximum rated drain

source current I_{DS} of 5.2 A and high drain source blocking voltage V_{DS} in order to monitor their wear-out condition.

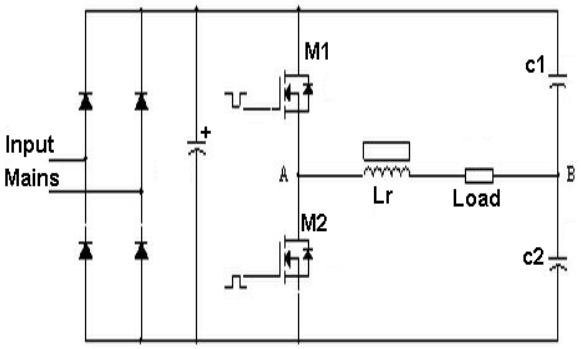

Fig. 5. Block diagram of Half Bridge Inverter Test Circuit.

Increase in Drain-Source current causes the increases the on state power loss [17] due to which the junction temperature and on-state drain source resistance $R_{dson}$of MOSFET increases as per Relation (3),

$$R_{dson}(\mathrm{T_J}) = R_{dson}(25^{o}\,\mathrm{C}) \times (1+\alpha/100)^{\mathrm{T_J}-25^{o}C}, \quad (3)$$

where, T_J is the Junction temperature; R_{dson} *(25 °C)* is the drain-source resistance at 25 °C given in datasheet; α is the temperature coefficient (calculated from two sets (T_{J1}, Rds_{on1}) and (T_{J2}, Rds_{on2}) from datasheet of STP 7NK60Z).

The junction temperature is obtained from Equation (2) by acquiring the case temperature using low cost microcontroller based data acquisition board and LM35 temperature sensor as shown in Fig. 4 in earlier section. Waveforms of for power stress of upper and lower leg MOSFETs at maximum rated current I_{DS} of 5.2 A and high $V_{DS}$is obtained on digital oscilloscope and is shown in the Fig. 6 and Fig. 7 respectively.

The initial (before aging) junction temperature calculated using Equation (2) is 138 °C. R_{dson} for both MOSFETs at the different junction temperatures over the aging period is calculated using Relation (3). From datasheet, maximum value of R_{dson} is 3.3 Ω. From the thermal variation of R_{dson} of MOSFETs, their wear-out condition is obtained at the maximum rated value of R_{dson}. ALT results for variation in R_{dson} for both lower and upper leg MOSFETs in half bridge inverter at the different aging intervals are given in Table 2. From results of Table 2, the wear-out condition for the lower leg MOSFET at half bridge inverter occurs faster for power stress aging test. After 4 hours of the accelerated aging test both of the MOSFETs arrives at their end of life condition.

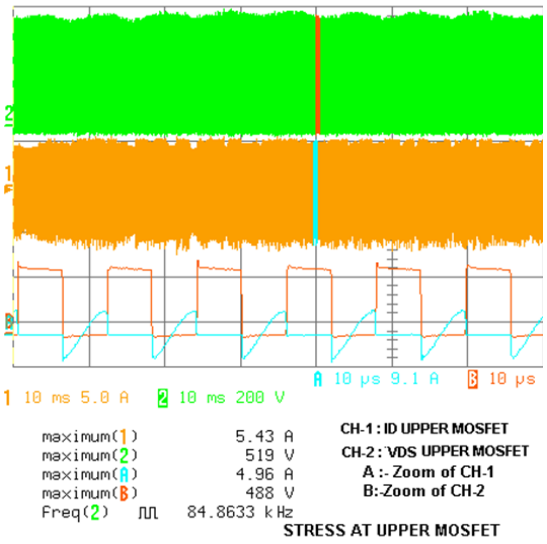

Fig. 6. High power stress aging for upper leg MOSFET.

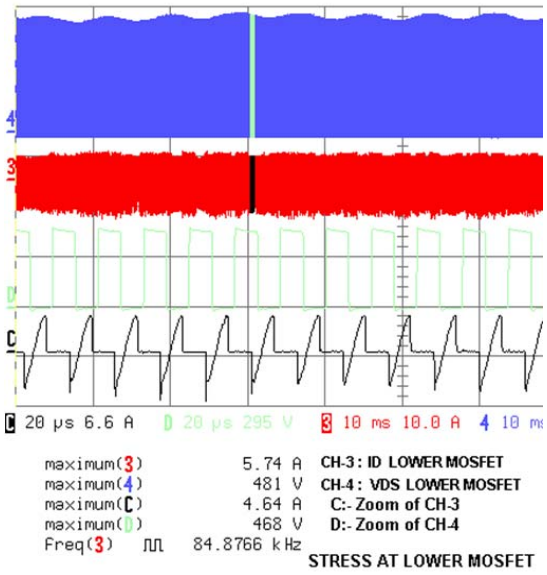

Fig. 7. High power stress aging for lower leg MOSFET.

Table 2. Accelerated Aging Results for MOSFETs under power stress condition in inverter circuit.

Aging test Period	Lower MOSFET R_{dson} (Ω)	Upper MOSFET R_{dson} (Ω)
1Hour	1.7	1.5
2 Hour	2.9	2.2
3 Hour	3.7	3.1
4 Hour	4.3	3.9

5. Conclusion and Future Work

As per MIL Handbook 217F, electrolytic capacitors and switching transistors together constitutes more than 90 % failures of power electronic systems.In this paper a simple and low

cost condition based monitoring technique are presented to characterize aging process of power MOSFETs in power converters. The wear-out condition for MOSFETsis obtained based on their parametric degradation.Wear-out condition of MOSFETs for aging due to repetitive unclamped inductive switching and also due to high power stress condition is presented. From the accelerated aging test due to repetitive UIS it is concluded that the increase in junction temperature occurs faster at low frequencies due to release of inductive energy through body diode during turn-off period. Same test can be done on power MOSFETs supplied by other manufacturer of similar ratings to determine and compare their repetitive UIS avalanche energy ratings at variable operating frequency in actual in-circuit condition. Also the wear-out condition for the two MOSFETs is monitored for half bridge inverter at high power stress condition. The proposed technique has the merits of using simple and low-cost methods to obtain parametric degradation for MOSFETsin different operating conditions. The scheme will alsohelp the system designers to test the reliability and practically benchmark the switching MOSFETs for their in-circuit operating conditions before selecting them in power electronic converters. The above technique can be implemented intelligently using sensor interfaced with low cost DAQ cards and supervisory control and data acquisition software (SCADA) like NI LabVIEW to monitor the in-circuit health of MOSFETs and alert the operator for wear out condition. Remote web based condition monitoring and circuit shut-down at end of useful life of device can also be implemented.

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