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Silicon-on-Insulator Lateral-Insulated-Gate-Bipolar-Transistor with Built-in Self-anti-ESD Diode

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Abstract: Power SOI (Silicon-On-Insulator) devices have an inherent sandwich structure of MOS (Metal-Oxide-Semiconductor) gate which is very easy to suffer ESD (Electro-Static Discharge) overstress. To solve this reliability problem, studies on design and modification of a built-in self-anti-ESD diode for a preliminarily optimized high voltage SOI LIGBT (Lateral-Insulated-Gate-Bipolar-Transistor) were carried out on the Silvaco TCAD (Technology-Computer-Aided-Design) platform. According to the constrains of the technological process, the new introduction of the N^+ doped region into P-well region that form the built-in self-anti-ESD diode should be done together with the doping of source under the same mask. The modifications were done by adjusting the vertical impurity profile in P-well into retrograde distribution and designing a cathode plate with a proper length to cover the forward depletion terminal and make sure that the thickness of the cathode plate is the same as that of the gate plate. The simulation results indicate that the modified device structure is compatible with the original one in process and design, the breakdown voltage margin of the former was expanded properly, and both the transient cathode voltages are clamped low enough very quickly. Therefore, the design and optimization results of the modified device structure of the built-in self-anti-ESD diode for the given SOI LIGBT meet the given requirements. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: Power SOI LIGBT, Built-in self-anti-ESD, Design and modification, Breakdown, Transient time.

1. Introduction

Power SOI (Silicon-On-Insulator) technology is well suitable for vehicle electronics, industry electronics and SPICs (smart power electronic systems) applications due to its advantages of fully dielectric isolation, compatibility with SOI BCD (Bipolar CMOS (Complimentary Metal-Oxide-Semiconductor) DMOS (Double-diffusion Metal-Oxide-Semiconductor)) technology and easy integration with low voltage SOI CMOS ICs (Integrated Circuits). Among the suitable SOI power semiconductor devices, LDMOS (Lateral-Double-diffusion Metal-Oxide-Semiconductor) and LIGBT (Lateral-Insulated-Gate-Bipolar-Transistor) are the most popular options. However, they have an

inherent sandwich structure of MOS gate, which is very easy to suffer charge from ESD (Electro-Static Discharge) charges and result in collapse of the devices. Therefore, on-chip built-in ESD protection structures should be considered and designed in-between SOI power device cells such as LDMOS, LIGBT and LMCT (Lateral Metal-Oxide-Semiconductor gate Controlled Thyristor).

It is well know that researches on on-chip ESD protection for varieties of low voltage ICs and SOCs (System On Chips) spanning a very wide frequency scope (S. Chen, et al. [1]; M. Ker, et al. [2]; M. Ker et al. [3]; Y. Hsiao, et al. [4]; Shih-Hung, et al. [5]; J. Park, et al. [6]; M. Ker, et al. [7, 8]; C. Yeh, et al. [9]; S. Dong, et al. [10]; X. Wang, et al. [11]; J. Liu, et al. [12]; X. Wang, et al. [13]; F. Ma, et al. [14] and M. Ker, et al. [15]).

In recently, some literatures by (X. Cai, et al. [16]), (L. Jiang, et al. [17]), (M. Ker, et al. [18]) and (J. Shu, et al. [19]) were reported on the applications of power SOI devices to ESD protection of high voltage power ICs. However, more and more attention has been being paid to the self-anti-ESD performance of integrated power SOI devices (H. Zhang, et al. [20]), (H. Zhang, et al. [21]), (H. Zhang, et al. [22]), (H. Zhang, et al. [23]).

To explore the way to improve self-anti-ESD performance of power SOI devices, H. Zhang, et al. began to put their shoulders to the wheel on exploring the feasible self-anti-ESD device structures of SOI LDMOS/LIGBT and their process compatibility with CMOS VLSI (Very technologies. As a preliminary result, a type of SOI LDMOS/LIGBT structure integrated with anti-ESD diode and its fabrication method in CMOS VLSI technology was reported in reference (H. Zhang, et al. [20]). After that, they took a try to transfer the lateral gate structure into a vertical one for lateral SOI power devices and tried to adjust their drain structures in order that they are featured of performance analogue to that of vertical ones.

Through studying and verifying by process and device simulations for a period of time, a novel SOI LDMOS and LIGBT with TGFPTD (a Trench Gate and Field Plate and a Trench drain) was proposed in turn (H. Zhang, et al. [24]), (H. Zhang, et al. [25]) and their fabrication feasibility was verified by process simulations with Silvaco TCAD tools (H. Zhang, et al. [26]), (H. Zhang, et al. [27]).

Based on the achievements mentioned above, by taking the vertical channel SOI LDMOS for example, a self-anti-ESD structure of TGFPTD SOI LDMOS was proposed, the positive and negative ESD discharging mechanisms of which were studied in details through process and devices simulations (H. Zhang, et al. [21]), (H. Zhang, et al. [22]), the simulation results of which (H. Zhang, et al. [21]), (H. Zhang, et al. [22]) indicate that multi-hybrid parasitic devices (maybe including diodes, BJTs (Bipolar Junction Transistors), MOSFET Metal-Oxide-Semiconductor Field Effect Transistor), SCRs (Silicon Controlled Rectifiers) and so on) take part in the HBM (Human Body Model) ESD discharging process and the induced gate voltage can be clamped under a safe limit in a very short time although the self-anti-ESD device structure was not optimized.

The results reported in references (H. Zhang, et al. [21]), (H. Zhang, et al. [22]) are applicative to the self-anti-ESD structure of TGFPTD SOI LIGBT since its device structure is analogue to the self-anti-ESD structure of TGFPTD SOI LDMOS except that an additional P^+/P anode region is added in the drain structure of the former, which makes the multi-hybrid parasitic devices more complicated and the self-ESD discharging easier.

On the basis mentioned above, the optimum design and verification on the characteristics of breakdown voltage and transient response of the built-in self-anti-ESD diode were focused in for an SOI LIGBT in this paper. Firstly, the initial condition of the SOI LIGBT was listed in details and the anticipant breakdown voltage and transient time of the built-in self-anti-ESD diode were defined. Then, the original device structure of the built-in self-anti-ESD diode was designed and verified by devices simulations with Atlas. After that, the modification of its structure was discussed based on the results above by considering the compatibilities of process and design. The obtained simulation result indicates its breakdown voltage was improved. At last, ESD transient response was measured by further simulations and the corresponding results were obtained.

2. Initial Conditions and Design Objects

An SOI LIGBT was designed and preliminarily optimized according to conventional design method and the assistant simulation with Atlas in advance, the parameters of which are summarized in Table 1 in details. The cross section view of the initial SOI LIGBT is illustrated in Fig. 1.

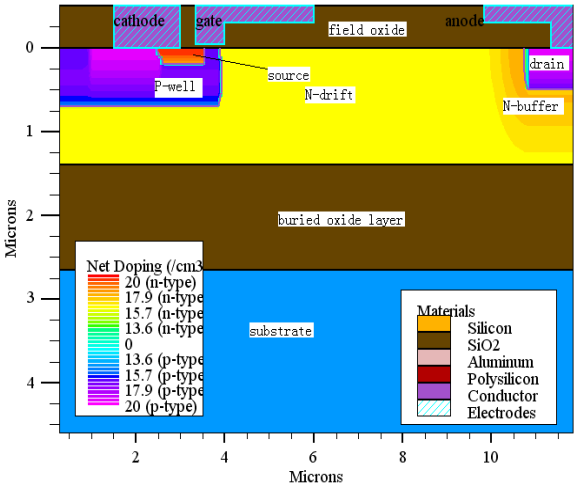


Fig. 1. Cross section view of the initial SOI LIGBT.

Table 1. The initial parameters of the SOI LIGBT.

Parameter (variable-definition)	Value	Unit
t_{BOL} -thickness of buried oxide layer	1.20	μm
t_{SOIF} - thickness of SOI film	1.40	μm
t_{GDL} - thickness of gate dielectric layer	40	nm
p_{PPW} - position of impurity concentration peak of p-well in Gauss distribution	0.40	μm
N_{PPW} - impurity concentration peak of p-well in Gauss distribution	3.0e17	cm^{-3}
X_{jpw} - junction depth of P-well	0.70	μm
N_S - impurity concentration of source region	1.0e20	cm^{-3}
X_{jS} - junction depth of source region	0.20	μm
N_{PPC} - impurity concentration of P^+ contact	5.0e19	cm^{-3}
X_{jPPC} - junction depth of P^+ contact	0.50	μm
N_{NB} - impurity concentration of N-buffer region	3.0e17	cm^{-3}
X_{jNB} - junction depth of N-buffer region	0.90	μm
N_{Ndr} - impurity concentration of N-drift region	1.0e16	cm^{-3}
L_{Ndr} – length of N-drift region	6.50	μm

All the parameters can be read out in Fig. 1 respectively. Based on the given structure and parameters, the electric properties of the SOI LIGBT were measured by simulation with Atlas. The measured results indicate that its threshold voltage is about 1.40 V and its breakdown voltage is about 101 V.

The gate oxide thickness of the SOI LIGBT is about 40 nm, which permits a voltage below 20 V applying between its gate and source terminals. In order to keep it from ESD overstress, at least one recoverable release bypath must be provided upon ESD stress. Therefore, an additional N^+ doped region was introduced into P-well region between two cathode regions of the most adjacent SOI LIGBT cells. The introduction of the additional N^+ doped region leads to the formation of a built-in self-anti-ESD diode and hence other hybrid parasitic device structures with the original material layers in the initial SOI LIGBT prototype. Since the SOI LIGBT structure is similar to that of SOI LDMOS except for an additional P^+/P-anode region, it was suggested in reference (H. Zhang, et al. [21]) that the hybrid parasitic devices except for MOSFET are only triggered after the self-anti-ESD diode is broken down during the electrostatic discharging process. Therefore, it is better to define the static breakdown voltage of the built-in self-anti-ESD diode higher than 10 V for an application of 5-10 V gate to source power supply. Besides, the maximum parasitic capacitance of the self-anti-ESD diode must be less than the gate capacitance of the SOI LIGBT so that the gate voltage can be clamped below 20 V in at least 10 ns.

3. Design of the Self-anti-ESD Diode

According to the constrains of the technological process, the new introduction of the N^+ doped region into P-well region should be done together with the doping of source region under the same mask. Therefore, the process control parameters of the phosphorus ion implantation must be the same as the doping of source region. As can be seen in Fig. 2 that the phosphorus impurities in source region abide by the Gauss distribution along vertical direction with a shallow junction depth, which should be the same as those in cathode region of the newly introduced self-anti-ESD diode. As a result, the virtual SOI LIGBT integrated with self-anti-ESD diode was fabricated by 2D process simulations and shown in Fig. 2. As can be seen in Fig. 2(a), an additional N^+ doped region is introduced into the previous P-well region next to the previous cathode.

In order to reduce the bulk peak field of the newly introduced self-anti-ESD diode, the doping of P-well adjusted as the retrograde doping process. Thus, the impurity profile of boron was improved to approximately comply with double ears-IV or united Gauss Pearson-IV distribution (H. Zhang, et al. [27]). Fig. 2(b) illustrates the doping profile of the self-anti-ESD region along vertical direction through its center. The non-linear V-shape vertical impurity distribution is benefit to elevate the bulk breakdown voltage of the self-anti-ESD diode to some extent.

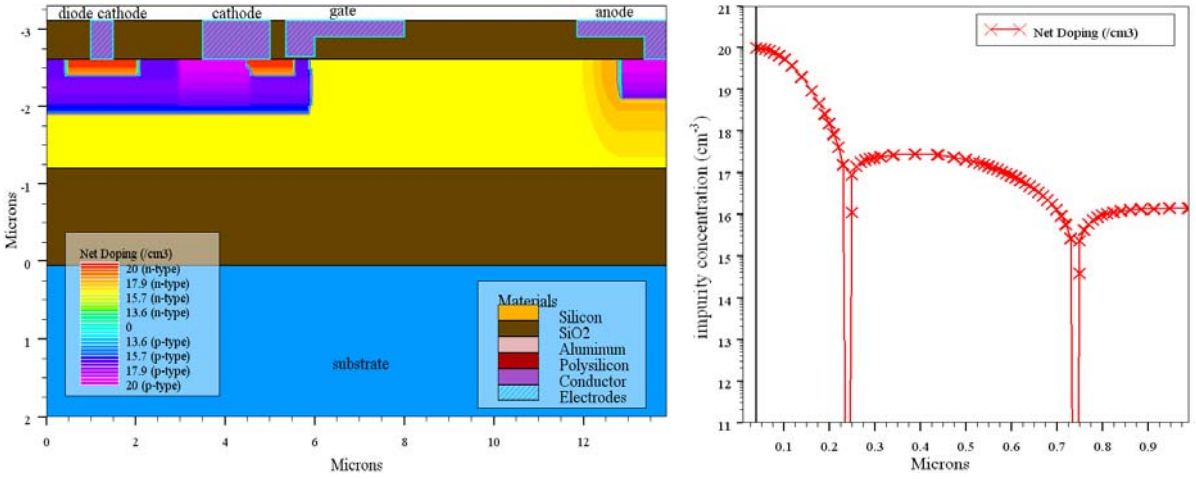
Since the anode of the self-anti-ESD diode is directly bypassed to cathode via P-well and P-well contact, the maximum parasitic capacitance of the self-anti-ESD diode might approximately equal to its potential barrier capacitance under the critical breakdown state.

$$C_D^{\max} \approx C_T^{br} \approx \frac{Q_{br}}{V_{br}} = \frac{\int_{x_{j0}(x,y)}^{x_{ju}(x,y)} S(x,y)dS}{V_{br}} \approx$$
$$\approx \frac{\int_{x_{ju1}(y)}^{x_{j01}(y)} S_1(y)dy + \int_{x_{j02}(x)}^{x_{ju2}(x)} S_2(x)dx + \int_{x_{ju3}(y)}^{x_{j03}(y)} S_3(y)dy}{V_{br}}, \quad (1)$$

where C_T^{br} is the potential barrier capacitance of the self-anti-ESD diode under the critical breakdown state, Q_{br} is the charge quantity in the depletion layer of the self-anti-ESD diode under the critical breakdown state and V_{br} is the static breakdown voltage of the self-anti-ESD diode, the integration domains of the first and the last integration terms among numerator lie in the sides of its depletion layer along vertical direction, and the 2nd term lies in the horizontal part of its depletion layer, while $S_1 \sim S_3$ represent the corresponding functions of integration elements. The gate capacitor C_g is composed of two capacitors in parallel, which are the gate oxide capacitor C_{go} and the gate plate capacitor C_{gp}, as can

be seen in Fig. 2 (a). The MOSFET is biased at V_{br} in a split second when the self-anti-ESD diode is broken down. Thus, the reverse channel is tied to the ground through source region.

Therefore, the gate oxide capacitor C_{go} and the gate plate capacitor C_{gp} might be considered as parallel plate capacitors approximately.



(a) cross section view

(b) impurity distribution of the diode

Fig. 2. The virtual SOI LIGBT integrated with self-anti-ESD diode.

$$C_g = C_{go} \,||\, C_{gp} = A_{go} C_{go} + A_{fo} C_{gp} \underline{\underline{W=1}} L_{go} \frac{\varepsilon_0 \varepsilon_{ox}}{t_{go}} + L_{fo} \frac{\varepsilon_0 \varepsilon_{ox}}{t_{fo}} = \frac{\varepsilon_0 \varepsilon_{ox} \left(L_{go} t_{fo} + L_{fo} t_{go} \right)}{t_{fo} t_{go}}, \quad (2)$$

where A_{go} and t_{go} are the area and thickness of the gate oxide layer, A_{fo} and t_{fo} are the area and thickness of the field oxide layer in the gate plate region, L_{go} and L_{fo} are the corresponding lengths of the gate oxide layer and field oxide layer in the gate plate region respectively, ε_0 is the dielectric constant in vacuum, and ε_{ox} is the relative dielectric constant of silicon dioxide.

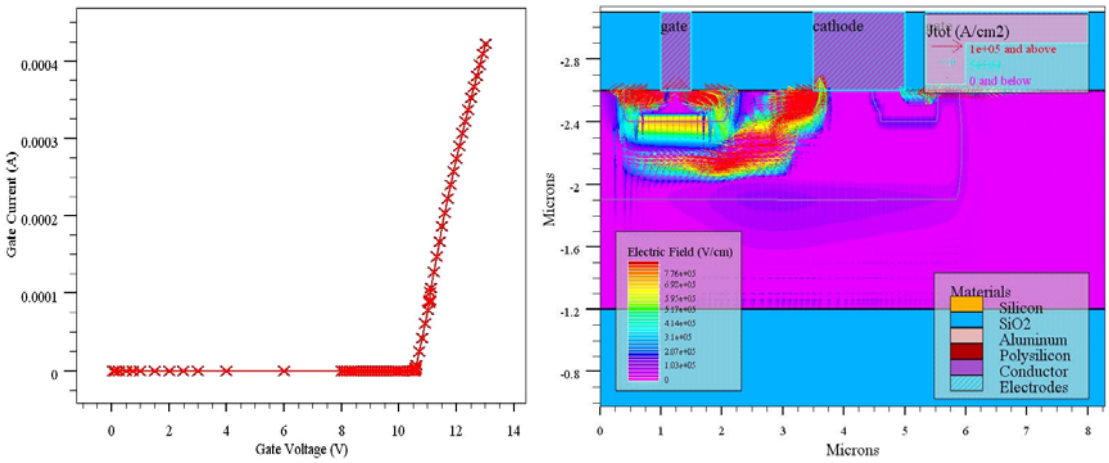
Once the self-anti-ESD diode is broken down under ESD stimulus (its current-voltage curve is shown in Fig. 3(a)), other related parasitic devices such as SCRs, BJTs will be triggered into on-state similar to that reported in references (H. Zhang, et al. [21]) and Fig. 3 (b) suggested, which provide at least one bypass branch with low resistance for gate charges releasing. For example, as can be seen in Fig. 3(b), a BJT+NMOSFET acts along the semicircle current flowing route, which consists of N^+(cathode of anti-ESD diode)/P-well(bottom)/N-drift/P-well(right side wall)/N^+(source region) and MOS gate and appears as a BJT and an NMOSFET in serials as the gate-source voltage is higher than its threshold voltage. Therefore, the induced gate voltage will be clamped in the safe range in a very short time in general.

As can be seen in Fig. 2 (b), the impurity distribution of the self-anti-ESD diode along vertical direction indicates that the PN junction of the diode is not an ideal abrupt PN junction and its static breakdown voltage will be a little higher than that predicted by the formula of ideal abrupt PN junction, which is about 9.50 V with average impurity concentration adopted. The offset is verified as about 1.10 V by device simulation as shown in Fig. 3(a), which is only a bit above the given static breakdown voltage limitation. That is to say, further improvements should be done to obtain a big enough margin.

4. Improving of the Self-anti-ESD Diode

As can be seen in Fig. 3(b), the current vectors concentrate on the interface between dioxide and the depletion region of the self-anti-ESD diode which indicate that electric field concentrate on the terminals of the self-anti-ESD diode, too. Therefore, to reduce the electric field on the terminals of the self-anti-ESD diode is very necessary in order to improve its breakdown voltage. By considering the compatibilities of process and design, it is a better choice to design a cathode plate for the self-anti-ESD diode.

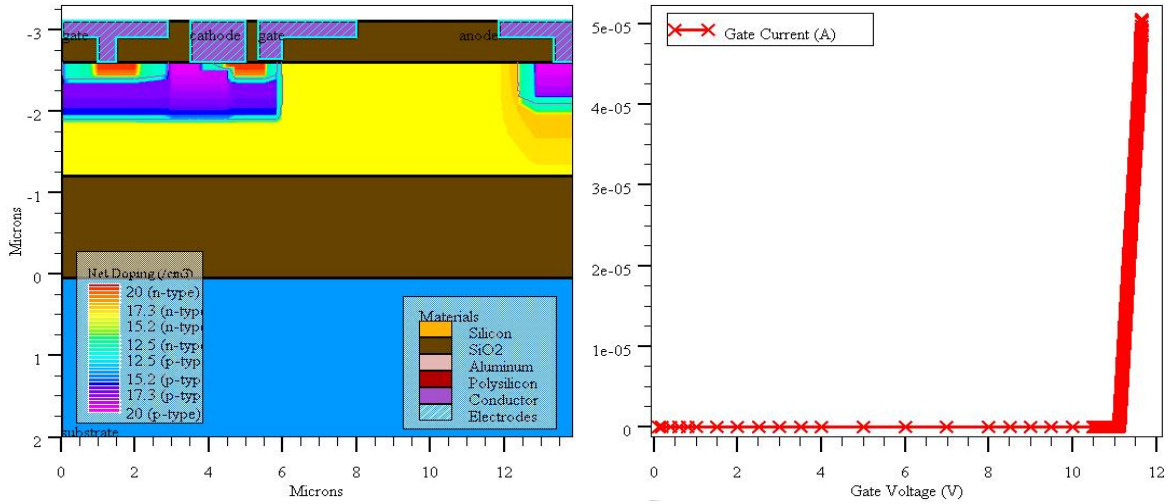
Fig. 4 illustrates the design results of its cathode plate structure and breakdown current-voltage curve.



(a) breakdown I-V curve

(b) electric field and current vectors

Fig. 3. Simulation results of the original self-anti-ESD diode in breakdown state.



(a) the modified structure

(b) the improved breakdown characteristic

Fig. 4. Simulation results of the modified self-anti-ESD diode.

As can be seen in Fig. 4(a), the cathode plate of the modified self-anti-ESD diode covers the forward depletion layer terminal of its PN junction, which relieves the electric field across the surface of depletion layer efficiently, hence removes the pre-breakdown on the surface of depletion layer. Fig. 4(b) indicates that its breakdown voltage is improved up to about 11.2 V, which is about 0.6 V higher than that shown in Fig. 3(a). The obtained result is an obvious improvement for the built-in anti-ESD diode since its process compatibility with the given SOI LIGBT on CMOS/BCD baseline has to be considered.

5. Simulation Results of ESD Transient

Fig. 5 illustrates the transient cathode voltage responses of the self-anti-ESD diodes to ESD stimulation, where the cathode was connected to the gate.

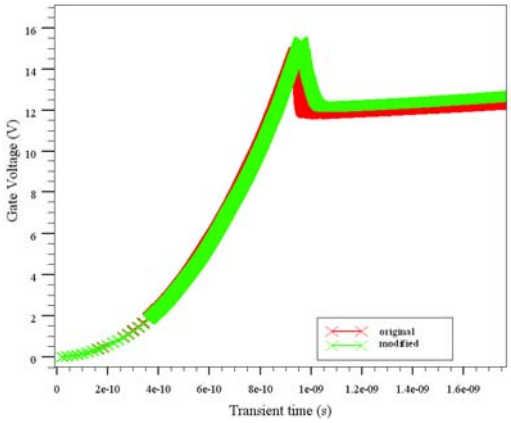


Fig. 5. The transient responses of the self-anti-ESD diodes to ESD stimulation.

As can be seen in Fig. 5, the cathode voltages of both the original and modified self-anti-ESD diodes are clamped below 16 V in a short time less than 1.0 ns, which correspond to the dynamic breakdown voltages of the self-anti-ESD diodes. Moreover, the dynamic breakdown voltage of the modified self-anti-ESD diode is a bit bigger than that of the original one, which is because that the introduction of the cathode plate leads to an increase of the static breakdown voltage of the self-anti-ESD diode. While the increment of the dynamic breakdown voltage equals to the increment of the static breakdown voltage approximately.

6. Conclusions

Based on the given SOI LIGBT structure parameters and process constrains, a built-in self-anti-ESD diode was designed and modified in turn according to the anticipated performance targets. Its structure was virtually fabricated and its electric properties concerned were measured by extensive 2D process and device simulations. The obtained results indicate that the modified device structure is compatible with the original one in process and design, the breakdown voltage margin of the former was expanded properly, and both the transient response times of its cathode voltage are less than 1 ns. Therefore, the design and optimization results of the modified device structure of the built-in self-anti-ESD diode for the given SOI LIGBT meet the given requirements. Therefore, the obtained results might be worth referring for subsequent researching and development.

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