Sensors & Transducers, Vol. 171, Issue 5, May 2014, pp. 250-255

Sensors & Transducers

Research on Multichannel Test Device of Missile Fuze

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Received: 21 May 2014 /Accepted: 30 May 2014 /Published: 31 May 2014

Abstract: This paper introduces the design of multichannel acquisition circuit based on FPGA which samples and records the Doppler signals, ignition signal and the working condition of fuze security enforcement agencies of missile fuze in real-time in the test of high speed dynamic intersection. Furthermore, for the problem of increasing number of sample channel which causes the complexity of the multiplexer control, a general programmable channel switching method is proposed based on FPGA. In the method, FPGA is the control core, and using the internal ROM resource effectively simplifies the complexity of channel switch in the multichannel acquisition system. This paper analyzes the acquisition system design, and describes the design of hardware circuit and analog switch address coding in detail. The test result shows that the acquisition circuit meets the design requirements with high sampling precision and application value. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: Missile fuze, Multichannel, FPGA, Switching method.

1. Introduction

In the missile dynamic intersection flight simulation test, usually test method is using the ground cable transmitting information, the tape recorder and telemetry technology. For the few test channels and low speed flight simulation test, the method of using the ground cable transmitting information can meet the experiment requirement. However, for the high speed flight experiment, due to the releasing speed and distance of cable, and the reliability reasons such as disturbances, broken line, it cannot be used. The tape recorder is being phased out gradually because of the complex operation and the mechanical system reliability [1-4]. Due to the high cost and test debugging complexity the telemetry is used on small tactical missile battle less. With the widely used of storage test technology which has many advantage such as high reliability, low cost, multichannel, large capacity, easy operation and so on, the solid state recorder is the best resolution for the test of missile fuze [5-7].

With the increasing performance of the missile, the test system is more and more complex and the number of test signal is also growing. In the high-speed dynamic intersection experiment, the Doppler signals, ignition signal and the working condition of fuze security enforcement agencies are needed to record in real-time. The more test channels are, the more complex the structure of the data frame is. The channel switch is mainly related to the order of input channel and the data frame. When the number of test signal is less and the structure of data frame is

simple, regulating the switch order of multiplexer or data frame can achieve multichannel acquisition. However, when the number of channel is many, the above resolution will undoubtedly increase the difficulty and complexity of the system design. Channel switch of multichannel acquisition system is becoming more complex. How to design of channel switching reasonably has become the key technology of the design of acquisition system. To solve these problems, we proposed a design of solid state recorder for the test of missile fuze. And for the requirement of multichannel test, a general programmable multichannel acquisition method is also proposed, which simplify the hardware design for the multichannel acquisition circuit. When the flight simulation test is finished, we recover the flight data from the recorder which is convenient for analyzing the cause of malfunction.

2. The Structure and Working Principle of System

The block diagram of acquisition and storage system is shown in Fig. 1. The system takes the 27 V pulse signal whose during time is 100 ms as the trigger signal. When the mixed signals go through the input interface, these signals are firstly regulated by the signal regulation module and are then transmitted to analog switch. Then, the analog signals are transmitted through analog switch that are sequentially controlled by the logic control module and sent to ADC. The FPGA stores the converted data into Flash memory. The recorded data is uploaded via USB after finishing the test. The system uses dry battery pack as the independent power supply, which avoids the need of power supply by missile and is convenient for interface design and installation.

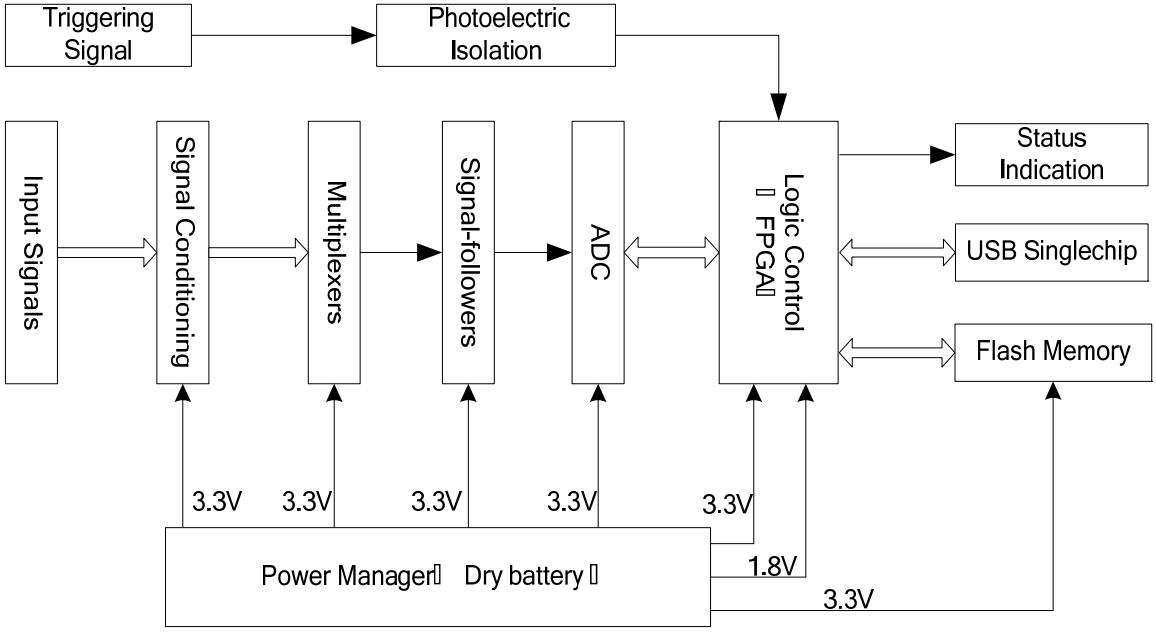


Fig. 1. The block diagram of acquisition and storage system.

3. The Design of Acquisition and Storage Module

After modulating by the operational amplifier, the modulated analog signals are outputted to analog multiplexer ADG732. And then FPGA control the address lines of ADG732 to switch in an order, so that the 80 analog signals can be orderly inputted into the analog-to-digital converter - THS1040. The output digital signal of AD-THS1040 is gathered by FPGA in 10 bit data length. In the FPGA, the sampled data will be framed as the data pack. The structure diagram of acquisition process is shown as the Fig. 2.

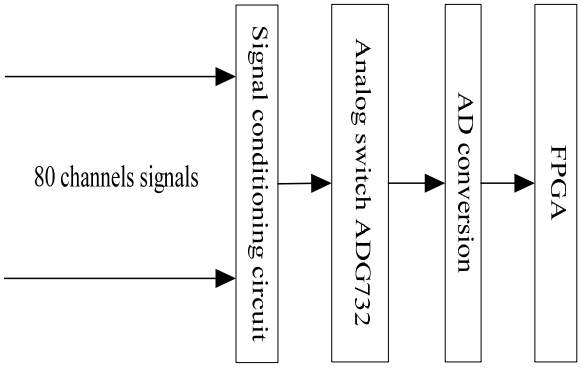
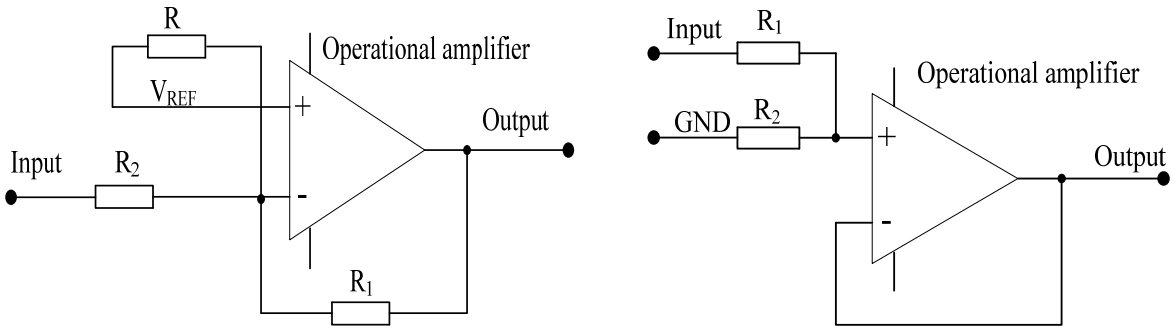


Fig. 2. The diagram of acquisition process.

3.1. Signal Conditioning

In the process of design, in order to guarantee the integrity and accuracy of signals before they are inputted to analog switch, we use operational amplifier with the character of rail to rail to modulate the signal. This design improves the input impedance of signal, and at the same time also reduces the output impedance of modulated signal. After modulating, all the high amplitude signals are processed uniformly into 0～2 V signals that are convenient for data sample. The -10 V ～ +10 V and -30 V ～ +30 V interface circuit is shown in the Fig. 3(a). The 0～+40 V, 0～+10 V interface circuit as shown in the Fig. 3(b). According to the different range of input, the value of R1 and R2 is different.



(a) (b)

Fig. 3. (a) -10 V~10 V and -30 V~30 V interface circuit, (b) 0 V~40 V and 0 V~10 V interface circuit.

In Fig. 3(a), the output V_{O1} is

$$V_{O1} = \left(1 + \frac{R_1}{R_2}\right) V_{REF} - \frac{R_1}{R_2} V_{I1} \quad (1)$$

In the Fig. 3(b), the output V_{O2} is

$$V_{O2} = \left(1 + \frac{R_2}{R_1}\right) V_{I2}, \quad (2)$$

According to the Eq. (1) and Eq. (2), the selection of R1 and R2 is shown in Table 1.

Table 1. The value of R1 and R2.

Input range	R1 (Ω)	R2 (Ω)
-10 V~+10 V	13 k	150 k
-30 V~+30 V	4.7 k	150 k
0~+40 V	120 k	6.2 k
0~+10 V	160 k	39 k

The operational amplifier is susceptible to the capacitive load in the unity gain configuration. To avoid the phenomena of oscillating, the resistor RX of 100 Ω can be inserted in the output of operational amplifier. The block diagram is shown in Fig. 4.

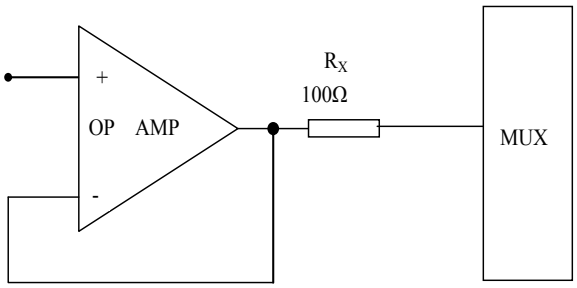


Fig. 4. The block diagram of the output of op amp.

3.2. General Programmable Channel Switching Method

The sample rate of each signal is different, so when data packing the hybrid frame is used with prime-frame and subframe. According the requirement of frame format, there is no regular switch between channels. The conventional method is regulating the order of multiplexer channels to meet the requirement of the sequential control of FPGA. However, when the number of signal channel is larger, the hardware design and the control of FPGA are more complex. So the conventional method is fit for the acquisition system with a few channels, not for the system with a large number of channels. Therefore, for the complex channel switch, we proposed a general programmable channel switching method. We encode all the switch addresses according to the frame format, and write them into the internal ROM of FPGA in advance.

When the acquisition system works, the addresses of channels are read out from ROM which is named addr_rom in Fig. 5 to control the group of multiplexers.

In the acquisition system, each sixteen-channel multiplexer contains four address gates (A3, A2, A1 and A0) and one enable signal (EN). Each enable signal of multiplexer uses one control line alone and all the multiplexers share the address lines. For the eighty channels acquisition system, five multiplexers are needed. So, nine control lines can determine a channel address, which is shown in Table 2.

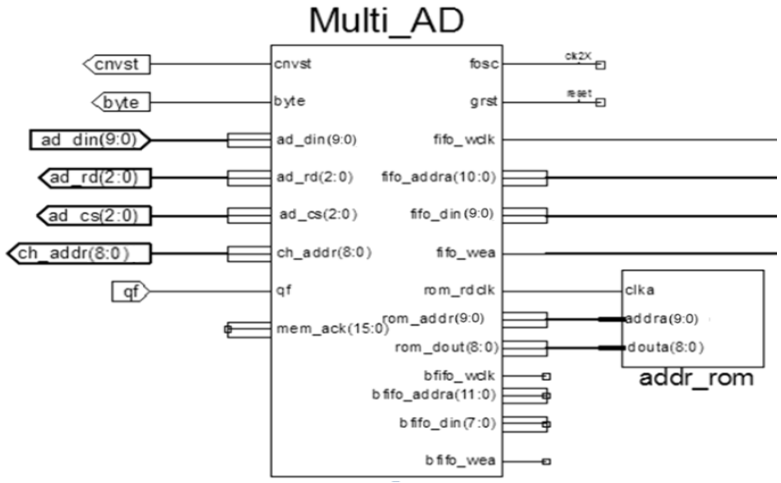


Fig. 5. The control of ROM in the FPGA.

Table 2. The corresponding relation of the multiplexer address.

9 bits of address								
The enable signals					Address gates			
EN4	EN3	EN2	EN1	EN0	A3	A2	A1	A0

The method realizes complete separation between the input signal channel and the frame format design. And the method is programmable, which can adjust the address code of ROM with the change of frame format. So, the method has generality. In the frame format, except the characteristic signal, one signal is according to one multiplexer address. The data frame format is 58×10. The characteristic data is 50, so the address number is 530. The data width of 9 bit and the depth of 1024 bit of the ROM in FPGA can meet the address control requirement.

3.3. Storage Module

The storage module uses Flash memory K9WBG08U1M (4 GByte) as data storage, due to the characteristics of small size, low power consumption, large memory capacity and so on [8-9]. The writing and reading operation of Flash is in the unit of page. It is necessary to write the control word and address of next page again after finishing writing one page. Therefore, to guarantee data integrity in the alternating time of adjacent page, the internal FIFO of FPGA is used as data cache. The sampled data is written into FIFO first, and then stored to Flash. In the process of data operation, the average speed of input of FIFO is low than output. To improve the writing speed of Flash, the interleaving two-plane programming mode is used in the writing operation that the fastest writing speed can reach 30 MByte/s. The waiting time of page programming is reduced to the minimum by the interleaving pattern.

Since the craft of the NAND Flash can't guarantee the reliability of the Memory Array's retain performance during its lifecycle, so there will be some bad blocks during the production and using process of the NAND Flash. Though the bad blocks will not influence the performance of valid blocks, we should try to avoid the programming and erase operations of the bad blocks during the operation of the Flash. If the data is written to an invalid block, it will result in the loss of the test data. The bad blocks in the NAND Flash are randomly distributed, thus, the Memory Array must be able to identify and store the information of the bad blocks, and can skip the invalid blocks during its programming and erase operations. Rational and effective management of the bad blocks in the memory module helps to improve the storage efficiency of the data.

Also, to manage the invalid block of Flash conveniently, the address of invalid block is identified and written into the RAM of FPGA. When in the operation of page programming, reading or erasing, the address is read out to compare with the current address to identify whether the current block is invalid or not.

The detection process of the FLASH invalid blocks is shown in Fig. 6. And the detection method

is: when detecting each block, the value of the address of the 4096th byte in the first two pages. If both of them are "FF", the current block is valid, and it can be erased, written and read normally; otherwise, the current block is invalid, the current plane and block address are written to the cache to generate a query list of the invalid blocks.

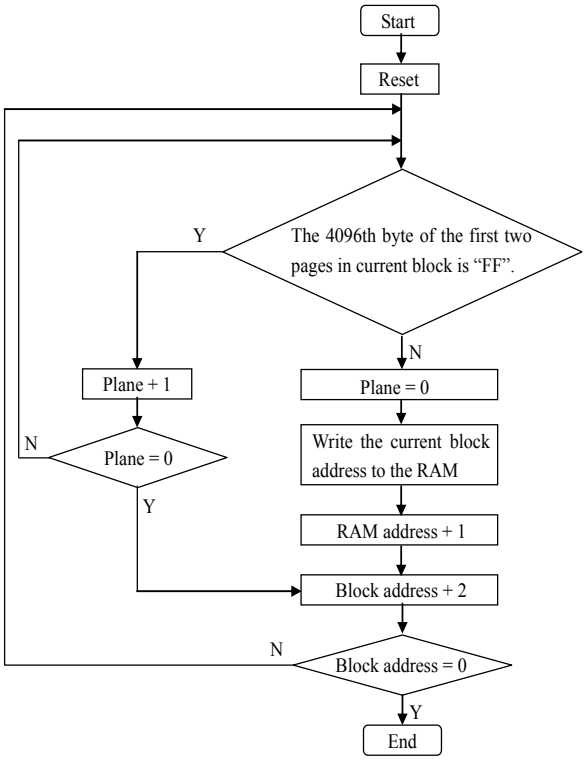


Fig. 6. The detection process of the FLASH invalid blocks.

4. The Design of Resistance to Overload

The solid state recorder accomplishes the acquisition and storage of signals. During the collision of missile high-speed intersection, the resistance to overload capacity of recorder reaches more than 2000 g. So the effective measure should be taken to strengthen overload resistance of the recorder [10]. After welding, chip itself is suspended in circuit boards, and connect the circuit boards only through the chip pin. Chip and circuit board didn't really form a whole. When the recorder is hit so hard, because the quality of various components is different, the overload is also different. This will be very easy to appear loose solder joints, virtual welding or pull up welding plate, etc. The circuit is packaged with encapsulating material and then become an integrated structure which is help for protecting the circuit. The process is called embedment. With a special resin of high strength and high toughness the chips and the circuit board are encapsulating into a whole, which can restrict the movement between the chip and circuit board. In addition, this has the effect of stable components, circuit parameters, to ensure no damage to circuit under high overload.

5. System Test and Result

In the process of system test, a multichannel signal source is used to verify the function of the acquisition system. In the experiment, the first operation is erasing after power-on. When the erase operation is complete, +27 V step signal is loading to start sampling and recording. After recording, the data is read into computer via the USB interface, and then analyze the data graphically. The software can draw up the wave of all the channels. Meanwhile, it also can check the frame format whether correct or not. The partial channels' waveform is shown in the Fig. 6. The frame format of all the data of each channel is correct. Through acquiring the sine ware, the acquisition precision which is expressed by ENOB can be calculated [11-15]. The ENOB of the acquisition system is better than 8 bit.

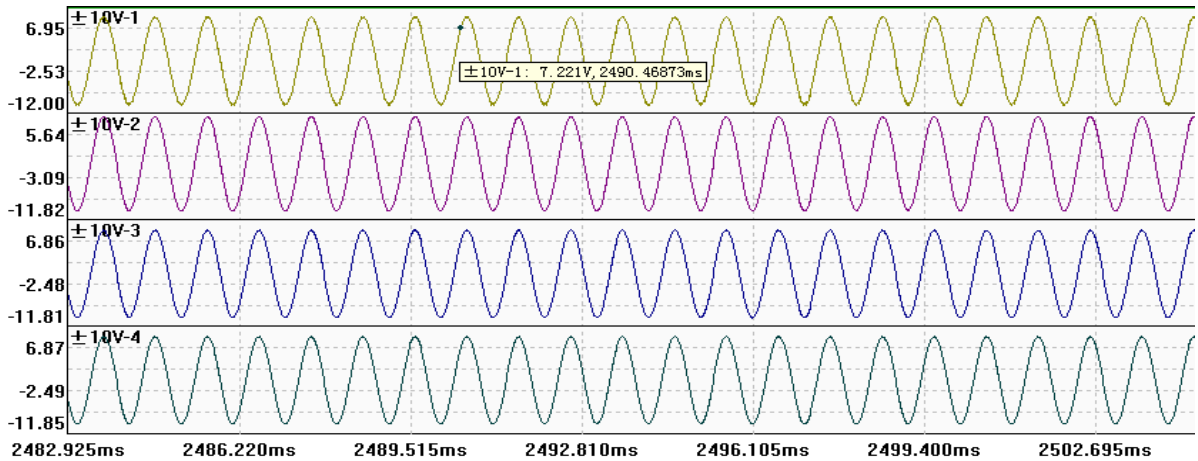


Fig. 6. The partial channels' waveform.

6. Conclusions

This paper proposed a general programmable multichannel acquisition method for the missile fuze test. For the eighty channels analog signals which consists Doppler signal and ignition signal and the working conditions of the security fuze enforcement agencies, the device is used solid state recorder which can resist the overload capacity of more than 2000 g and be employed repeatedly. Therefore, the design reduces experiment cost and has engineering practical value. The device has been used in the high-speed dynamic intersection experiment, which records the signals correctly and provides the accurate data for the fuze design and the fault analysis.

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