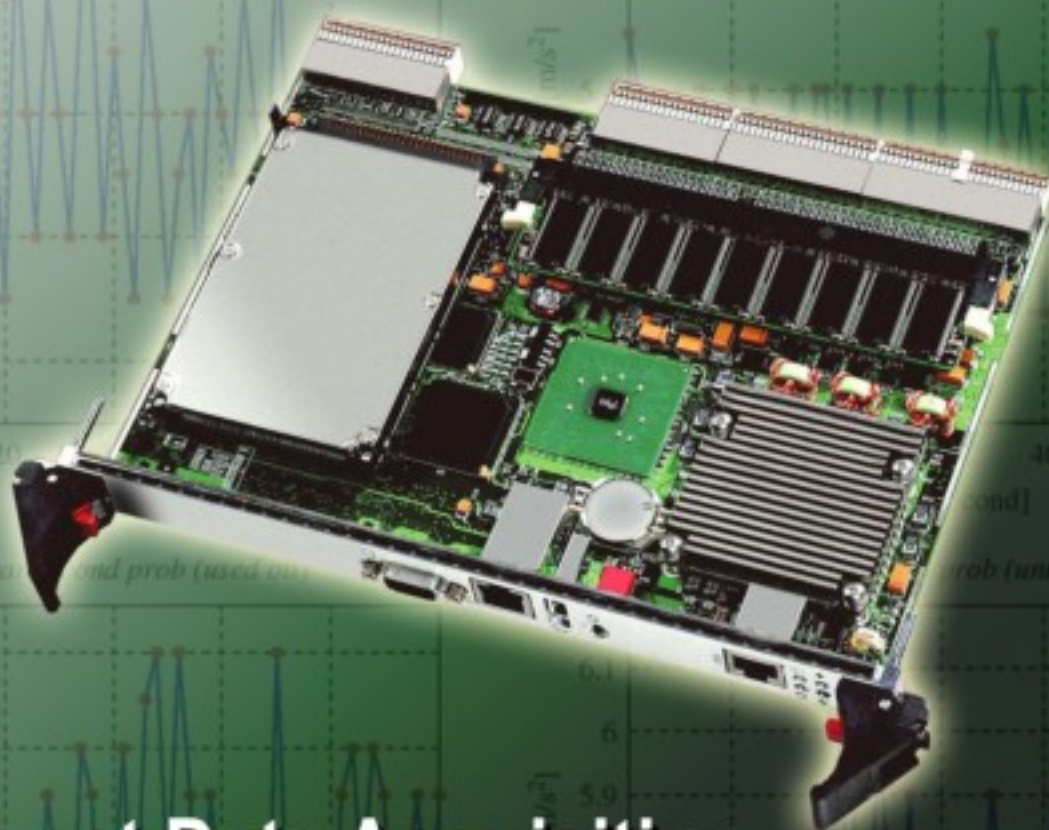


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Precise Time Synchronization Technology for Distributed Automated Test System

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Abstract: Clock synchronization is essential to the distributed automated test system which is widely used in the world. A time stamp generation circuit based on FPGA is introduced, and a synchronization algorithm based on prediction is used to adjust the frequency of slave clocks in the system. The peer-to-peer communication and the seven-point communication test environments are built, and clock synchronization can achieve the precision of us. *Copyright © 2012 IFSA.*

Keywords: Distributed automated test, Precision time synchronization, Prediction.

1. Introduction

Automated test system is increasingly using distributed system technologies such as network communication, local computing, and distributed objects. Many of these applications will be enhanced by having an accurate system wide sense of time achieved by having local clocks in each sensor, actuator, or other system device. Ethernet based distributed automated test system (EBDATS) make it easy for multi-point test, otherwise, some test tasks must be completed under coordination work with several signals, and these signals such as high frequency signals' pulse_cycle may even be up to 1us. This requires EBDATS must have a precise synchronization mechanism to ensure the synchronization operation of the test units.

Network Time Protocol (NTP) is one of the most widely applied software clock synchronization method [1], but its 1 ms synchronous precision can't meet the requirements of the test tasks for EBDATS in many cases. IEEE 1588 Standard for Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (PTP, Precision Time Protocol) [2] and the hardware trigger based synchronization method [3] can achieve the precision of ns, but they need specialized test equipment to support, and need to change the network link layer exchanging or routing equipments [4].

Some universal test equipments can provide high precise clock synchronization, but they can't meet the demand because of the particularity of signals in some special test tasks. In this case, the hardware with high precise clock synchronization function is needed to acquire and process special signals, and the corresponding precise clock synchronization method is needed. A time stamp (time with respect to an epoch) generation circuit based on FPGA is introduced in this paper, this method uses serial different input pulse but asynchronous message as the synchronous clock source. A clock drift correction algorithm based on prediction is provided, this algorithm ensured that the hardware can keep high precision synchronization with each other and need not to change the network link layer and the routing equipments.

2. Implementation

2.1. Time Stamp Offset Analysis

2.1.1. Time Stamp Additional Offset

In Ethernet, message package is received by physical layer, then sent to MAC layer, MAC layer sends the package to the host memory packet, and at the same time it generates an interrupt to notice the host that there are some packets received. Host responses to the interrupt, sends the packet to upper protocol stack, finally the packet reach the application layer [5]. The whole process is shown in Fig. 1. Timestamp can be generated in several positions: MAC (media access control) layer, drive layer as well as the application layer.

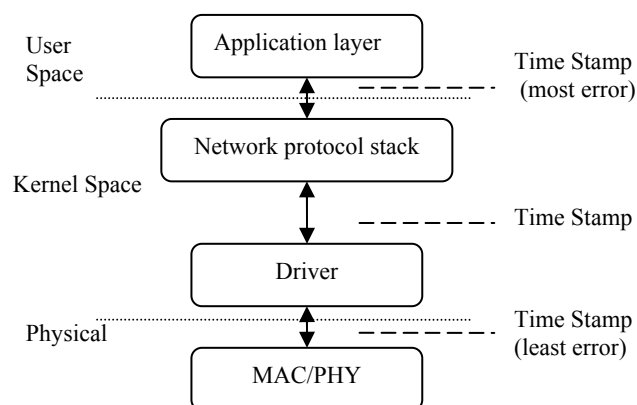


Fig. 1. Possible positions for adding timestamps.

The time delay caused by cache and interrupt response is different when the position of generating time stamp is different. As a result, the time stamp value and the real time deviation of the packet is not the same [6], which has produced additional time stamp additional offset. The timing information captured at physical or MAC layer will have a higher accuracy.

Definition 1: time stamp additional offset. Set the real time of data packets for t , the physical delay of packets for P_t , interrupt response time for I_t , driver delay for D_t , the application layer processing delays for A_t , then the time stamp adding time S_t :

$$S_t = t + P_t + I_t + D_t + A_t \quad (1)$$

Time stamp additional offset:

$$\varepsilon_t = S_t - t = P_t + I_t + D_t + A_t \quad (2)$$

There are several time stamp additional offset sources, most of them have millisecond timescale. Until now the attempts to improve the accuracy of the time stamp additional offset always face to the factors above: reference [7] improved the accuracy of time stamp by changing the time stamp position from the application layer to drive layer, finally increased the accuracy of the one-way network delay measurement and further; Reference [8] moved the time stamp position to physical link layer, and reduced the synchronous packets delay in the MAC through the priority queues.

2.1.2. Time Stamp Inherent Offset

The clock used to produce time stamp is affected by the jitter and drift of oscillators, and its frequency is instability [9-10], different oscillators produce different clock drift [11].

Definition 2: Time stamp inherent offset: set the current real time for t , clock resolution for α , the clock drift coefficient for β , the time stamp value of node i is $C_i(t) = t + \Delta\alpha + \beta(t)$, then the time stamp inherent offset:

$$\varphi(t) = C_i(t) - t = \Delta\alpha + \beta(t) \quad (3)$$

The time stamp offset contains time stamp inherent offset and time stamp additional offset:

$$\theta(t) = \varphi(t) + \varepsilon_t \quad (4)$$

2.2. Design and Implementation of Precise Time Stamp System

2.2.1. Time Stamp Representation Type Analysis

In EBDATS, the accuracy of time stamp depends on the characteristics of the oscillator (drift) and the frequency of the synchronization procedure (determined by the software). To get a higher precision of the system clock, the hardware circuit must be introduced to insert time stamp at the bottom layer to reduce the influence of software; but the characteristics of the oscillator (drift) can not be eliminated thoroughly, so some corresponding algorithm must be introduced to compensate the error, and finally reduce its influence to the system.

Time stamp generating circuit is shown in Fig. 2, the core is the comprehensive frequency adjust module (ADJ), this circuit adjust generating frequency of the clock by changing the value of frequency controlling word. Set the input clock frequency of the ADJ module for f_{ref} , the clock frequency output for f_{syn} , frequency controlling word for K_{adj} (32 bit), then:

$$f_{syn} = K_{adj} \times f_{ref} / 2^{32} \quad (5)$$

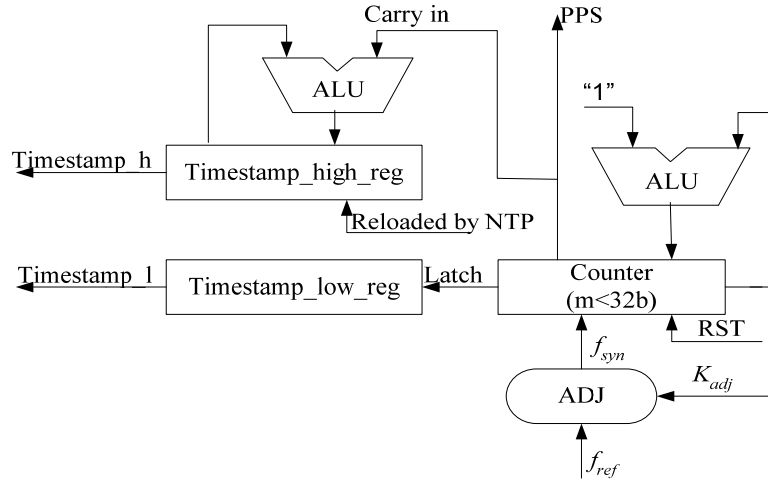


Fig. 2. Timestamp generation circuit.

To get a snapshot of the time, the TimeRepresentation type is defined, this time is 64-bit format with the upper 32 bits providing time in seconds (time stamp high register in Fig. 2), and the lower 32 bits indicating time in nanoseconds (time stamp low register in Fig. 2) .

```
struct TimeRepresentation
{
    UInteger32 seconds;
    Integer32 nanoseconds;
};
```

Actually, the precision of the clock can be changed by setting the lower 32-m bit to 0 ($m < 32$), in this way, we can get a 2^{-m} s precision for the clock.

2.2.2. Clock Drift Correction Algorithm Based On Prediction

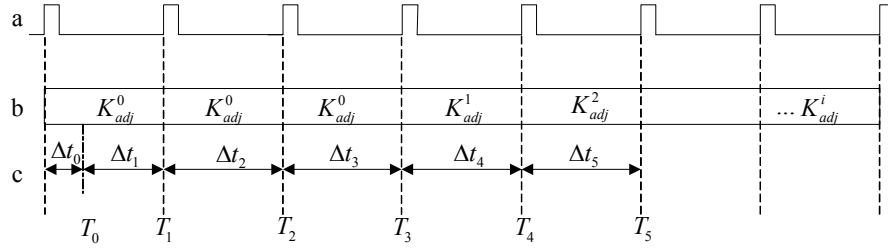
The synchronization for seconds can be easily achieved by NTP protocol, only the lower 32 bit time stamp value is generated by the internal counter. The counter clock can be divided by a prescaler f_{syn} , when the counter overflow event encountered, and the time stamp high register plus one. To ensure that the time between initialization to overflow of the counter is 1 second, then

$$f_{syn} = 2^m \quad (6)$$

In many applications of EBDATS, the local time of nodes is not required to be synchronization with UTC, but may be required to keep synchronism with a master clock in the system to enter a specified precision. Two clocks are synchronized to a specified uncertainty if they have the same epoch, and measurements of any time interval by both clocks differ by no more than the specified uncertainty.

In the synchronous process, master clock connected to slave clocks by different serial bus. The master clock outputs a PPS pulse every 1 s, the pulse is 125 ns wide. The slave clocks interrupt when they receive the pulse from master clock, and read time stamp value form the time stamp register, then use the synchronous algorithm based on prediction to adjust the frequency controlling word K_{adj} . The slave clock frequency drift with respect to the master clock is corrected over a period of time, and finally reach a minimum deviation from master clock. The longer correction time helps maintain linear time and does not introduce drastic changes (or a large jitter) in the reference time between Sync pulse intervals.

The synchronous algorithm based on prediction can be divided into two stages in the implementation process: starting stage (Fig. 3) and synchronization stage.



a: reference clock pulse (PPS) input from master card
b: frequency control word
c: timestamp value of slave card when PPS interrupt occurred

Fig. 3. Schematic diagram of Predict algorithm.

2.2.2.1. Starting Stage

Step 1: The slave clock begins to work, it needs to be initialized, and this time is set for Δt_0 , T_0 is the moment when the node complete the initialization. When the next time the sync pulse from master clock arrives, the slave clock reads and records the time stamp T_1 .

Step 2: Read the time stamp T_2 , $\Delta t_2 = T_2 - T_1$, then the actual clock frequency:

$$f_{ref} = f_{syn} \times 2^{32} / K_{adj} = \Delta t_2 \times 2^{32} / K_{adj}^0 \quad (7)$$

In step 2, the frequency control word K_{adj}^0 is also used, so we can suppose that the time difference will reach to $2\Delta t_2$ in step 3, calculating the frequency control word K_{adj}^1 :

$$K_{adj}^1 = [4 \times 2^m - (\Delta t_1 + 2\Delta t_2)] / \Delta t_2 \times K_{adj}^0 \quad (8)$$

Step 3: Calculate the frequency control word K_{adj}^2 with the current time stamp T_3 :

$$K_{adj}^2 = 2^m \times K_{adj}^0 / \Delta t_3 \quad (9)$$

The slave time stamp is closer to the master time after step 3, but it is not the normal pursue stage, the offset is not useful, the frequency control word K_{adj}^i is calculated in synchronization stage.

2.2.2.2. Synchronization Stage

Every moment of receive the pulse from the master clock, the time stamp T_i is recorded, and the offset is calculated: $\Delta t_i = T_i - T_{i-1}$.

The prediction value of the time offset for the forward two steps is calculated:

$$e^0(i) = 2^m - \Delta t_i \times K_{adj}^i / K_{adj}^{i-1} \quad (10)$$

$$e^1(i) = 2^m - \Delta t_i \quad (11)$$

The frequency control word K_{adj}^{i+1} for next step is calculated through K_{adj}^i of the current step:

$$K_{adj}^{i+1} = [2^m + e^0(i) + e^1(i)] \times K_{adj}^i / \Delta t_i \quad (12)$$

3. Performance Tests

In order to verify the precision of the time stamp in the automatic system, the peer-to-peer communication and the multi-points communication test environments were built.

In each test environment, the slave clock keep synchronization with the master clock when the 1s pulse comes. There are something need to be pay attention to:

1) To eliminate software delay effects, time stamp registers value is locked when the second pulse comes, the values used in the software are the locked value, this method can ensure that the value read from register can take away from the software delay;

2) Frequency control word K_{adj} doesn't take effect immediately after updated but until the next pulse comes, in this way, the final time stamp value can be prevented from being influenced by software written delay.

3.1. Peer-to-peer Communication

A slave clock node is connected to the master clock with different serial bus and the two nodes can exchange their sync-message through the network. In this module, we can test the correctness of the synchronous algorithm, system is connected as shown in Fig. 4.



Fig. 4. Peer-to-peer connection.

To achieve the clock precision of 50 ns, the value of m in formula (6) should be set as 25, the update clock frequency f_{syn} should be 20 MHz. If the frequency of the oscillator f_{ref} is 40 MHz, then we can initialize the frequency control word $K_{adj}^0 = 2^{25} / (40/20) = 0x1000000$, the slave clock calculate the predicted value K_{adj}^{i+1} in every pulse period, and use the new frequency f_{syn} to keep synchronization with the master clock.

Allan variance [12] $\delta_y(\tau)$ is used to indicate the time offset:

$$\delta_y(\tau) = \{ [\Sigma(\theta_{k+2} - 2\theta_{k+1} + \theta_k)^2] / [2(M-2) \tau^2] \}^{1/2} \quad (13)$$

$$k = 1, 2 \dots M-1$$

In formula (13), θ_i is the offset of the slave clock at the moment t_i , $\delta_y(\tau)$ is the statistics information for frequency variance.

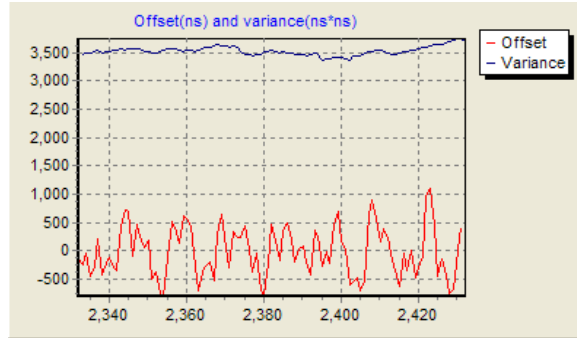


Fig. 5. Results of Allan variance and Time offset.

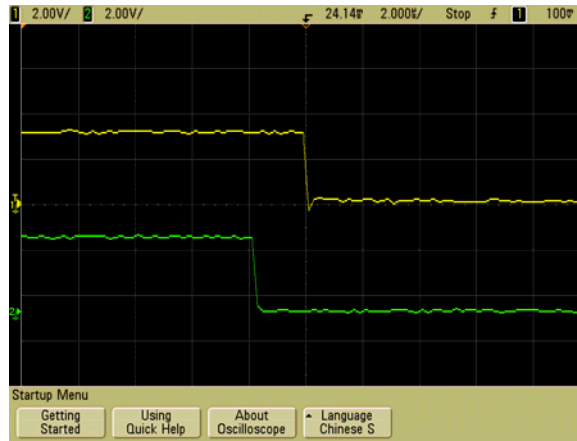


Fig. 6. Synchronization accuracy in peer-to-peer system.

3.2. Multi-points Communication

Network is constituted by 7 nodes, which contains one master clock and 6 slave clocks, we can get the relative accuracy synchronization by compare the PPS signals of the 7 nodes, the module is shown in Fig. 7.

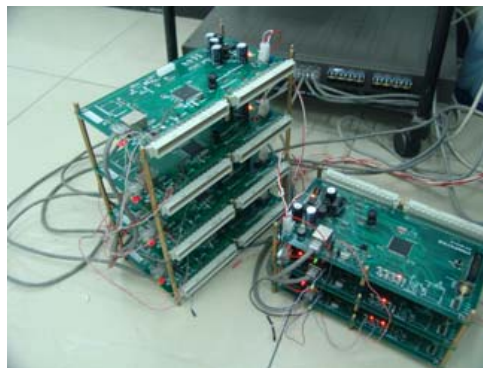


Fig. 7. Multi-points synchronization precision test system.

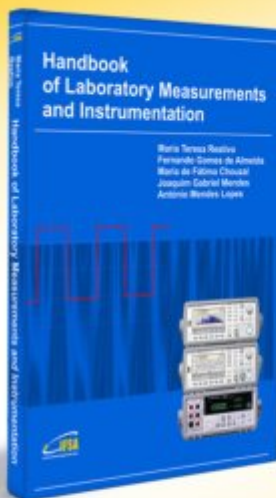
Although the information is exchanged through switch, only NTP synchronization message is network related, and the delay caused by network is lower than 1 second. In the synchronization system, the accuracy of time stamp will not descend with the increase of the slave clock number, so the synchronization accuracy in multi-point communication system keep the same as in peer-to-peer communication system, but a longer correction time helps maintain linear time with master clock between Sync pulse intervals.

4. Conclusions

The clock synchronization circuit and the clock drift correction algorithm based on prediction designed in this paper can support system-wide synchronization accuracy in the submicrosecond range, and the implementation of exchanging information is also based on the original Ethernet. In this way, the proper automatic test system, which needs a higher precision synchronization less than 1 ms can be designed without expensive universal equipments.

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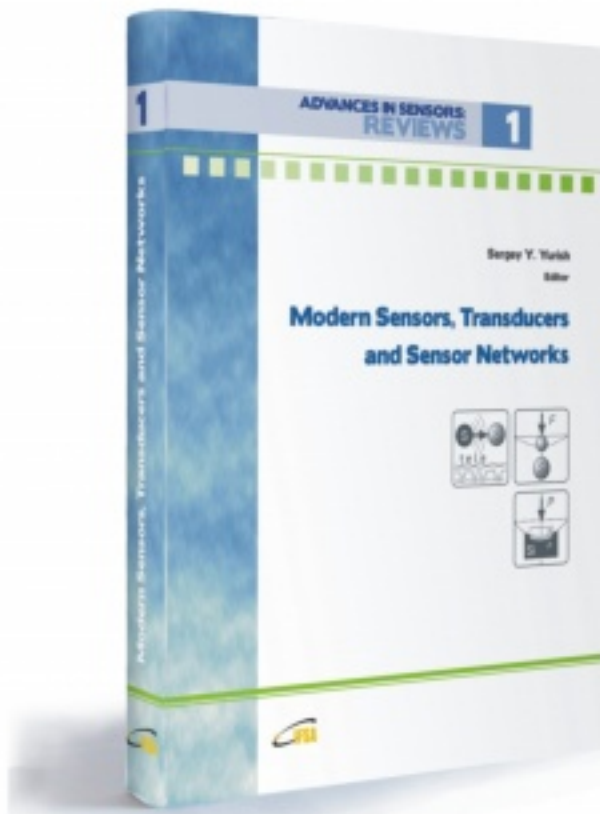
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