

A Low-Power Energy Detection IR-UWB Synchronization and Decision Scheme for Wireless Sensor Network Applications

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Abstract: Impulse Radio Ultra-wideband (IR-UWB) is a modern radio technology that uses modulated pulses to transmit information and works at extremely low energy levels. It is popularly used in short-range, low power and low cost communications such as vehicular ad-hoc networks (VANETs), RFIDs and wireless sensor networks (WSN). This paper presents the design and implementation of an IR-UWB Transceiver using energy detection scheme with on-off keying (OOK) modulation. A synchronization and detection algorithm called energy offset based scheme is proposed and used in the transceiver, which can greatly reduce power consumptions for synchronization and simplify hardware complexity. To increase flexibility, the prototype of the transceiver's baseband is implemented on FPGA, with design of FSMs in the controller. Simulation results are given, which reveal that the proposed UWB receiver has simple and power saving synchronization blocks, smaller preamble code length in synchronization, while maintaining performance in the target level. With RF front-end added, the transceiver is used as a wireless communication module in a WSN for water quality monitoring. Field testing data are given, showing the transceiver can work at 10 Mbps in 10 m radius, with energy efficiency below 1 nJ/bit. *Copyright © 2013 IFSA.*

Keywords: IR-UWB transceiver, Energy detection, Synchronization, Energy offset, FPGA.

1. Introduction

Nowadays, as vehicles become more and more popular in China's cities, the Vehicle Ad-hoc Network (VANET) is getting more and more research focus. By vehicle-to-vehicle and vehicle-to-roadside communications, VANETs can greatly avoid traffic accidents on the road. As well as RFIDs and wireless sensor networks (WSN), VANET is playing an essential role in the emerging era of Internet of Things (IoTs). The IoTs is regarded as an extension of today's Internet to the real world of physical objects, and may impose an impact on our daily life dramatically as what internet has had in the past years. The perception layer of IoTs, which

includes RFID tags and WSN nodes, will be smartly networked and organized by micro-power wireless links that bridge them to the existing ICT infrastructures. In the application area of VANET, the main focus is on high efficient communications between adjacent cars or between cars and roadside nodes. Such micro-power wireless links used in VANETs usually require ultra-low energy consumption (~ 1 nJ/bit and below), low hardware complexity, low transmission latency, high channel capacity and highly integrated transceivers, with moderate operation range (< 100 m) and data rate ($\sim M$ b/s at 10 meters). Besides, the VANET should also operate with high mobility.

Fig. 1 below shows a common scene of VANET application. There are two typical communication ways: vehicle-to-vehicle and vehicle-to-roadside. The network, where sensors are located in roadside or vehicles, monitors the traffic situation in real time. Some useful traffic data can be transmitted to all vehicles on the road, and each vehicle has a display to tell the driver what's happening on the road. For example, when traffic accident or traffic jam happens, sensors from the accident cars or roadside will immediately send information to nearby vehicles, with highest priority. Other information, such as traffic, speed, weather, or even music, can be transmitted with lower priority. This need the VANET possesses a multi-hop transmission capability.

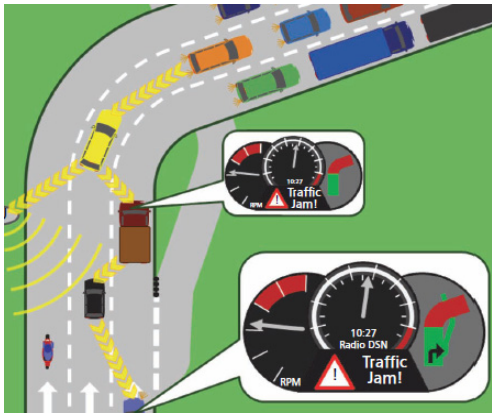


Fig. 1. VANETs, with vehicle-to-vehicle and vehicle-to-roadside communication [1].

In recent years, several wireless standards have been proposed for low power low cost IoT applications. Among them, Impulse radio ultra wideband (IR-UWB) shows great advantages owing to its inherent carrier-less property. The signal transmission relies on short duration pulses (~ns) that can be generated without RF mixing stage. The baseband-like transceiver architecture deals with a low duty cycled (<1 %) signal. In frequency domain, noise-like signals distributed in extremely broad bandwidth (3.1 GHz~10.6 GHz, according to FCC) provide robust and high speed communication links. All these features guarantee transceivers with low power consumptions, low hardware complexity, low cost and moderate data transmit rate [2]. Coherent and non-coherent receiving can both be used in IR-UWB receivers. Fully coherent receivers perform well but at the expense of high computational and hardware complexity. Therefore, they are not feasible for the resource limited low power low cost applications. As a sub-optimal solution, a non-coherent receiver is able to relax information of channel, fine timing and pulse shape. Energy detection receiver belongs to non-coherent category. The advantage of energy detection is its low complexity architecture, which does not require channel estimation and precise synchronization time

as in coherent receivers. Thus, the proposed transceiver architecture for low power low cost RFID and WSN applications is based on energy detection.

Low power and low complexity energy detection UWB receivers have been studied previously in [3-5]. In these literatures, the synchronization scheme based on maximum energy search method is employed. This algorithm is simple, but requires either a bank of integrators or a long preamble period, which is not energy efficient. Fig. 2 below shows a UWB transceiver block diagram of a previous work using maximum energy search scheme [10]. This block used 8 integrators to do synchronization. The detailed work process is as follows: The start time of each integrator is uniformly distributed in one bit time, with integration length equal to 1 bit. First get all the outputs of 8 integrators, then search all the eight outputs and find out the integrator with maximum value. The start time of this integrator is thus the start time of bit.

From the power consumption table of each block in the right, we see that the integrators consume most of the power. In order to overcome this problem, an innovative synchronization and detection scheme based on energy offset is suggested in this contribution. By using a single integrator, it can significantly reduce the hardware complexity, power consumption, and the length of preamble, whereas maintaining system performance in the target level. Shorter preamble length means lower transmission overhead and more energy efficiency [4]. Simulation and implementation results show that the innovative receiver architecture which requires only one integrator has almost the same BER performance as the one using 8 integrators [3].

The remaining part of this paper is organized as follows. Section II presents the proposed system architecture and discusses the mathematical modeling of signals in this system. Section III gives principles of the innovative synchronization and detection scheme used in energy detection IR-UWB architecture. Section IV discusses the FPGA implementation of the digital baseband in detail. Section V discusses the usage of proposed transceiver architecture in a practical WSN system. In field data-rate performance is measured and given. Finally, conclusions are given in Section VI.

2. System Architecture and Modelling

2.1. System Architecture

The proposed IR-UWB receiver in this paper is an OOK modulated, energy detection based receiver. According to the application requirements in IEEE 802.15.4a [5], the system specification is as follows. Bandwidth: 3.1~10.6 GHz; operation range: 10 m; data rate: 10 Mbps. The pulse repetition interval of IR-UWB waveform is 10 ns. Architecture of the UWB receiver proposed is shown in Fig. 3 below.

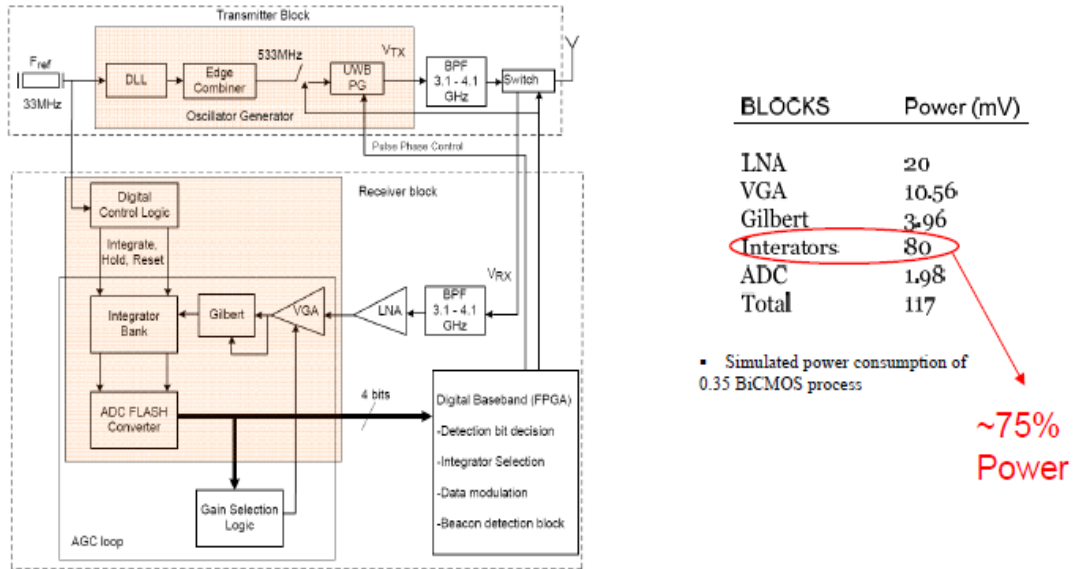


Fig. 2. Block diagram of a previous work, with power consumptions [10].

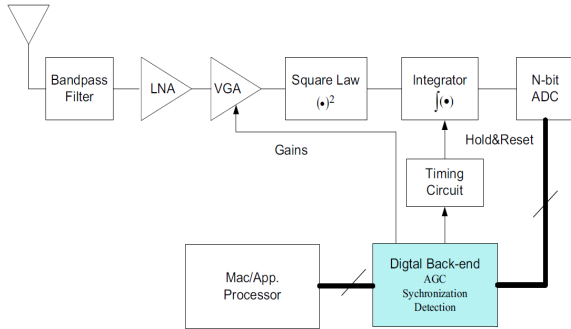


Fig. 3. Proposed energy detection IR-UWB Receiver.

2.2. System Modelling

The system model of the energy detection receiver is shown in Fig. 4.

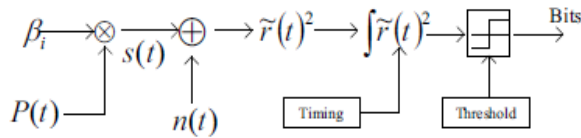


Fig. 4. System model of signals from transceiver to receiver.

It works as follows: an IR-UWB transmitter sends a stream of ultra short pulses. In OOK modulation, the information bit is represented by absence or presence of pulses in each pulse repetition interval. The core component of proposed receiver is an energy detector, which consists of a square law device followed by a finite time integrator. The received signal is first squared and then integrated during a certain time. The output of integrator is sent to a threshold detector for detection [7].

The energy detection process can be expressed below:

$$y_i = \int_{T_s}^2 r(t) = \int_{T_s} [\beta_i \tilde{s}(t) + \tilde{n}(t)]^2 dt \quad (1)$$

$$= \beta_i \int_{T_s}^2 s(t) dt + 2\beta_i \int_{T_s} \tilde{s}(t) \tilde{n}(t) dt + \int_{T_s}^2 \tilde{n}(t) dt$$

where β_i is the transmitted data, $P(t)$ is the pulse shape, T_f is the pulse repetition period, N_s is the number of pulses per symbol, $T_s = T_f N_s$ is the symbol duration, and $n(t)$ is the Gaussian Noise with double-sided noise spectral density $N_0/2$. The output of the integrator is the energy of the input signal over time interval T_i in the past. [8] A symbol period time $T_i = T_s$ is chosen as the integration window in this work. A decision is made by comparing y_i with a threshold δ , to judge if there is energy or not in a symbol period.

3. Synchronization and Detection Scheme

Synchronization is one of the most challenging tasks in receivers. There are three different synchronization levels: frame-level, bit-level and pulse-level synchronization [8]. In non-coherent receivers especially the energy detection receiver, bit-level synchronization is primary used. The synchronization process is used to get the precise start time of bit transmission and improve the correctness of bit detection later on. Traditional synchronization scheme using maximum energy search method requires either a bank of integrators or a long preamble period [9]. In the following, an innovative synchronization scheme based on energy offset is suggested. This scheme needs only one integrator, which greatly reduces power consumption

and hardware complexity. Fig. 5 shows signal waveforms in each stage of transmission between the transmitter and the receiver RF front-end. The data transmitted here is: 01001101.

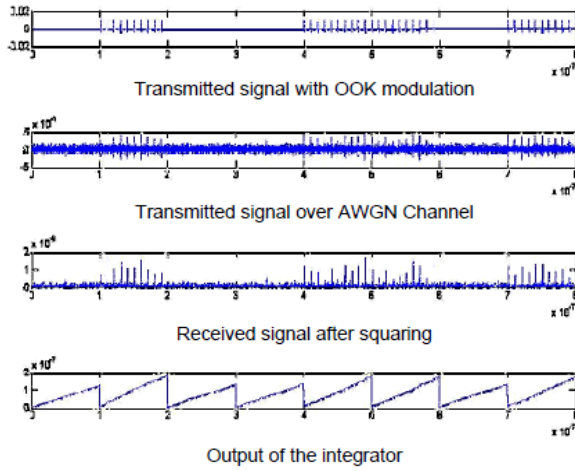


Fig. 5. Signal waveforms in transmission.

Fig. 5 shows that, due to the noise in AWGN channel, the variances in output value of the integrator between bit 0 and bit 1 are not so significant. The difference between these two values are called detection margin, which is shown in Fig. 6.

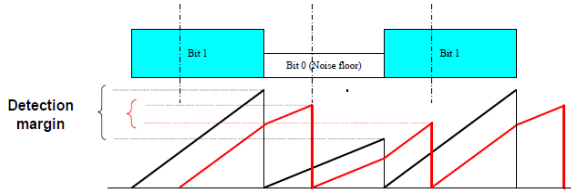


Fig. 6. Synchronization and detection margin.

In Fig. 6, preamble bits are transmitted. The first starting line represents the integrator output when time is matched (that is, the signal is synchronized), and the later starting line represents the integrator output when time is mismatched. When time is mismatched, a fraction of adjacent bit's energy is shifted to current bit. This can reduce the detection margin between 0 and 1. When synchronized, the detection margin reaches its maximum value. So an important task is to find out the maximum energy margin between 0 and 1. This bit-level synchronization scheme is called the energy offset based scheme.

Then how to get the maximum energy margin when the signal is not synchronized? To solve this problem, noise bits and preamble bits are used before the useful data in one frame. Several bits of "0" are sent first, the total and average energy of bit 0 are derived as E_{noise} and E_{bit0} . Then, N_{pre} bits of preamble code are sent (that is, N_{pre} bits of alternating 1 and 0).

The preamble code has $0.5N_{pre}$ bit 1s and $0.5N_{pre}$ bit 0s. We have the following equations:

$$E_{bit0} = \frac{E_{noise}}{N_{bit0}} \quad (2)$$

$$E_{bit1} = \frac{2}{N_{pre}} (E_{preamble} - 0.5E_{noise}) \quad (3)$$

where E_{bit1} is the average energy of bit 1. $E_{preamble}$ is the total energy of the preamble code. The detection with perfect synchronization is $E_{bit0} - E_{bit1}$. That is also the maximum energy margin. Finally, the offset factor ε is derived from the following equations:

$$\begin{aligned} \hat{E}_{bit1} &= \int_{(1-\varepsilon)T_s}^{T_s} S_1^2(t) dt + \int_{\varepsilon T_s}^{T_s} n_0^2(t) dt \approx (1-\varepsilon)E_{bit1} + \varepsilon E_{bit0} \\ \hat{E}_{bit0} &= \int_{(1-\varepsilon)T_s}^{T_s} n_0^2(t) dt + \int_{\varepsilon T_s}^{T_s} S_1^2(t) dt \approx (1-\varepsilon)E_{bit0} + \varepsilon E_{bit1} \end{aligned} \quad (4)$$

$$\varepsilon = 0.5 - \frac{\hat{E}_{bit1} - \hat{E}_{bit0}}{2(E_{bit1} - E_{bit0})}, \quad (5)$$

where $\hat{E}_{bit1}$ and $\hat{E}_{bit0}$ is the estimated value of energy in bit 1 and 0 before synchronization. The offset ε is critical in synchronization process. It is actually the relative time needed to delay in order to synchronize the bit. When ε is calculated, synchronization can be done by delaying the signal for a certain time (relative to ε).

In addition to synchronization, the estimation of threshold for deciding 0s or 1s also yields from the preamble. The proposed estimation process is accompanied with time synchronization, by averaging the energy in even N symbols of alternating 1 and 0. The estimated threshold can be written as:

$$\zeta_{estimated} = \frac{1}{2} \left(\frac{(E_{preamble} - \frac{E_{noise}}{2})}{0.5N_{pre}} + \frac{\frac{E_{noise}}{2}}{0.5N_{pre}} \right) = \frac{E_{preamble}}{N_{pre}} \quad (6)$$

4. FPGA Implementation

4.1. Digital Baseband Design – Hardware

Fig. 7 presents the top level architecture of a digital baseband module designed based on the energy offset synchronization scheme previously discussed.

It is used to control the RF receiver and recover information bits from incoming signals. It is designed and implemented on FPGA, working at the bit rate frequency, with 4-bit data width [11].

In the baseband block diagram shown in Fig. 7, there contains control logic, noise processing block, preamble code block, threshold block and offset output block. These blocks together can fulfill the

energy offset based algorithms previously discussed, and output precise offset value.

Fig. 8(a)~8(e) below shows the detailed block diagrams of control logic, noise processing block,

preamble code block, threshold calculation & detection block and offset output block. Among them, the control logic is the most important and complicated block in the overall baseband module.

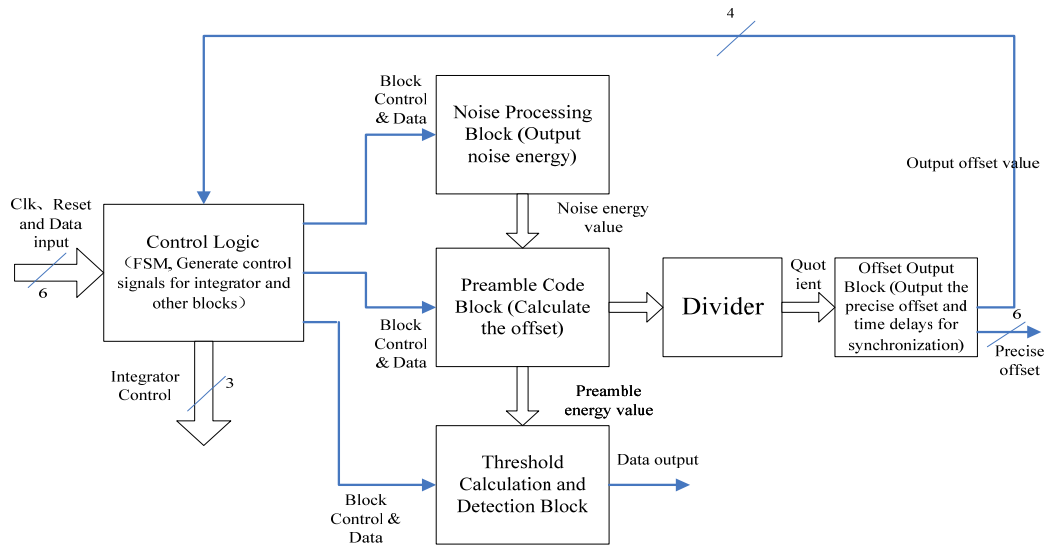


Fig. 7. Top level block diagram of the digital baseband.

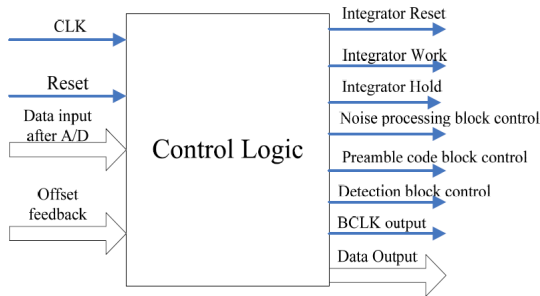


Fig. 8 (a). The control logic.

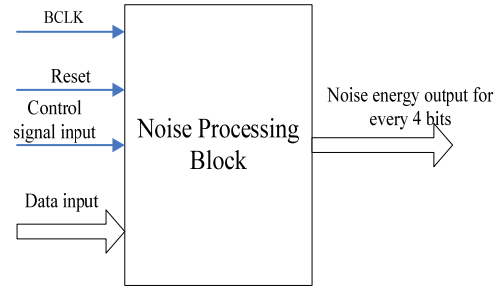


Fig. 8 (b). The noise processing block.

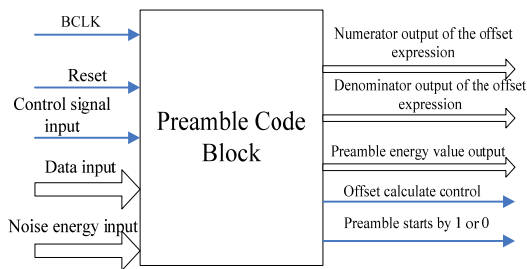


Fig. 8 (c). Preamble code block.

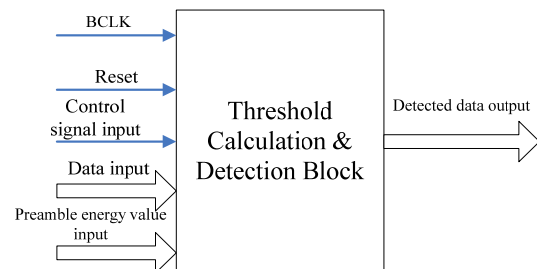


Fig. 8 (d). Threshold calculation & detection block.

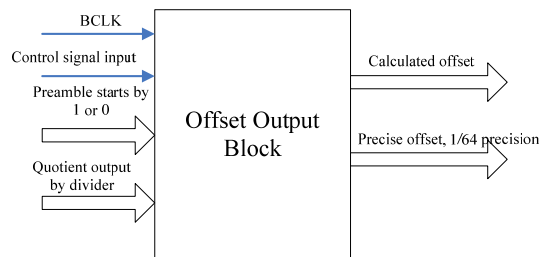


Fig. 8 (e). Offset output block.

The control logic controls the starting and finishing time of other blocks. It also controls the integrator and realizes bit synchronization based on the offset value input. In this control logic, the input signal is CLOCK, RESET, Data input after ADC (That is 4-bit wide in this system), and the 4-bit wide offset value feedback (Calculated by the offset output block). Here, 4-bit data width is chosen because of a tradeoff between time precision in synchronization and power consumption.

In the noise processing block, the input is BCLK, RESET, control signal and 4-bit wide data. BCLK is the clock used by all the above blocks other than the control logic. In this system, the frequency of BCLK is set to be 1/8 the frequency of CLK, due to the requirement of synchronization process. The control signal is connected to control logic. When the control signal is set to "1", this block works, input the 4-bit wide noise data and output the calculated average noise energy. The function of this block is based on equation (2). The noise energy calculated is sent to another block called the preamble code block. When the control signal is set to "0", this block stops working.

The preamble code block works when its control signal is set to "1". It inputs the 4-bit wide preamble bits after ADC, together with the noise energy calculated. Functions of this block are based on equation (3) and (4). After calculation, the numerator and denominator outputs are derived for the divider to calculate the offset factor. The bit width of numerator and denominator depends on the accuracy requirement. In this system 8-bit wide numerator and denominator are used. Another output is the preamble energy value output, which is the total energy of n bit preamble bits. This value is used to calculate the estimated threshold for bit detection according to equation (5). The output "offset calculate control" is used in the offset output block to show whether the quotient of the divider is larger or smaller than 0.

In the threshold calculation and detection block, the estimated threshold is calculated according to equation 4. Then the system uses this threshold to detect the 4-bit wide data received (called Data Input in the graph) and output data stream. This output data is only 1-bit wide.

The offset output block works to output two kinds of offset values. One is 4-bit wide, sent back to the control logic and used in the synchronization process. The other is more precise. It has 6-bit wide, which means that its precision is 1/64. This offset value is only used to validate the correctness of the block's calculation function.

4.2. Digital Baseband Design – Software

As discussed before, the control logic works as a scheduler, making precisely the starting and finishing work time of each other blocks. There are 3 states in the control logic. State 00 is the initial state. In this state, the noise processing block is working and

counting noise bits. When preamble codes (alternating 0 and 1) are detected by receiver, state turns to 01. The preamble code block is working instead, counting the number of preamble bits. After the preamble codes end (in the simulation we use 8 bit preamble), threshold calculation & detection block is working and state turns to 10 to detect normal bits. The following figure is the control dataflow graph (CDFG) of the control logic block.

There are also two FSMs in the control logic. One is the FSM in main control block, which has its CDFG presented in the Fig. 9.

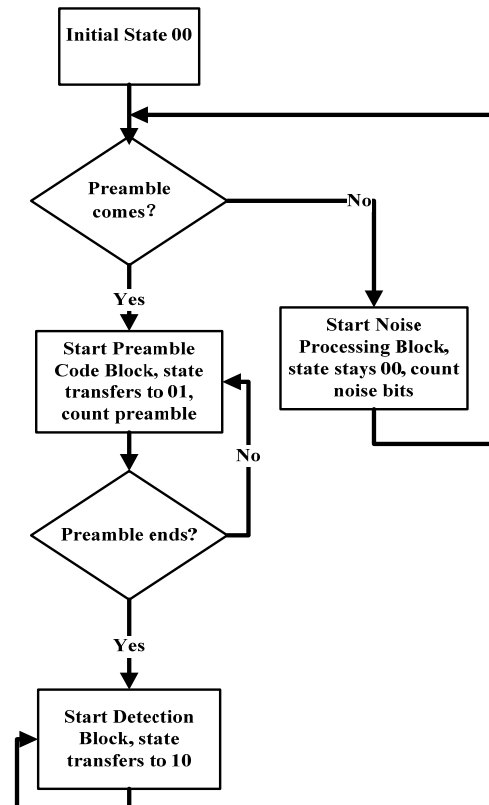


Fig. 9. CDFG of the control logic block.

The other is the FSM in integrator controller. These two FSMs are presented in Fig. 10 and Fig. 11. Note that the output signal $lj0_control$, $ljpre_control$ and $pj_control$ are three output signals that control three function blocks.

In state 00, the output control signal " $lj0_control$ " of control logic is 1 and noise processing block is working. There is a counter in this block to count on the number of noise bits. After n bits of noise, the preamble comes and the state turns to 01. In this state, " $ljpre_control$ " is set to 1 and the preamble code block is working. This block contains the calculation functions of the offset factor and the estimated threshold. There is also a counter in the preamble code block. If the number of preamble bits received are smaller than n , stay in state 01. After n bits of preamble, the preamble finishes and the state turns to 10. Note that the bit number of noise is the

same as preamble, due to algorithms discussed before. In State 10, “pj_control” is set to 1 and the detection block is working. This block calculates the estimated threshold from preamble bits and do bit detection based on this threshold. The state stays on 10 as the function of data detection goes on.

Fig. 11 presents the FSM in integrator controller. In this FSM, there are 8 states. The state transfers when positive edge clock comes. S0 and S1 are the reset states; the integrator reset its output value to 0. After that, in state S2 the controller gets the offset value calculated by other blocks, and detect whether it is larger than 0. If the value is larger than 0, the state stays in S2 and delays for N clock cycles. N is equal to the offset value calculated. If the value is 0, which means that the signal is already synchronized and thus do not need to do more synchronization, the state will transfer directly to S3 after 1 clock. S3, S4, S5 and S6 are the working states for the integrator. In these states, the integrator integrates the input value. And state S7 is the hold state. The value integrated is

the 4-bit wide output signal of the control block. Then the state transfers back to S0, finishing a cycle.

4.3. FPGA Implementation

The digital baseband is developed by VHDL in RTL level and mapped on an Altera Cyclone II chip, with the area of 1468 logic elements, 532 registers and 3968 bits memory. The design is verified by simulation and test. Fig. 12 presents the schematic diagram in Quartus II. Fig. 13 shows RTL schematic of the baseband module. Fig. 14 shows waveforms of signals from FPGA chip using Signal Tap II Logic Analyzer. We can see 8 bits preambles (0 and 1 alternating) before data transmission. After the preamble codes sent, the bit-level synchronization process is finished and the estimated threshold for detection is calculated. Signals received and detected are the same as signals sent, except for a certain delay caused by hardware processing.

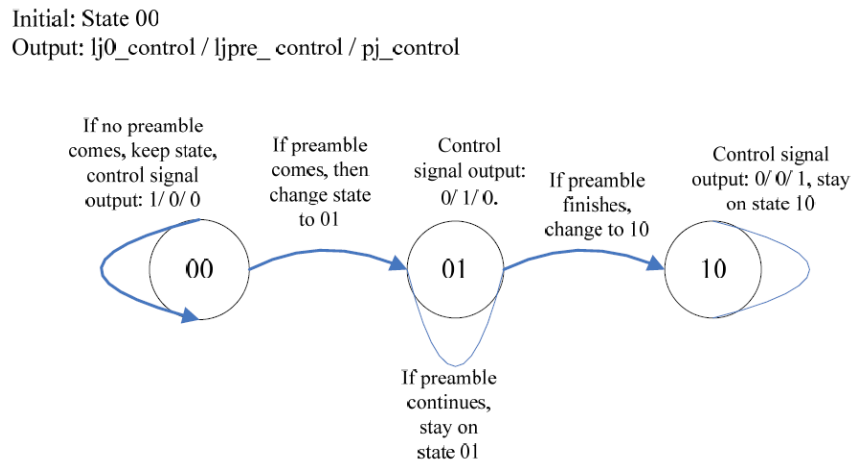


Fig. 10. FSM in the block control unit.

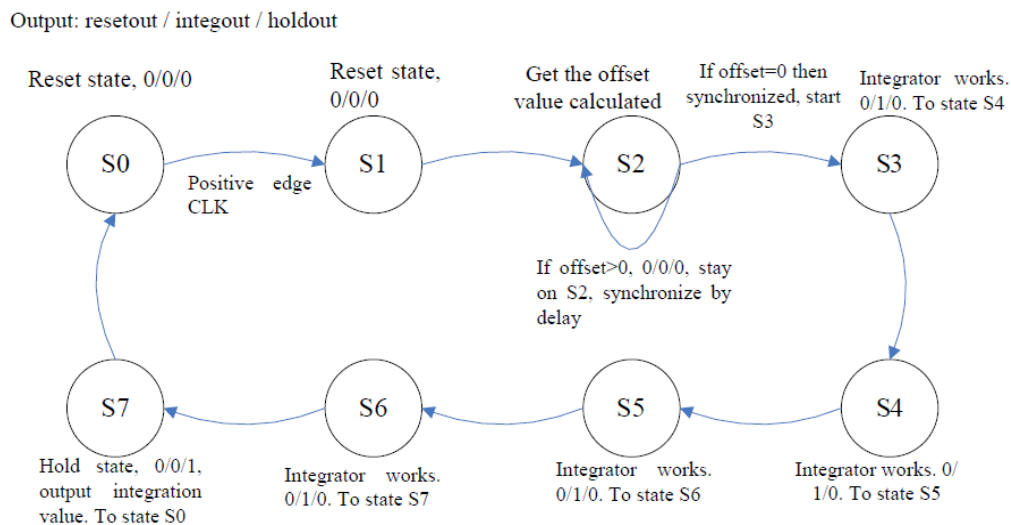


Fig. 11. FSM in the integrator controller.

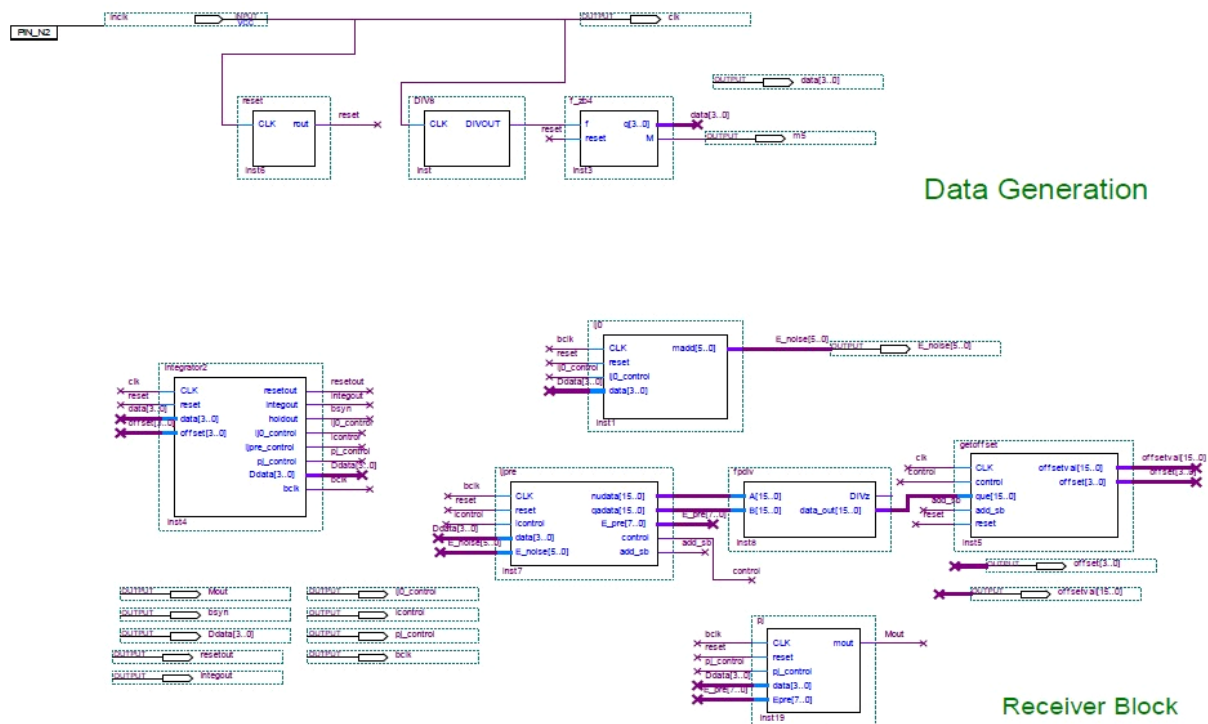


Fig. 12. Schematic diagram in Quartus II.

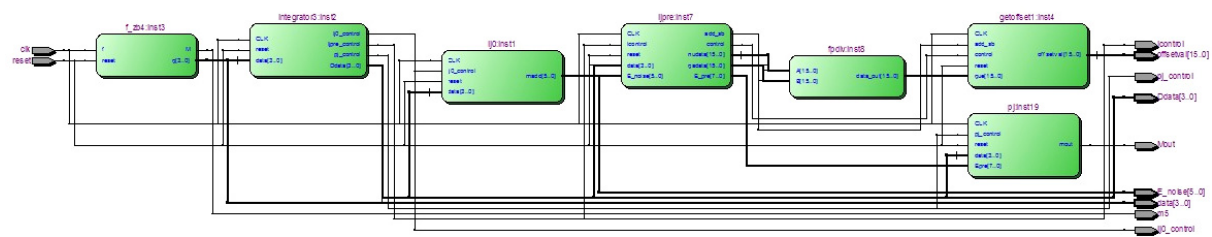


Fig. 13. RTL schematic of digital baseband.

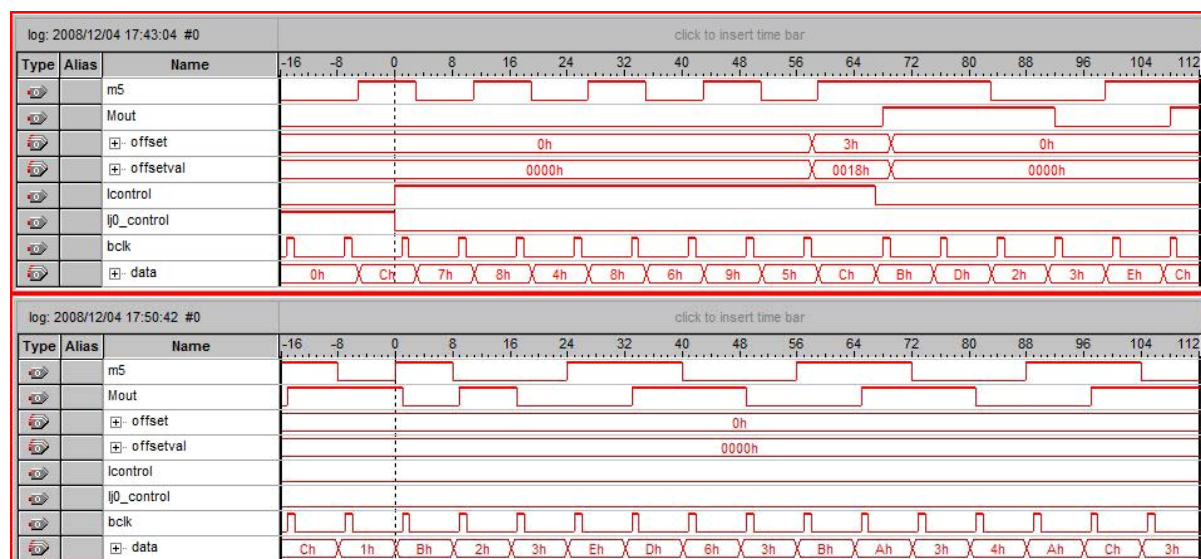


Fig. 14. Signal Tap II Logic Analyzer waveform.

5. Application in a Water Quality WSN System

Nowadays, wireless sensor network (WSN) based applications are getting more and more popular. The rapid development of WSN technology provides us a novel approach to real-time data acquisition, transmission and processing.

Take a practical solar panel powered water quality monitoring WSN system for example. We need to get the water quality data (temperature, pH, oxygen density, turbidity and so on) of a certain area in real time, and using as little power as possible. In this typical WSN system, there are several sensor nodes and a base station. Each node contains a group of sensors and the nodes are distributed in different

water bodies. Data collected by sensors is sent to the base station via WSN channel. The data-rate needed is well below 1Mbps. The base station is usually a PC with Graphic User Interface (GUI) for users to analyze water quality data or alarm automatically when water quality detected is below preset standards [12].

In this part, the proposed IR-UWB transceiver is used as communication module of the sensor node. The node can thus achieve its energy saving property because of the low power low cost architecture of IR-UWB transceiver. Besides, the data-rate of the transceiver is much higher than WSN needed. Fig. 15 below presents the detailed block diagram of a sensor node.

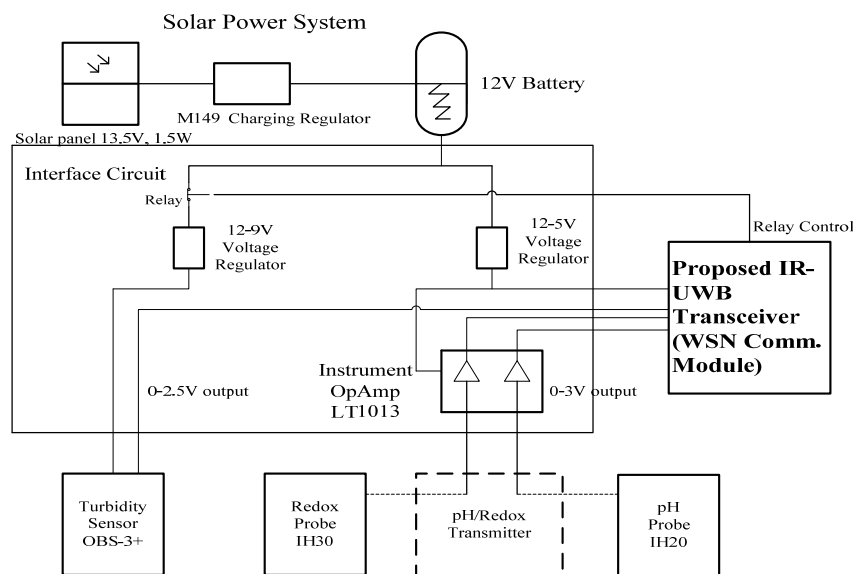


Fig. 15. Detailed Block Diagram of a Sensor Node in WSN [11].

Fig. 16 below shows the actual communication performance of the proposed IR-UWB transceiver, collected from a real water quality WSN testing environment at normal temperature. To simplify measurement, data transmitted here is random bits. In this figure, the horizon axis is distance from transmitter (TX) to receiver node (RX), and the vertical axis is the maximum data rate, in Mbps. As the figure shows, the transceiver can achieve required performance: ~10 Mbps @ 10 m distance. When the distance between TX and RX increases to above 20 meters, the data rate falls to nearly zero, which is the upper limit of transmission distance.

6. Conclusion and Future Works

In this paper, a design of energy detection IR-UWB transceiver for RFID and wireless sensing applications has been presented. An innovative synchronization method called energy offset based

scheme and a threshold detection scheme are suggested in the proposed IR-UWB receiver. Simulation and FPGA implementation results show that the innovative receiver which requires only one integrator has almost the same performance with the traditional one using maximum energy search scheme, while significantly reduces the hardware complexity and power dissipation. Besides, it allows shorter preamble code length, which makes it more energy efficient and has less transmission overhead. The proposed transceiver has the possibility to achieve energy saving communication (~nJ/bit) and low complexity implementation. Due to its low-power low-cost advantages, this IR-UWB transceiver prototype is applied in a practical solar panel powered water quality monitoring WSN system. The transceiver works as a communication module in WSN nodes. Field testing results show that the maximum data rate can achieve ~10 Mbps in 10 m radius, much higher than WSN and VANET system requires.

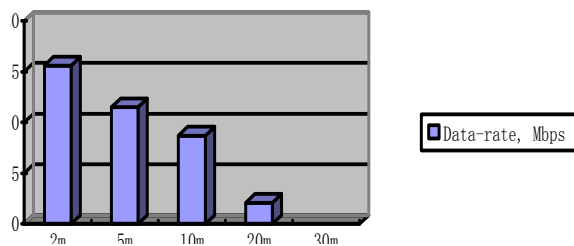


Fig. 16. Transceiver data-rate performance in field testing.

Future works will be focused on ASIC implementation of the proposed transceiver as a whole and its application in WSN at large amount. The works can be done in several aspects. Firstly, the synthesis for ASIC implementation could be done using Cadence design tools. Secondly, the backend design of the ASIC design flow could be done, for example, place and route. In the long term, the RF front-end and analog parts could be designed and simulated by ADS. We can get the suitable RF parameters which match the digital backend best. Other related works are the A/D converter design, performance & power measurement, and system integrations.

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