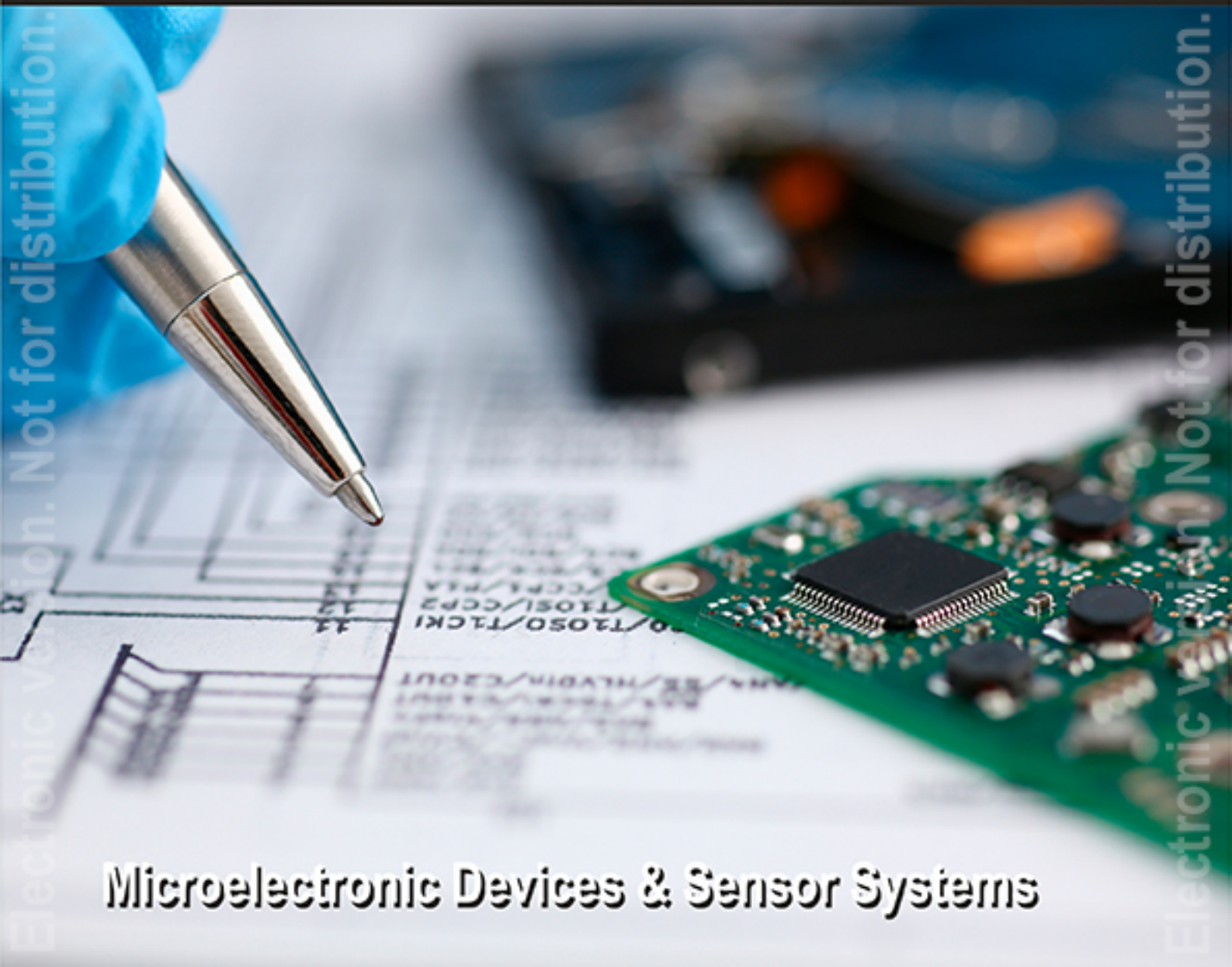
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Microelectronic Devices & Sensor Systems

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Editor-in-Chief
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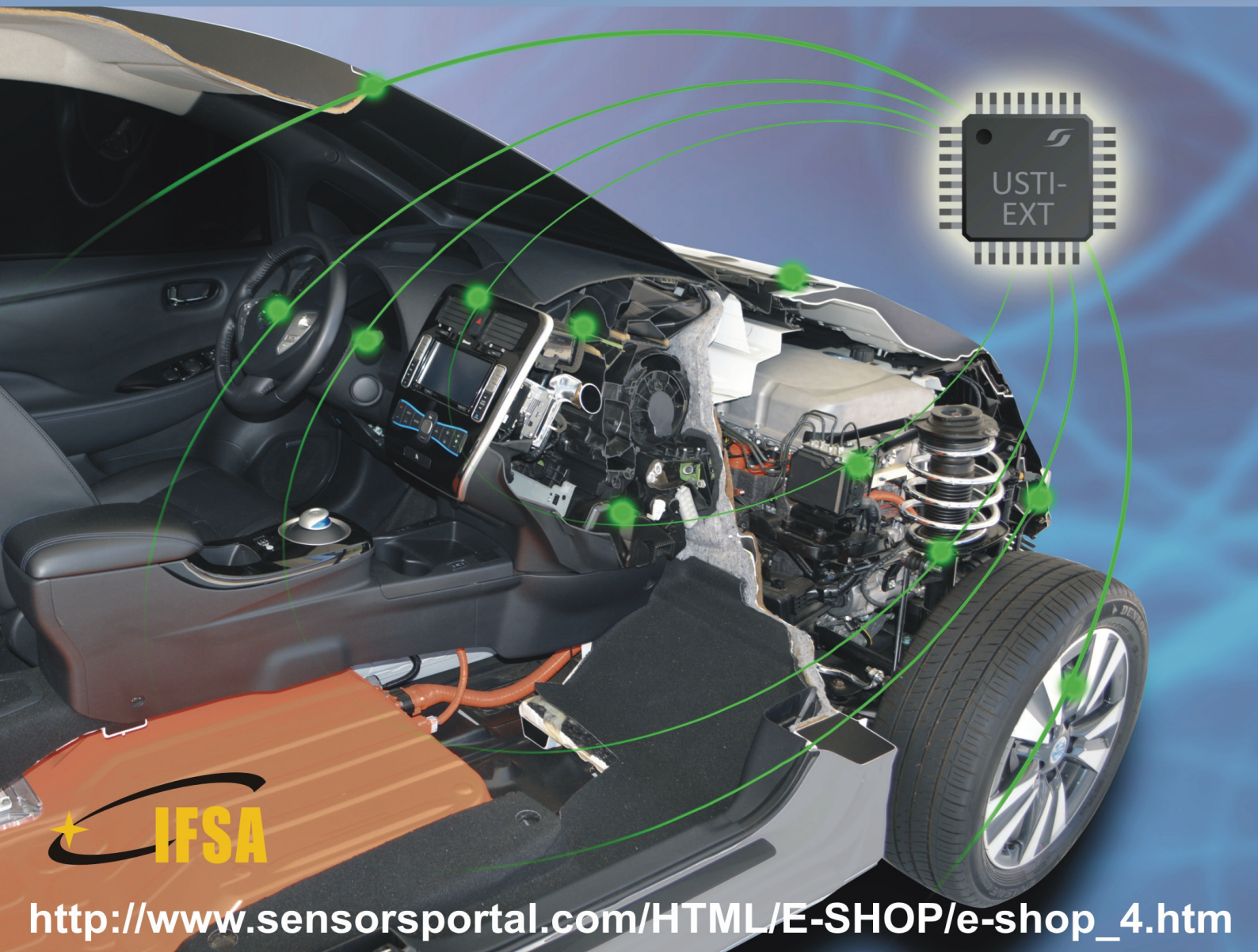




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Foreword to Special Issue

It is my great pleasure to introduce a special issue of *Sensors & Transducers* journal, titled '*Microelectronic Devices and Sensor Systems'*.

This journal issue contains selected and extended papers from the *1st International Conference on Microelectronic Devices and Technologies (MicDAT '2018),* which taken place on 20–22 June 2018 in Barcelona, Castelldefels, Spain.



The conference was organized by *International Frequency Sensor Association (IFSA)* with media partners - MDPI leading international peer-reviewed open access journals 'Low Power Electronics and Applications' (ISSN 2079-9268), 'Micromachines' (ISSN 2072-666X) and 'Sensors' (ISSN 1424-8220) Switzerland, in technical cooperation with *Excelera, S.L*, and *IFSA Publishing S.L*., Spain.



The annual MicDAT conference is intended to create awareness of the huge potential of modern microelectronic technologies and to improve understanding on the recent challenges in a wide range of applications. The many different technological bases for the fabrication of microelectronic devices, SoC, SiP, MEMS and NEMS where discussed during the conference.





A number of recognized experts from both: academy and industry in the field of microelectronic design were invited to give their view in selected application areas including three keynote speakers from Italy, Chile and Algeria; and two invited speakers from Singapore and India. In 2018 we have got more than 50 submissions, and after review, 33 papers have been selected for presentations (25 oral and 8 posters presentations) including keynote and invited presentations, submitted by authors from 20 countries (7 European and 13 non-European countries), covering theory, design, technology and applications of various microelectronic devices.



The conference was organized in one dedicated poster session and four regular sessions: 'Advances in Analog and Digital Circuits', 'Advances in Microelectronic Technology', 'Simulation and Emulations' and 'Applied Microelectronics'.

A limited number of the best articles from this journal issue will be selected for extension into book chapters for publication in our popular open access Book Series '*Advances in Microelectronics: Reviews*' Vol. 3, which will be published in 2019 in both formats: electronic and paper.

The 2nd *International Conference on Microelectronic Devices and Technologies (MicDAT '2018)* will take place in Amsterdam (The Netherlands) on 15-17 May 2019, when tulips bloom. The conference web site http://www.micdat-conference.com is up-dated. Please visit this site for more details.

I hope you will enjoy this journal issue !



Sergey Y. Yurish
Editor-in-Chief

Second International Conference on Microelectronic Devices and Technologies (MicDAT '2019)

http://www.micdat-conference.com/

MicDAT 2019

15-17 May 2019 • Amsterdam, The Netherlands

The conference is the 2nd of a series of International Conferences on Microelectronic Devices and Technologies (MicDAT) held in Barcelona, Castelldefels, Spain, 2018, organized by IFSA. The MicDAT' 2019 conference is intended to create awareness of the huge potential of modern microelectronic technologies and to improve understanding on the recent challenges in a wide range of applications. The many different technological bases for the fabrication of microelectronic devices, SoC, SiP, MEMS and NEMS will be outlined in this 3-day conference.

A number of recognized experts from both: academy and industry in the field of microelectronic design will be invited to give their view in selected application areas.

The aim of MicDAT series of conference is to provide an annual world forum for the presentation and discussion of recent advances in microelectronics, and bring together leading international researchers, engineers and practitioners interested on any of the microelectronics related technologies.

Topics of interests:

- Analog, digital, mixed, and RF circuits and related design methodologies
- Analog-to-Digital Converters (ADC)
- Voltage-to-Frequency Converts (VFC)
- Frequency-to-Digital Converters (FDC)
- Time-to-Digital Converters (TDC)
- Logic, architectural, and system level synthesis
- Nonlinear circuits
- Microprocessors, microcontrollers and DSPs
- Testing, design for testability, built-in self-test
- Area, power, and thermal analysis and design
- Mixed-domain simulation and design
- Embedded systems, low-power designs
- VLSI systems circuit and design
- Non-von Neumann computing and related technologies and circuits
- Design and test of high complexity systems integration
- SoC, MPSoC, NoC, SIP, and NIP design and test
- Process technologies, CMOS, BJT, BiCMOS, GaAs
- 3-D integration design and analysis
- Emerging device technologies and circuits, such as FinFETs, SETs, spintronics, SFQ, MTJ, etc.
- Design for Manufacturability/Technology
- Microelectronics processing and materials
- Semiconductor processing
- Solid-state electronics
- Quantum electronics
- Thin solid films
- Nanoprocessing, nanotechnology and nanofabrication
- Flexible and stretchable electronics
- MEMS and NEMS
- CAD tools for microelectronics
- Hardware/software co-design
- Algorithms, methods and tools for modeling, simulation, synthesis and verification of Ics
- Electronic materials science and technology
- Organic electronic materials and devices
- Microelectronics reliability and qualification
- Assembly and Packaging



Deadlines:

Submission (2-page abstract):	30 January 2019
Notification of acceptance:	28 February 2019
Registration:	15 March 2019
Camera ready (4-6 pages paper):	10 April 2019

Contribution Types:

- Keynote presentations
- Invited talks
- Special sessions
- Regular and Poster sessions
- Industrial presentations
- Exhibition



IFSA

Second International Conference on Microelectronic Devices and Technologies (MicDAT '2019)

Special Sessions:

Authors are welcome to organize and manage special sessions during the conference. Each session will contain 4-6 papers in a related field as specified above.

One event - three publications !

1) All registered abstracts will be published in the conference proceedings (Flash drive edition of published Proceedings with the ISBN).

2) Authors will be invited to submit full-page extended papers to special issue of Sensors and Transducers open access journal (ISSN 2306-8515, e-ISSN 1726-5479).

3) The limited number of full-page papers published in the journal will be selected by the Editorial Board to extend for book chapters for the open access Book Series on 'Advances in Microelectronics: Reviews' Book Series, Vol. 3.

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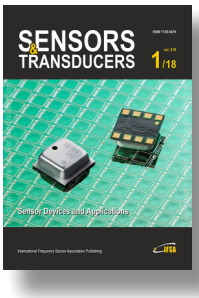
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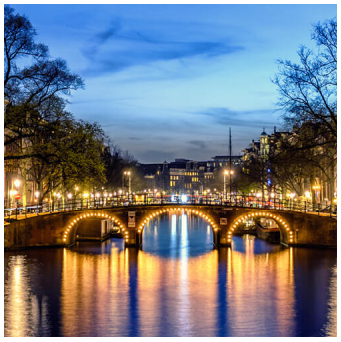


Gala Dinner and Social Programme

The Gala Dinner will take place on an Amsterdam comfort and elegant modern channel cruise boat, to enjoy the heritage-listed canals of the 'Venice of the North' in style. We will have a truly unique evening (a culinary and cultural trip all in one) in the beautiful Dutch capital - Amsterdam. It will be a treat for the eyes and stomach. You'll discover the enchantingly lit waters of Amsterdam by night as you savor the flavors of a hearty, gourmet dinner. Over the Gala Dinner, the cruise boat takes you to all the top spots, like the Western Church and Anne Frank House.









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130 nm CMOS SAR-ADC with Low Complexity Digital Control Logic

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Abstract: This paper reports on an original approach to design the digital control logic of a Successive Approximation Register Analog to Digital Converter, where no sequencers or code registers are used. It turns out a low complexity digital circuitry, which is applied to the design of a 130 nm CMOS 8-bit SAR ADC. The simulations demonstrate that the proposed digital control logic correctly works leading to an Analog to Digital Converter exhibiting performances well aligned with the literature in terms of linearity, dissipated power, and energy spent per bit generation.

Keywords: SAR-ADC, Control circuitry, CMOS, Shift register, Counter.

1. Introduction

The Successive Approximation Register Analog-to-Digital Converter (SAR-ADC), when compared with other ADC solutions (e.g. sigma-delta ADC, pipeline ADC), has its strengths in the low power consumption, medium-to-high resolution, and small form factor. Its weakness is in a high latency, as the conversion process requires operation cycles as many as the resolution. This mix of strengths and weakness makes the SAR-ADC very well suited for applications targeting low frequency signals and suffering from a limited energy availability. In medicine, the battery powering the integrated electronics front-end cannot be frequently replaced, because it is often implanted (e.g. pace-makers, heart defibrillators, epileptic seizure detector). In smart agriculture, the nodes of the sensor network distributed on a cultivation (e.g. vineyard) should work with a limited amount of available energy, because this energy should be harvested from the environment. Same consideration holds for the mobile sensors embedded in the collars for the smart monitoring of livestock (e.g. cow).

A SAR-ADC converts the value of the input analog signal, sampled at the given time, into a digital word generated after a given latency time elapsed from the sampling instant. The conversion process is based on a binary search algorithm, which explores a binary tree to find the best digital approximation, for a given resolution, of the input analog value. During the latency time the SAR-ADC explores this binary tree. The binary search algorithm is implemented in a digital control circuitry, which is usually constituted by sequencers and code registers [1-5], that makes complex the design flow. Aim of the present paper is to report on a low complexity approach to the design of the digital control circuitry [6]. The paper is organized as follows. Section 2 explains how the binary search algorithm can be implemented, in order to simplify the design of the digital control circuitry.

Section 3 focuses on the architecture and schematic of the proposed digital control circuitry. Section 4 applies the proposed digital control circuitry to the design of an 8-bit SAR-ADC in a bulk CMOS 130 nm CMOS technology. Section 5 reports on the performances obtained for the designed SAR-ADC. Eventually, the paper ends with Section 6, where some conclusions are drawn.

2. Binary Algorithm Implementation

Fig. 1 depicts the general architecture of a SAR-ADC. It is constituted by three main building blocks: the comparator, the Digital-to-Analog Converter (DAC), and the digital control circuitry, which is called hereinafter Digital Control Logic (DCL).

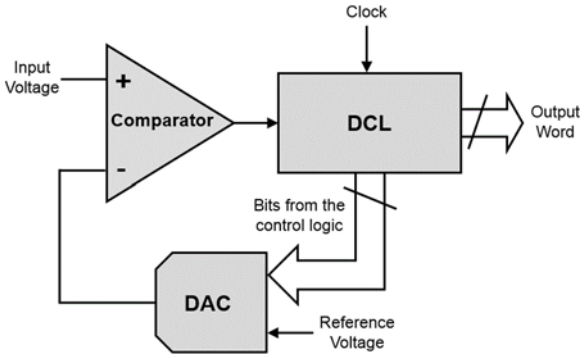


Fig. 1. General architecture of a SAR-ADC.

The present section addresses the implementation of the search binary algorithm run by the DCL. Generally speaking, the chosen implementation can make the design of the DCL more or less complex. In particular, in the present work the implementation was simplification orientated. For sake of clarity, a 4-bit resolution SAR-ADC is addressed.

The proposed approach moves from thinking of the DCL as a finite state machine, a point of view not adopted in the literature, even when the design sounds very close to a state transition diagram [2]. Fig. 2 depicts the state transition diagram for the DCL, described as a finite state machine. It is worth noticing that the state diagram reproduces the structure of a binary tree. The diagram is distributed on four layers. The first layer is the initial state. In the fourth layer are the final states obtained at the end of the digitization process. The DCL goes through the states following the outcome of the comparator around which the SAR-ADC is designed (see Fig. 1). Fig. 2 shows that in the approach proposed in the present paper, for a 4-bit resolution SAR-ADC, each state is encoded into six bits. The two right-most bits (in grey) count the layer (e.g. they are "00" for the first layer and "10" for the second layer). The remaining four bits (in black) track the sequence of the comparator outputs. In the initial state, these bits are all set to "1". After each comparison, these bits are right-shifted and the left-most one is replaced by the comparator outcome.

In the general case of an R-bit resolution ADC, the right-most bits in grey are in the number of the next higher integer of $\log_2 R$ and the remaining bits in black are in the number of R.

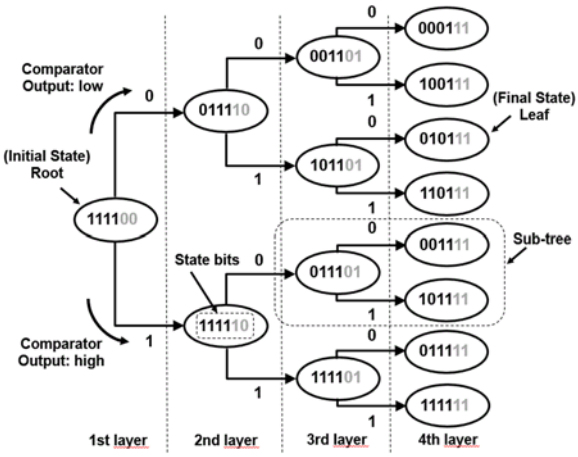


Fig. 2. State transition diagram for the DCL.

3. DCL Architecture and Schematics

The state encoding described in the previous section does not minimize the number of bits for the design of the finite state machine. In fact, four bits would be indeed enough to encode the fifteen states in Fig. 2. The advantage offered by the proposed state encoding is that the next state of the binary algorithm can be generated from the actual one by using a shift register for the bits in black and a counter for the bits in grey, making straightforward, in this way, the design of the DCL. The resulting architecture of the DCL is depicted in Fig. 3.

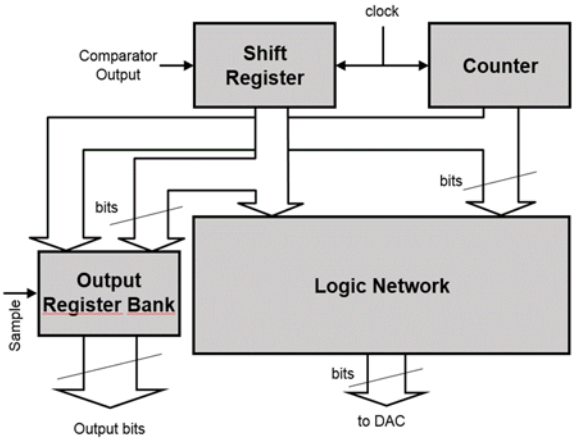


Fig. 3. Building block diagram of the DCL.

It is constituted by four main building blocks: a shift register, a counter, a logic network, and an output

register bank. Note that no sequencers and code registers are used. The shift register can be obtained by cascading four D-type registers as depicted in the following Fig. 4(a). The counter can be implemented as a binary counter obtained by arranging two D-type registers as in Fig. 4(b). Eventually, the output register bank is an array of four D-type registers as sketched in Fig. 4(c). In the case of a 4-bit resolution SAR-ADC, the design of the DCL requires therefore a total of ten D-type registers. The D-type register is therefore the basic cell to build up the DCL. In the present work, this register was designed by arranging in a master-slave configuration two transmission gates based latches, as depicted in the following Fig. 5.

Fig. 4 shows the ten D-type registers used in the case of a 4-bit resolution SAR-ADC. For a higher resolution R, the DCL can be quickly re-designed by just extending the register chains in Fig. 4. This consideration highlights the simplification in the design of the DCL allowed by the sub-optimal state encoding described in Fig. 2. The shift register and the output register bank, each needs a chain of R D-type registers and the binary counter needs a chain with a number of D-type registers equal to the next higher integer of $\log_2 R$. In the case of an R-resolution SAR-ADC the design of the DCL requires therefore a total of $2R+ \log_2 R$ registers.

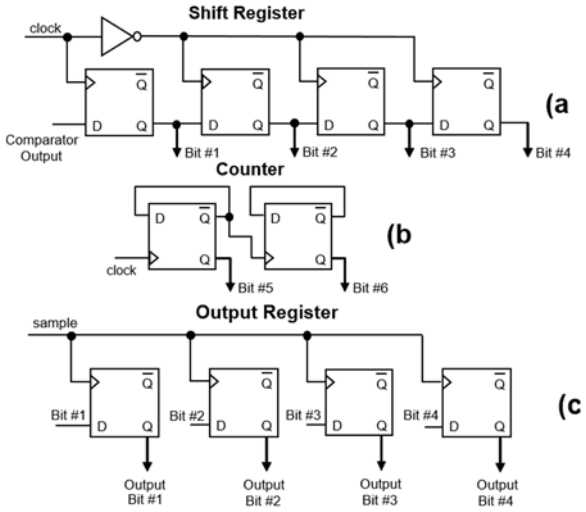


Fig. 4. Schematics of the shift register, the counter, and the output register bank in the case of a 4-bit SAR-ADC.

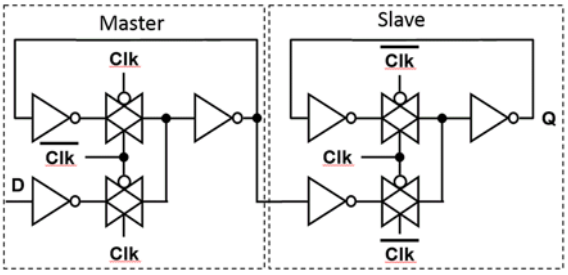


Fig. 5. Schematic of the D-type register.

The state encoding bits, as generated by the shift register and the binary counter, cannot be used directly to control the DAC. The logic network in Fig. 3 is in charge of translating the state encoding bits into signals useful to control the DAC. The design of this logic network depends therefore on both the implementation of the DAC and the specific architecture of the SAR-ADC.

4. 8-bit Resolution SAR-ADC

The previously described idea of DCL was applied to the design of an 8-bit resolution 130 nm CMOS SAR-ADC, whose architecture is depicted in the following Fig. 6. As in the case of the general architecture in Fig. 1, it uses one comparator and one DCL but, as a difference, it uses two DACs instead of only one. With the DAC implemented in the form of a switching capacitor network, as depicted in the following Fig. 7, this architecture allows for the minimization of the dissipated energy [2]. The use of two DAC's leads to a different way of using the comparator. In the general architecture the comparator receives the sampled value of the analog input signal V_{IN} to be digitized (see Fig. 1) while in the architecture in Fig. 6 V_{IN} is sampled by the DAC2 when the signal Sample is active. The comparator compares the voltages at the node Y and Z generated by the two DACs.

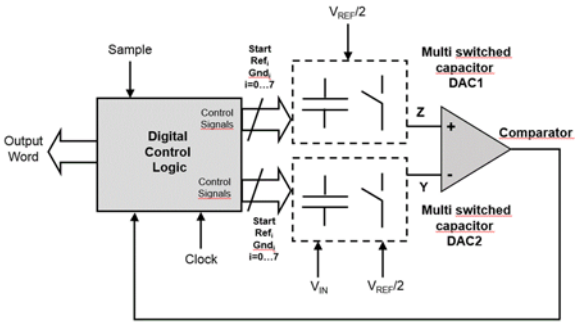


Fig. 6. Architecture of the designed 8-bit SAR-ADC.

For the architecture in Fig. 6, the logic network, has been designed to implement the following switching strategy. During the sample phase, the capacitors in the DAC1 are discharged with both plates at the potential $V_{REF}/2$, where V_{REF} is the reference voltage used for the conversion process, while the capacitors in DAC2 are charged at V_{IN}-$V_{REF}/2$. In the following phase, all Ref_i signals are forced to 1 and Gnd_i signals to 0. This phase generates the Most Significant Bit (MSB). The comparator outcome is used by the DCL to generate the future control signals for the two DACs. In particular, at the n^{th} comparison phase, the signal Ref_n is forced equal to the comparator outcome and the signal Gnd_n equal to inverse of the comparator outcome. At the same time, the signal Ref_{n-1} is forced to zero and the signal

Gnd_{n-1} to one. In this way, comparison by comparison the DCL explores the binary tree of Fig. 2 until the Least Significant Bit (LSB) is generated. For an 8-bit resolution SAR-ADC the logic network receives therefore eleven ($8+\log_2 8$) bits from the shift register and the binary counter and generates sixteen control signals Ref_i and Gnd_i (i=0…7). The logic network was synthesized through Karnaugh's maps and designed by using static NOR and NAND CMOS logic gates.

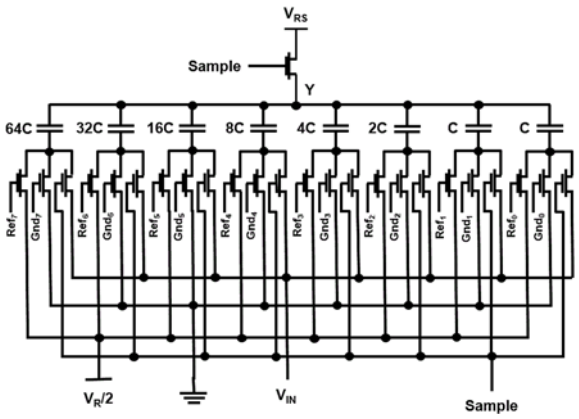


Fig. 7. Schematic of the DAC for the designed 8-bit SAR-ADC.

The comparator was designed as a dynamic latch, because of its higher sensitivity and lower dissipated power with respect to an operational amplifier based solution. Fig. 8 depicts the schematic of the designed dynamic latch comparator. Since the circuit is very sensible to capacitive mismatches at the output nodes, a dummy inverter was added at the output node of the comparator not connected to the DCL.

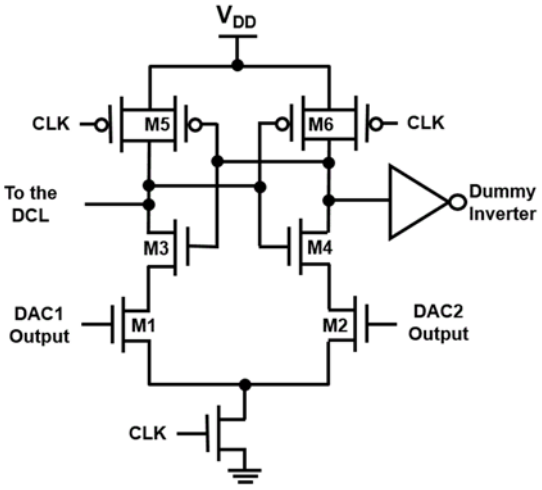


Fig. 8. Schematic of the dynamic latch comparator.

5. Simulations

As a first simulation, a sinusoidal tone with an amplitude of 800 mVpp and an oscillation frequency of 70 Hz was applied at the input of the designed SAR-ADC. The sampling frequency was set equal to 1.4 kS/s, the clock signal to 12.5 kHz, and V_{REF} to 800 mV. The following Fig. 9 shows a 12 ms time interval of the input signal. The figure highlights on the input waveform six samples (samples #2, #6, #9, #11, #13 and #16), whose values are reported in Table 1. Fig. 10 shows how the output bits are generated during the time for each of the previous six samples.

For example, the input sample #2, sampled in correspondence of the sampling pulse #2, is digitized during the time interval between this sampling pulse and the following sampling pulse #3. The output bits are made available in correspondence of the rising edge of the sampling pulse #3. It is therefore visible a latency time, spent by the DCL for exploring the binary tree (see Fig. 2) during the digitization process.

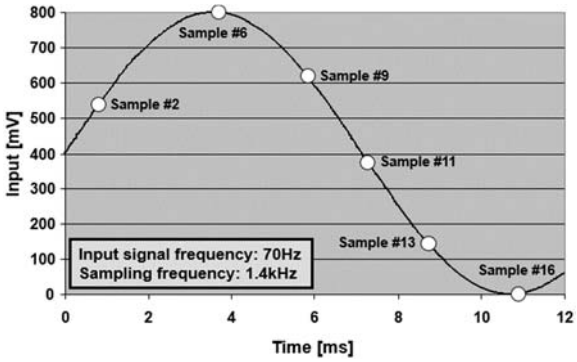


Fig. 9. Sampled values on the input sinusoidal waveform.

Table 1. Output words and quantization error.

Sample	V_{IN}, (mV)	Output Word	V_A, (mV)	ΔV, (mV)
#2	537.790	10101100	537.50	0.29
#6	799.560	11111111	796.88	2.69
#9	617.310	11000101	615.63	1.69
#11	374.780	01111000	375.00	0.22
#13	143.500	00101110	143.75	0.25
#16	1.120	00000000	0.000	1.12

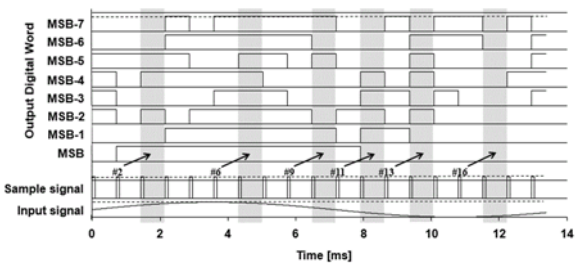


Fig. 10. Generation of the output digital word.

Table 1 reports also the voltage V_A computed from the output digital word using the usual formula:

$$V_A = V_{REF} \sum_{i=0}^{7} \frac{MSB - i}{2^{i+1}}, \qquad (1)$$

where MSB-i is the i[th] output bit, being MSB-0 the MSB and MSB-7 the LSB. The most-right column in Table 1 shows the quantization error ΔV between V_{IN} and V_A. It is possible to observe that ΔV is always lower than one LSB (3.13 mV). Table 1 provides therefore a first rough indication that the designed SAR-ADC is correctly working.

The performances of the designed SAR-ADC were more in depth tested by investigating the static parameters Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), and the dynamic parameters Equivalent Number of Bit (ENOB), Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), and Signal-to-Noise And Distortion ratio (SINAD), as well. The simulation set-up employed for these parameters are shortly sketched in the following Fig. 11. The ideal DAC was described in Verilog-A code. For INL and DNL (upper part of the figure) a slow linear voltage ramp covering the whole input dynamic range was applied at the input of the SAR-ADC under test. The stair-case ramp generated by the Verilog-A code DAC was analyzed in the time domain by investigating the distribution of the thresholds. The following Fig. 12 and Fig. 13 show the obtained DNL and INL, respectively.

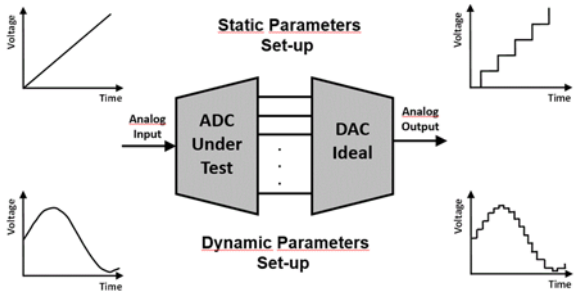


Fig. 11. Simulation set-ups for static and dynamic parameters of the SAR-ADC.

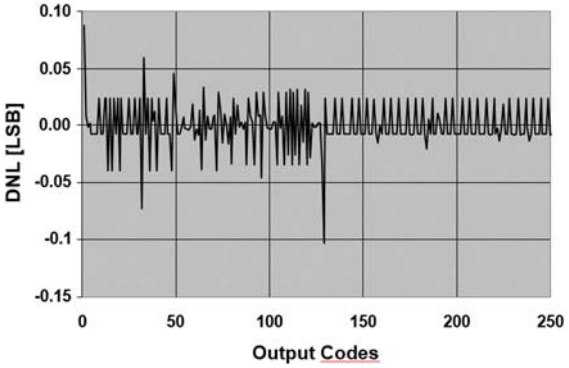


Fig. 12. Differential Non-Linearity of the designed SAR-ADC.

The DNL oscillates in the +/-0.05LSB range with exception for the code #128, where it exhibits a peak at around -0.1LSB. The worst DNL can be indeed expected when the MSB changes [7]. The INL is in the -0.15LSB/+0.10LSB range with a step in correspondence of the worst DNL.

For ENOB and SNR (lower part of Fig. 11) a 70 Hz sinusoidal tone was applied at the input and the stair-case waveform generated by the ideal DAC was analyzed in the frequency domain with a Discrete Fourier Transform. The following Fig. 14 shows the spectrum. The summation of the first eleven harmonics leads to a THD of 45.9 dB. By accounting for the process gain from the noise floor it is possible to compute a SNR of about 42.9 dB.

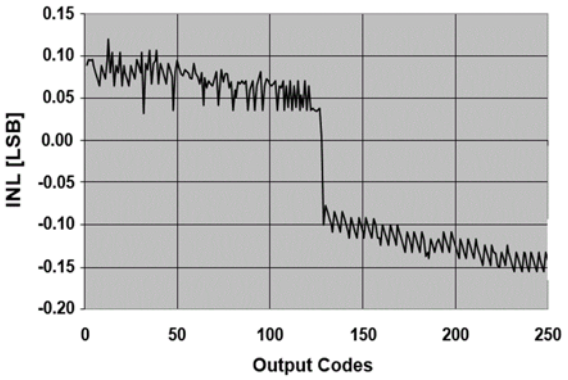


Fig. 13. Integral Non-Linearity of the designed SAR-ADC.

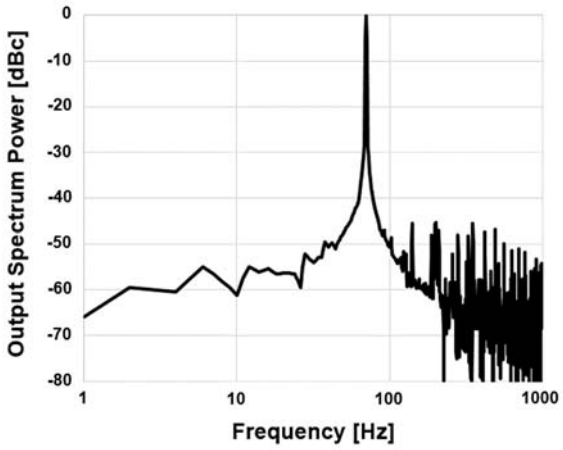


Fig. 14. Spectrum of the stair-case sinusoidal tone generated by the ideal DAC in the simulation set-up for dynamic parameters.

The following Equation (2) allows for computing the SINAD:

$$SINAD = -10log\left(10^{-\frac{THD}{10}} + 10^{-\frac{SNR}{10}}\right), \qquad (2)$$

which results to be 41.2 dB. Finally, through the following Equation (3) it is possible to compute the ENOB:

$$ENOB = \frac{SINAD - 1.76}{6.02}, \quad (3)$$

which results to be 6.5 bits.

THD can be also estimated from the INL through the following Equation (4) [8]:

$$THD = 20log \frac{INL_{MAX}}{2^{N-1}}, \quad (4)$$

where INL_{MAX} is the maximum observed module of INL and N is the number of bits. Since INL_{MAX}=0.15LSB from Fig. 13 and N=8 for the designed SAR-ADC, the equations from (2) to (4) provide therefore an ENOB of 6.8 bits. It is therefore possible to estimate an ENOB of 6.65 bits for the SAR-ADC proposed in the present work.

Table 2 compares the obtained DNL, INL and ENOB with those reported of other 130 nm CMOS SAR-ADCs in the literature. The present SAR-ADC well compares with the literature even if it suffers from a somewhat low ENOB.

Table 2. Output words and quantization error.

	[9]	[10]	[11]	This work
Resolution [bits]	8	10	8	8
DNL [LSB]	+/- 0.61	-0.61 / +0.54	-0.15 / +0.15	-0.05 / +0.05
INL [LSB]	+/- 0.63	-0.46 / +0.45	-0.35 / +0.23	-0.15 / +0.10
ENOB [bits]	7.6	9.1	7.8	6.7

The following Fig. 15 plots the dissipated power versus the sampling rate for several SAR-ADC collected in the literature regardless of the employed technology. The two dashed lines in the figure suggest that the power dissipated (P_D) by the SAR-ADC increases of 10 dB when the sampling frequency increases of one decade. Fig. 15 shows that the SAR-ADC proposed in the present work (open symbol in the figure) well compares with the literature.

A more homogeneous comparison with the state-of-the-art in the literature can be carried out through the following Figure-of-Merit (FoM) [11], [14]:

$$FoM = \frac{P_D}{f_s 2^{ENOB}} \quad (5)$$

It quantifies the energy dissipated to complete a conversion step. The following Fig. 16 plots this FoM versus the sampling rate for the SAR-ADCs already addressed in the previous Fig. 15. Even if with a FoM somewhat higher than the average value, the SAR-ADC described in the present work still remains comparable with other SAR-ADCs reported in the literature.

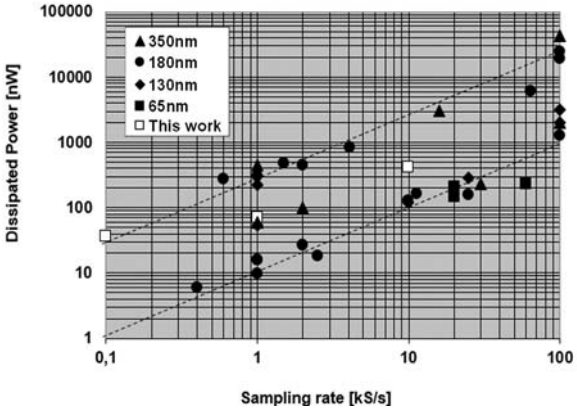


Fig. 15. Dissipated power versus sampling rate. References for 350 nm: [2], [12-16]. References for 180 nm: [2], [17-27]. References for 130 nm [10], [11], [28-31]. References for 65 nm: [32]

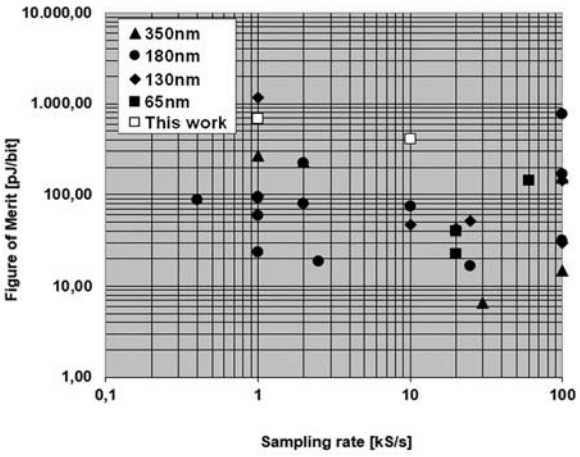


Fig. 16. FoM versus sampling rate. References for 350 nm: [2], [12-16] References for 180nm: [2], [17-27]. References for 130 nm [10], [11], [28-31]. References for 65 nm: [32].

6. Conclusions

The present paper proposes the design of a low complexity digital control circuitry for SAR-ADC. The elementary cell for the design of this control circuitry is a D-type register. The obtained control circuitry results to be of low complexity. It is indeed constituted by two chains of registers, whose lengths can be easily accommodated to the desired resolution.

The proposed digital control circuitry was applied to the design of an 8-bit resolution SAR-ADC in a 130 nm CMOS bulk technology. The simulations demonstrated that the designed SAR-ADC correctly works exhibiting performances well comparable with the literature in terms of DNL, INL, and dissipated power. The only weakness was the ENOB, which results to be less performant without nevertheless severely affecting the energy spent per bit generation that remains comparable with the literature.

Acknowledgements

The authors would like to acknowledge STMicroelectronics for providing the 130 nm CMOS technology Design Kit. The technical contribution of Luca Toni is also warmly acknowledged.

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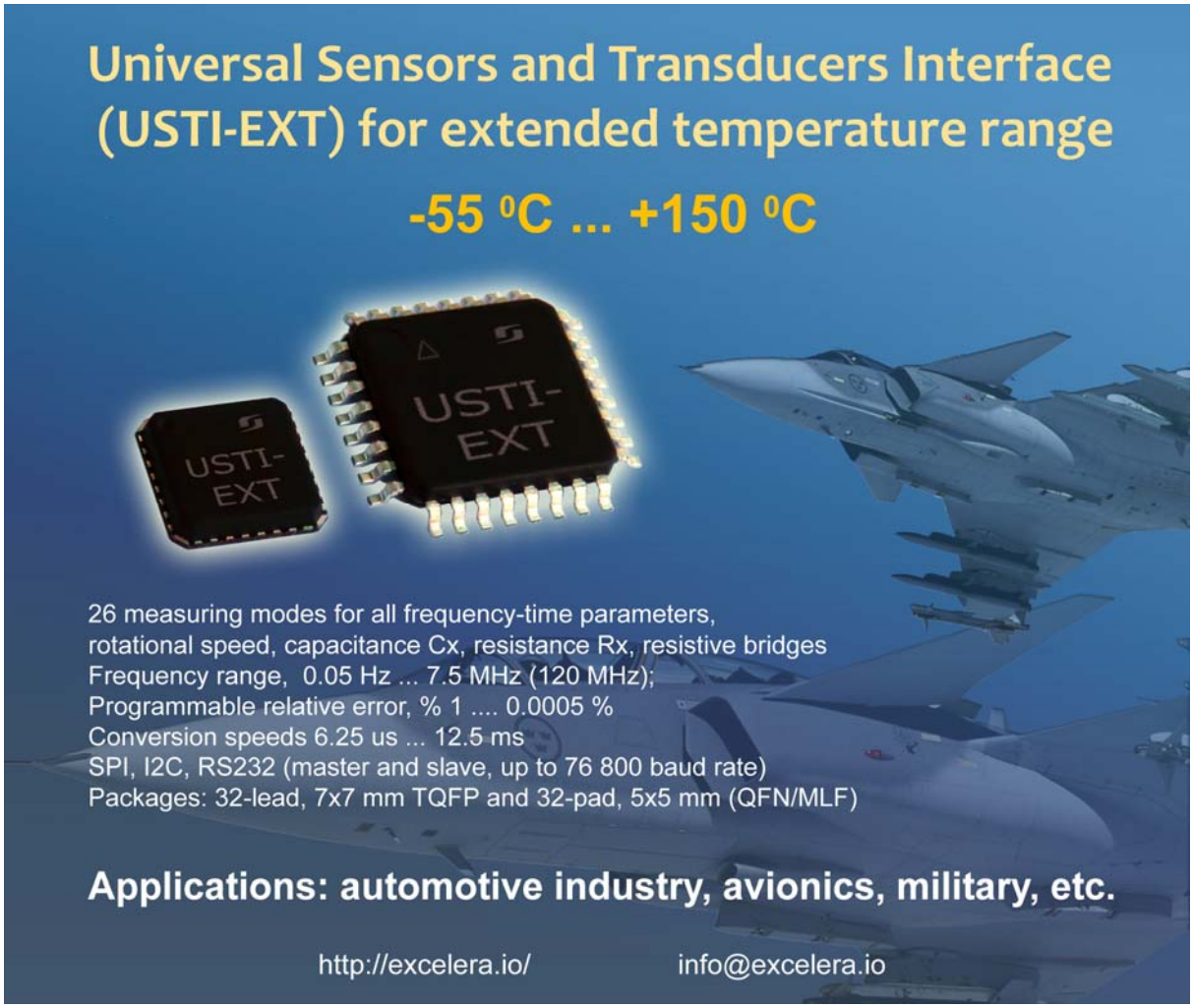
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Fully Differential Operation Amplifier Using Self Cascode MOSFET Structure for High Slew Rate Applications

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Abstract: In this paper, an adaptive fully differential OPAMP using Self Cascode MOSFET Transistors giving a maximum differential gain 75.31 dB with slew rate of 14.58 V/µS has been presented. In comparison to conventional 2 stage operational amplifier design, proposed design with adaptive bias has slew rate increased by 7× for a capacitive load of 3 pF. An adaptive bias circuit with current reference circuit is also designed using Self Cascode MOSFET Transistors to get reference current varying by only 20 nA when temperature varies from 25ºC to 100ºC. A Common Mode Feedback circuit designed using Self Cascode MOSFET Transistors shows only 0.01 % variation in Vocm as Vicm varies by 1 V. The proposed OPAMP has been developed in a standard TSMC 0.18 µm CMOS technology and the simulations are done using Cadence software.

Keywords: Self cascode, Slew Rate, High DC Gain, Adaptive bias, Common Mode Feedback, Operational Amplifier, Current reference.

1. Introduction

The decrement of supply makes difficult to implement useful analog circuits, so novel circuit architectures have to be introduced. The values of the current sources inside the amplifiers are the main responsible of quiescent power dissipation. Adaptive bias boosts the bias current of the input differential pair when large signals are applied, thus increasing circuit dynamic characteristics without affecting stand-by dissipation. In this paper we propose a novel rail-to-rail fully differential self cascode (SC) operational amplifier (OPAMP), showing enhanced gain characteristics, where DC gain has been enhanced by a technique which increases the output impedance of the OTA input stage through a regenerative feedback [1-2].

Fig. 1 shows the variation of Rout with length of M1 in SC, where "Ls" and Ld are transistor lengths for M1 and M2 respectively in SC already published in [2] but reproduced here. Using this a highly optimized SC can be obtained by just varying the length of M1 resulting in maximum gain of OP AMP. SC is also used in the design of current mirrors in this paper.

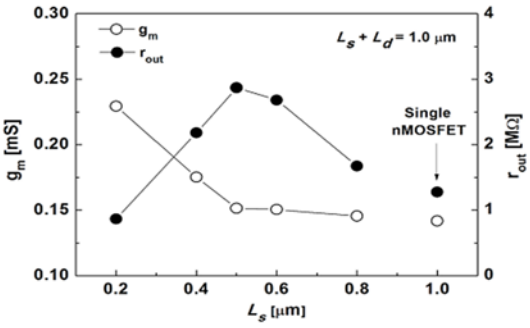


Fig. 1. Variation in Gm, and Rout of SC with variation in Ls and Ld [2].

2. Design Methodology

2.1. Self CascodeTransistor

Fig. 2 shows an NMOS SC configuration with gates shorted together and width of upper transistor is **m** times the lower transistor where **m**>>1. Length can be adjusted between the two so as to get the optimized trans-conductance gm_{eff} and output résistance R_{out}. For this design, Ln=400 nm (for M1) and Ln=600 nm (for M2) transistor.

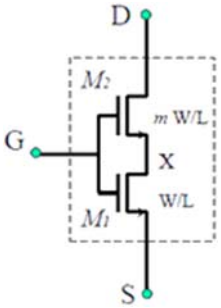


Fig. 2. Self Cascode Transistor.

Fig. 3 shows that gm_{eff} of SC increases with decrease in length but its R_{out} increases. Hence, an optimum value for gm_{eff} and r_o needs to be found out which will provide highest gain as compared to non SC transistor. Similar but complementary setup is made and used for pMOS transistors.

For a V_{DS} varying from 0 to 3.3 V, 'gm_{eff}' graphs are plotted in Fig. 3. As observed in simulations, gm_{eff} and R_{out} are functions of length of M1 transistor.

Fig. 4 shows circuit for computing equivalent resistance R_{out} of SC. Equivalent trans-conductance 'gm_{eff}' and R_{out} of SC are as computed below in Eq. (1) and (2).

$$R_{out} = (g_{m2}r_{o2}r_{o1} - r_{o2} - r_{o1}) \approx (g_{m2}r_{o1} - 1)r_{o2} = (mg_{m1}r_{o1} - 1)r_{o2} = (m-1)r_{o2} \quad (1)$$

$$g_{meff} = \frac{g_{m2}}{m} = g_{m1} \quad (2)$$

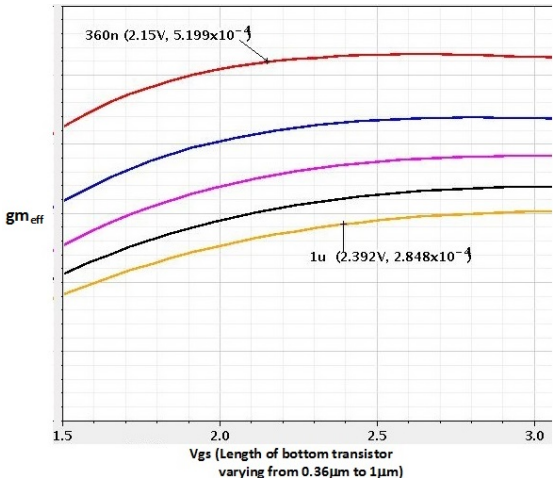


Fig. 3. Variation of gm_{eff} versus Vgs.

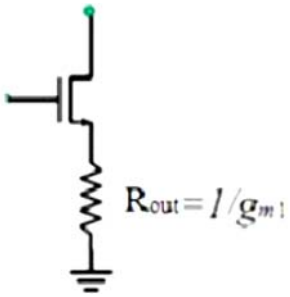


Fig. 4. Circuit for equivalent impedance of SC.

2.2. Operational Amplifier Schematic

Here, a positive feedback has been provided at the PMOS stage which gives us a gain increment of about 35 dB as compared to classical two stage cascode OPAMP at 1 MHz operating frequency.

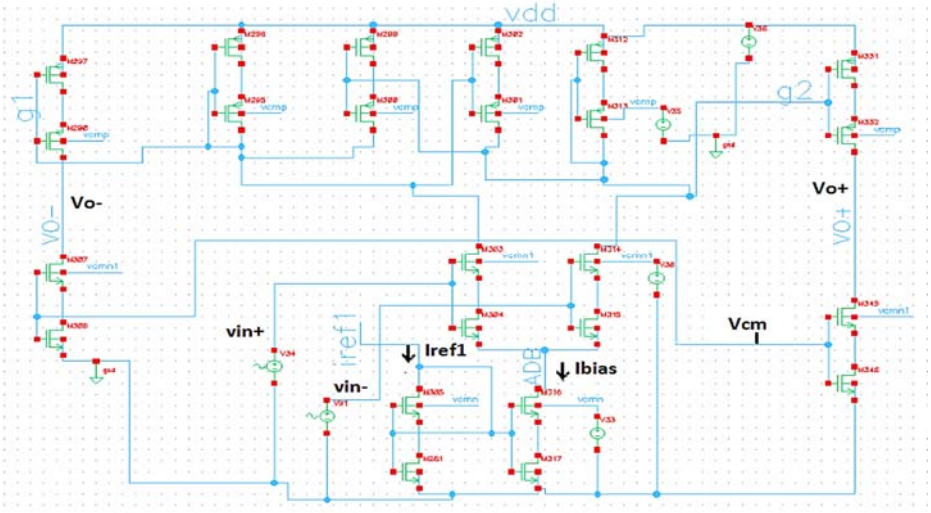


Fig. 5. Schematic design of proposed OPAMP [4].

Fig. 6, Fig. 7 and Fig. 8 shows frequency response of proposed OPAMP for differential mode gain (Adm), Adm with frequency compensation and common mode gain (Acm) respectively.

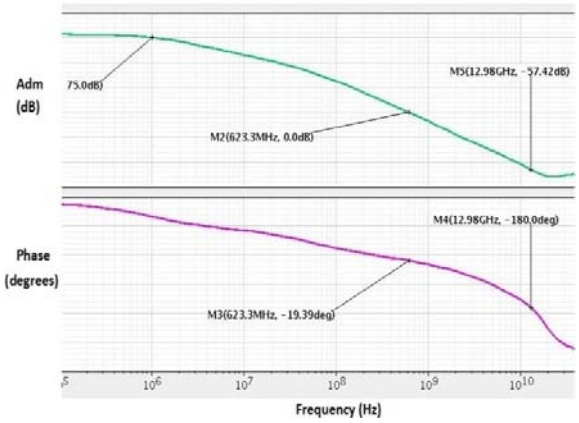


Fig. 6. Differential mode gain (Adm) of proposed design versus frequency.

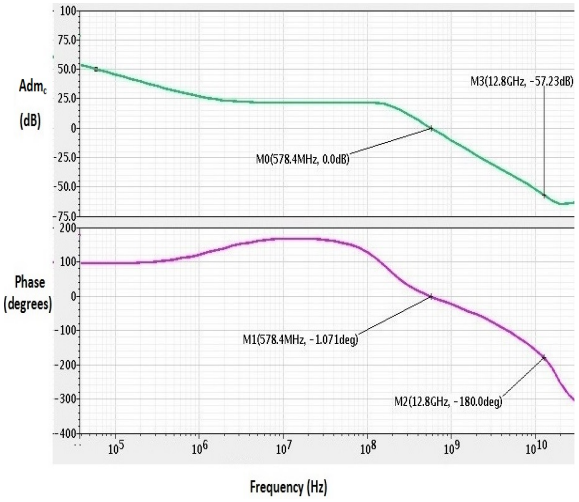


Fig. 7. Adm of proposed OPAMP with R-C miller compensation at second stage Vs. frequency.

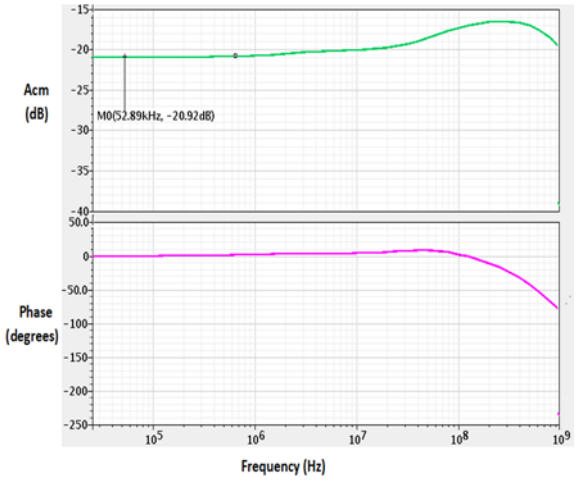


Fig. 8. Common mode gain (Acm) of proposed design versus frequency.

Table 1 shows the tabulated values of characterizing parameters of proposed and conventional OPAMP.

Table 1. Simulated values of characterizing parameters of proposed OPAMP.

No.	Parameter	Proposed Self cascode OPAMP Design	Conventional 2-stage CMOS OPAMP
1.	DC Differential Mode Gain, Adm, (dB)	75.31	40
2.	DC Common mode Gain, Acm, (dB)	-20.92	–
3.	CMRR (dB)	99.23	–
4.	Bandwidth (UGB) (MHz)	623.12	0.75
5.	Phase Margin (deg)	82	–
6.	PSRR (dB)	53.86	–
7.	ICMR (mV)	700	–
8.	OCMR (mV)	800	1000
9.	Slew Rate (58 V/μS)	14.58	2.3

2.3. Novel Current Reference Circuit Using SC

Typically CMOS reference current, Fig. 9 is designed using a CMOS Widlar source mirror and a passive resistor.

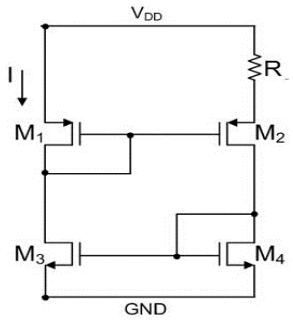


Fig. 9. Wildar reference current Generation [5].

The precision of the reference current depends on the complete value of the resistor. A slight variation in the resistor value can degrade the performance over temperature and process corners as current I is proportional to inverse of mobility and square of resistance. Since μp (mobility of pMOS) is a temperature dependent variable that reduces with temperature, the reference current 'I' *will increase with temperature.* Also, the mobility will change with carrier concentration, which makes the reference current sensitive to process variations too.

Thus in proposed OPAMP, a current reference is designed with only MOS transistors using SC as shown in Fig. 10 generating a 10 µA in each arms.

Here, instead of using resistor, a SC is replaced in linear region. PMOS Transistor pairs e.g. (M11, M12) in Fig. 10 is biased in deep triode region so that even if temperature increases, (M11, M12) remains in linear region. Thus a better stability with respect to temperature can be obtained by varying the W/L of Transistor pair (M11, M12).

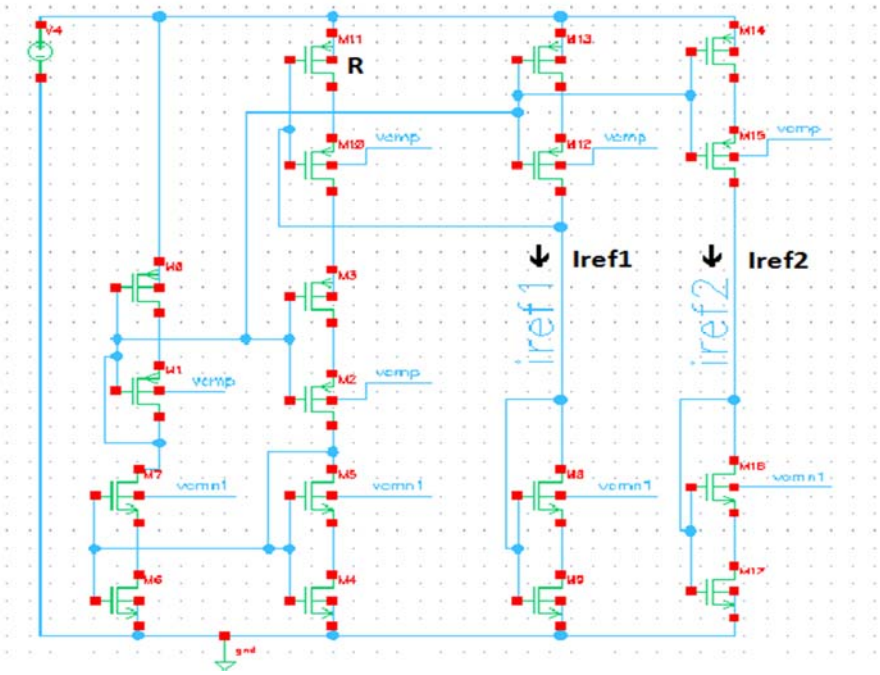


Fig. 10. Proposed current reference design using SC.

Fig. 11 shows the variation of only 0.02 uA in reference current I_{ref} with 50° change in temperature.

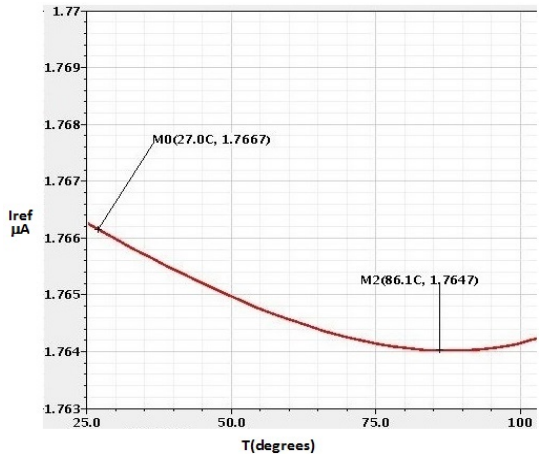


Fig. 11. Variation of reference current Iref w.r.t temperature.

2.4. Adaptive Bias Circuit

An adaptive bias circuit is designed for slew rate improvement. The circuit is shown in Fig. 12.

Basic current subtractor is realized in differential arms to provide extra current as seen from Eq. (4),

$$I_{total} = I_{bias} + A * \mathrm{mod}(I_2 - I_1) \quad (4)$$

I_1 and I_2 are current in branches close to main I_{bias} current mirror branch in differential tail branch.

$$I_{total} = I_{bias}(1 + A + A^2 + ...) \quad (5)$$

To ensure transistors to remain in saturation it is necessary to have value of parameter A<1 but not too less than 0.5 as it will reduce slew rate. I_{total} forms a geometric progression because of the positive feedback for A<1 as in Eq. (5).

For A= 0.9, current I shows 10 times improvement in slew rate as observed in Fig. 13 and Fig. 14.

2.5. Common Mode Feedback Circuit

Common mode feedback circuit is designed to maintain stable DC value at output, which will stabilize from process variations. CMFB senses voltage Vout should remain constant with V_{CM} variations. This is achieved by adjusting the current of Ibias, i.e. supplying it whenever needed to maintain constant Vocm. Instead of using resistive sensing, we have used all SC in implementation of CMFB [6] as shown in Fig. 15.

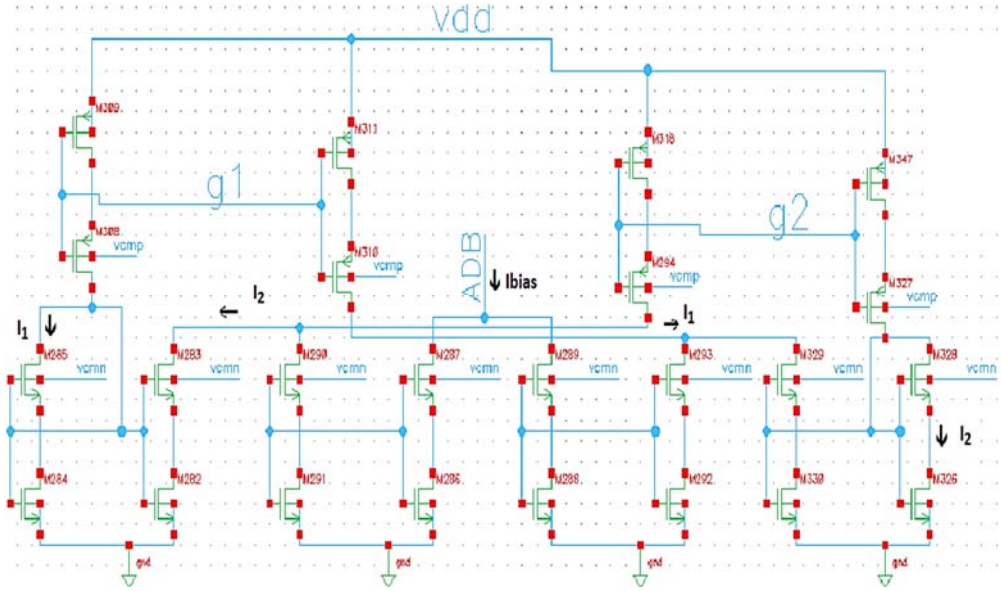


Fig. 12. Adaptive bias circuit [4].

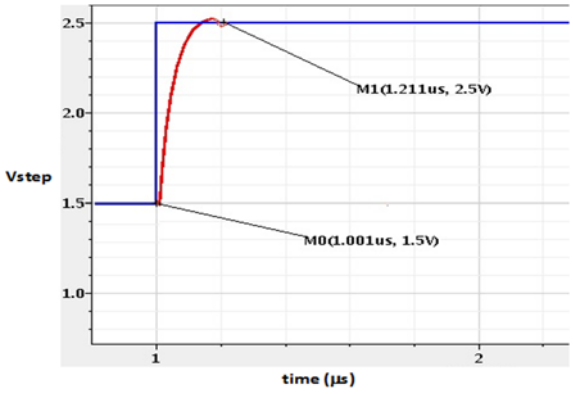


Fig. 13. Step voltage response of proposed OPAMP with time without adaptive bias, Slew Rate =2.3 V/µS.

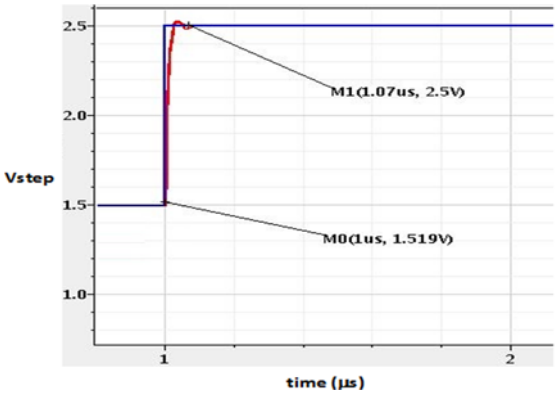


Fig. 14. Step voltage response of proposed OPAMP with time with adaptive bias, Slew Rate =14.58V/µS.

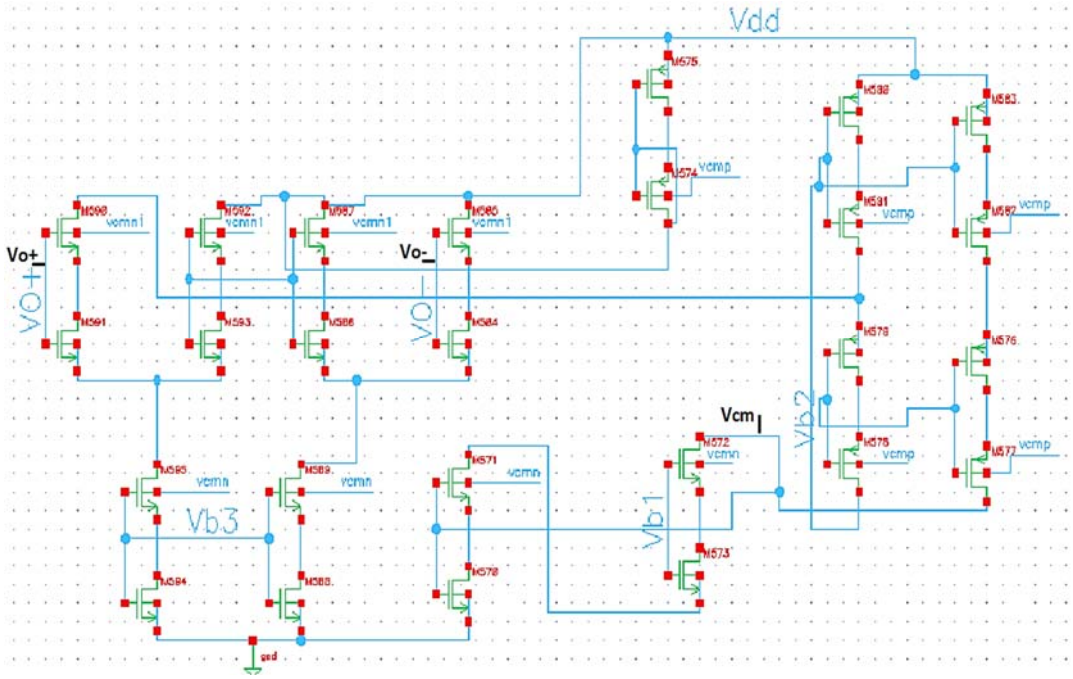


Fig. 15. Common Mode Feedback Circuit (CMFB) circuit.

As observed in Fig. 16, CMFB circuit tries to level the output to a constant value, within 0.01 % for Vicm varies from 1.5 to 2.5 V in differential mode operation.

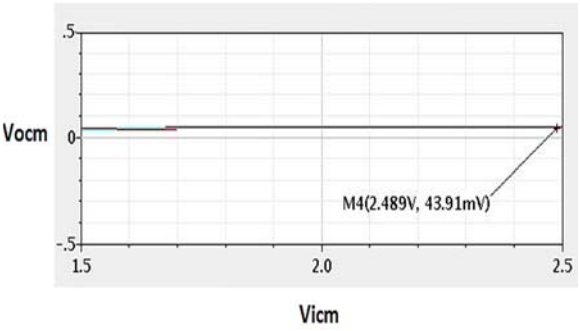


Fig. 16. Variation of Voutcommon mode (Vocm) w.r.t input common mode voltage Vicm varying from 1.5 to 2.5 V.

3. Conclusion

This paper presents a high performance 2 stage OPAMP design using SC based on the concept of dual-work function gate devices. Both the trans-conductance gm_{eff} and output resistance 'R_{out}' are optimized by channel length ratio of the SC MOSFETs. SC MOSFETs optimized for trans-conductance and output resistance are utilized in both input differential and output stages of the OPAMP. The DC gain improvement has been achieved by using partial positive feedback technique. This technique improves gain and bandwidth of the circuit. The measured DC gain of the proposed OPAMP is 35 dB higher, and slew rate is 7 times higher than that of the conventional 2 stage cascode OPAMP.

The proposed OPAMP has a power efficient high DC gain adaptive bias circuit which utilizes current subtractor based on CCM for providing extra tail current sources in addition to fixed bias current sources. The current subtractor provides the variable bias i.e. adaptive biasing, in the presence of input signal by providing additional bias current when the large signal is applied. The proposed circuits can be widely used in various signal processing applications such as filters, data convertors, resistors, inductors, integrators etc.

Acknowledgements

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Behavior Analysis of a Simultaneous Read/Write Nanoelectronic SRAM

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Abstract: This work presents and analyzes a fully working single-electron transistor (SET) based SRAM with individual read and write addressing for simultaneous operation. The SET-based SRAM presents smaller area, lower power consumption and lower latency time, making it ideal for devices with small area and low power consumption demands such as Systems-on-Chip (SoCs).

Keywords: SRAM, SET, Nanoelectronics.

1. Introduction

The capability of storing and retrieving large amounts of information is essential for most modern digital systems. The structured storage of bits, usually as a two-dimensional array, is defined as a memory [1]. One of the types of memories used in modern systems is the Random-Access Memory (RAM). The RAM is a volatile read/write memory in which the access time for read and write operations is independent of the data location in the memory array. The Static RAM (SRAM) is a type of RAM in which the written data remains stored while there is power applied to the system.

Area and dissipated power are limiting factors in improving the performance of mobile and Systems-on-Chip (SoCs) devices [2]. About 70 % of the area of a SoC chip is occupied by the SRAM memory [3]. Using a nanoelectronic device instead of CMOS transistors within the SRAM could be the solution to these limitations.

Particularly the single-electron transistor (SET) present attractive features like reduced dimensions, extremely low power consumption and low noise behavior. Single-electronic devices are able to control the movement of individual electrons through the tunneling phenomenon, i.e., the nonzero probability that the electron will be transmitted through a potential energy barrier [4].

This work presents and further analyze a fully working nanoelectronic SRAM based on the SET transistor with individual read and write addressing [5].

2. Single-Electron Transistor

The SET consists of two tunnel junctions connected together, forming an island between them (Fig. 1) [6]. Its operation is based on the flow control of single electrons (or small groups of electrons) by tunneling. That leads to very low power consumption, noise and device dimensions. The gate voltage

manipulates the Fermi level, i.e., the highest energy level occupied on the island, thus controlling the electrons conduction through the transistor [7].

The disadvantages of the SET include low gain, high susceptibility to offset charges, and high temperature operation issues. However, the operation of SETs up to 350 K has already been reported [8]. In this work, a SPICE model for the SET, which operates at room temperature, proposed by and available at Lientsching, *et al.* [9] was employed.

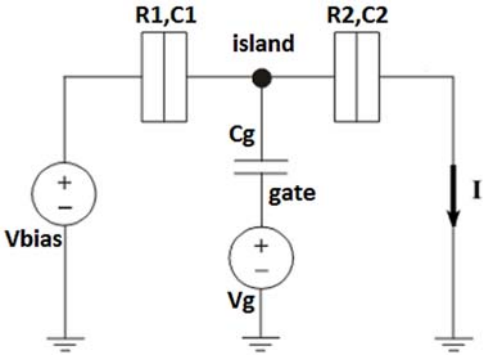


Fig. 1. Single-electron transistor.

3. SRAM Architecture

A generic SRAM architecture (Fig. 2) is composed of storing cells, read and write control, and address logic. The cells store 1 bit in a latch or flip-flop device and are usually arranged in a $m \times n$ matrix, where m corresponds to the number of arrays (words) that can be stored in the memory, and n represents the number of bits each array contains. They also contain the read/write logic that selects the operation to be executed, and a select control that enables the operation of each cell.

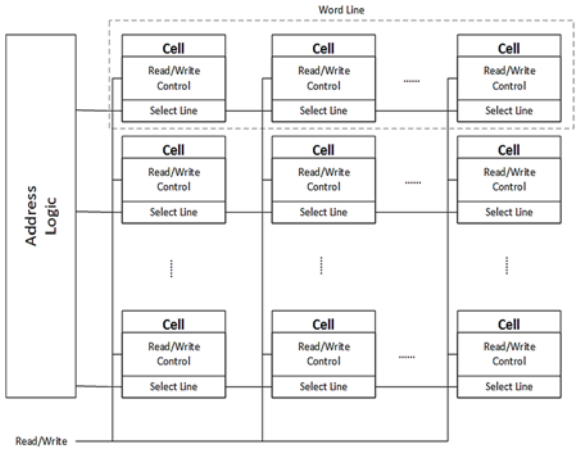


Fig. 2. Generic SRAM architecture.

The address logic allows each array of the memory matrix to be selected individually. As both read and write operations are controlled by one control, only one operation can be executed at a time, which generates a latency during the SRAM operation.

The developed SRAM module can store 8 words of 8 bits and presents separate controls for read and write addressing, allowing an individual and simultaneous execution of these operations (Fig. 3). The module is completely digital, and it can be combined with more modules to further expand the SRAM storage capacity.

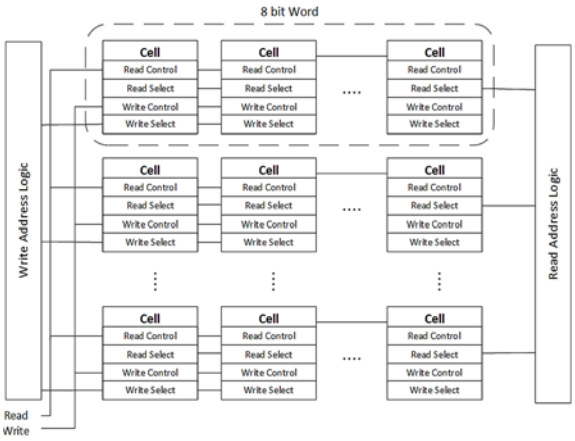


Fig. 3. Proposed SRAM architecture.

All the components of this digital architecture were designed with a nanoelectronic gate (nanoNAND) as base element (Fig. 4), which in turn is composed of SET transistors. All simulations were made using the LTSpice software [10]. Its building blocks are presented in the next subsections.

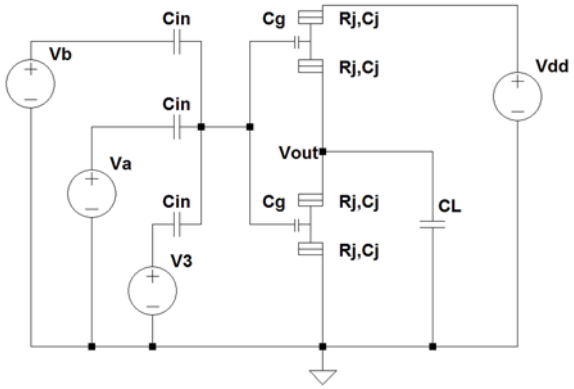


Fig. 4. Nanoelectronic NAND gate architecture.

3.1. Nanoelectronic NAND Gate

The NAND gate can be used to implement any Boolean function due to its functional completeness property. All the components of this digital architecture were designed with a nanoNAND as base element, including the NOT gate.

Various nanoNAND based on SET devices have been previously proposed in the literature [11-12]. The nanoNAND used in this work is the one redesigned at Silva, *et al.* [13] (Fig. 4). This choice was made because this specific nanoNAND configurations allows its simulation at ambient temperature. This nanoNAND is a programmable gate and its parameters are presented in Table 1.

In Fig. 4 voltages V_a and V_b are the inputs A and B of the digital signals. Voltage V3 is a select input that enables a NOR function on the output of the gate when its value is high (0.5 V) or a NAND function when its value is low (0 V). The nanoNAND is composed of two SET transistors.

Table 1. NanoNAND gate parameters.

Parameters	Value
R_j	1 MΩ
C_j	0.001 aF
C_{in}	2 aF
C_g	0.15 aF
C_L	0.25 aF
V_{dd}	0.5 V
V_3	0 V

3.2. SRAM Cell and Array

The SRAM cell consists of a flip-flop D, which can store 1 bit. The cells are arranged in an array of 8 bits, constituting a word. Each array consists of the 8 bits entries, a clock and an asynchronous clear, read and write signals to indicate the current operation and independent select signals for each operation, which are used by the addressing logic (Fig. 5).

In order for the read/write operation to occur in the m^{th} word, both the corresponding operation signal and operation address should be selected in the m^{th} array. Because it is possible to realize a simultaneous read and write operation in the same array, an unstable situation could be reached in the output. To avoid this problem both operations are also regulated by the system's clock. The write operation is executed only during the rising of the clock signal, while the read operation is executed when the clock signal is low.

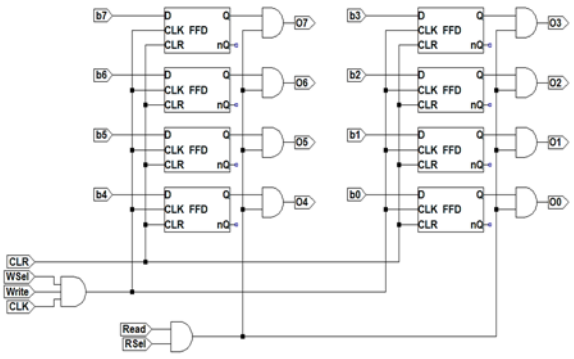


Fig. 5. SRAM array.

3.3. Read and Write Addresses

Because the proposed SRAM contains 8 memory arrays (words), read and write addressing are done through separated 3 to 8 decoders. An array address is then a 3-bit number that should be input in the corresponding operation decoder.

4. Simulation

The simulations were done through the software LTSpice. In this phase a test was presented to evaluate the correct functioning of the SRAM. The test consisted of writing two different 8-bit words on address 3 and 7 (Table 2), respectively, and retrieving them later.

The simultaneous read/write feature was also assessed during the test. Table 3 presents a timetable for when the write and read actions occurred and what addresses they accessed.

Table 2. Words for SRAM testing.

Add.	b7	b6	b5	b4	b3	b2	b1	b0
3	1	0	0	1	0	1	1	1
7	1	1	0	1	1	0	0	1

Table 3. Read/Write actions timetable.

Time (ms)	Write Action	Write Address	Read Action	Read Address
0 – 0.5	1	3	0	-
0.5 – 1	0	-	1	3
1 – 1.5	1	7	1	7
1.5 – 2	0	-	1	7

5. Results

The results of the test presented during simulation shows that the nanoelectronic SRAM works correctly. The write, read, addressing and simultaneous read/write functions perform as expected, as shown on Fig. 6.

The complete nanoelectronic SRAM has a total of 1890 nanoNANDs. The area of 1 nanoNAND is 172 nm² and 3.5 pW [13] and its dissipated power can be calculated by using equations 1 to 3. The total dissipated power is given by the sum of the static and dynamic powers. Table 4 presents the values for area and dissipated power for 1 nanoNAND, 1 array (word), 1 decoder, and the complete SRAM.

$$P_{dissipated} = P_{static} + P_{dynamic}, \quad (1)$$

$$P_{static} = V_{dd} \times I_{max}, \quad (2)$$

$$P_{dynamic} = f \times {V_{dd}}^2 \times C_L \quad (3)$$

The complete SRAM has an area of 0.325 μm² and dissipates 6.6 nW, which highlights the advantages of a nanoelectronic SRAM.

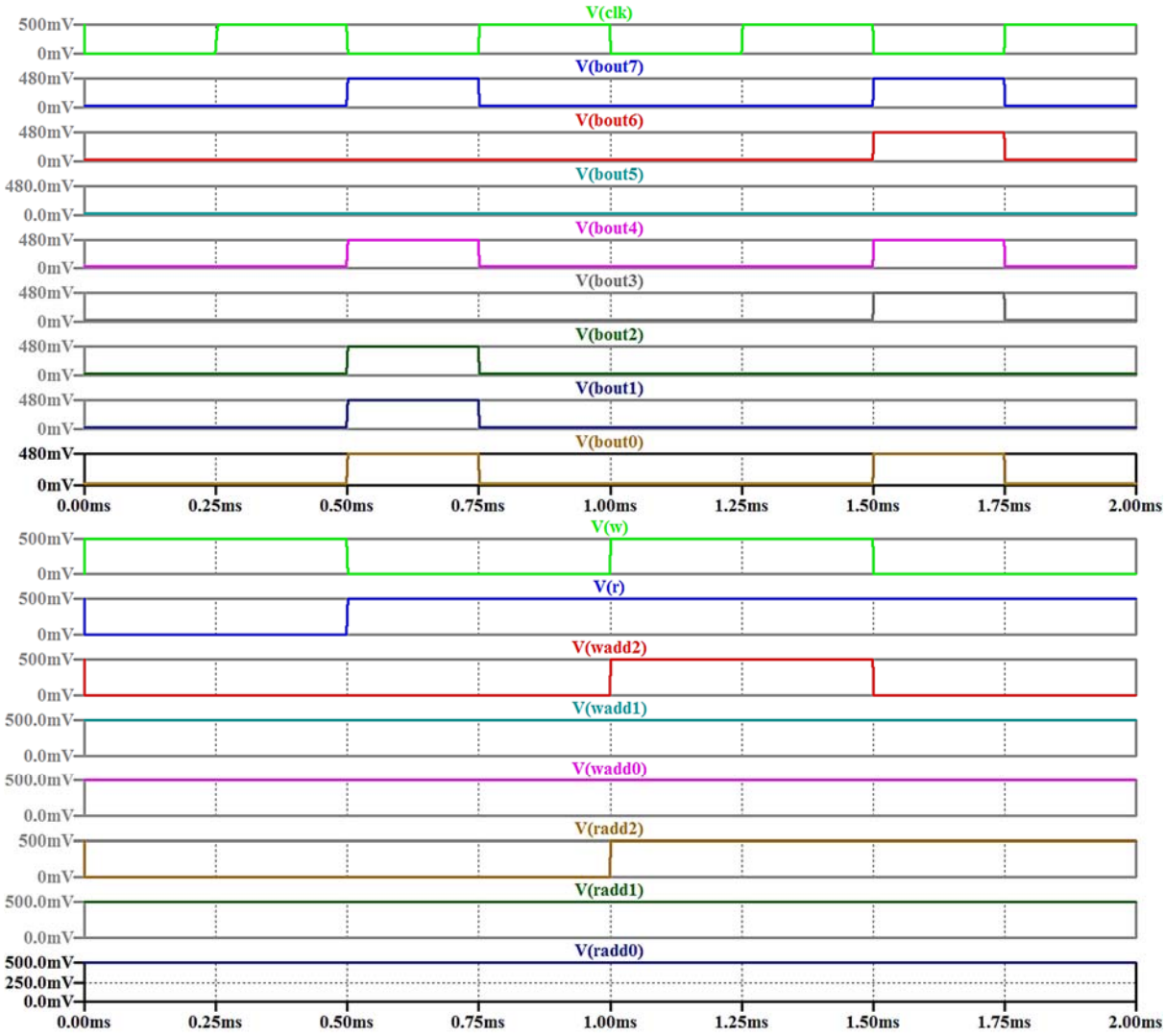


Fig. 6. SRAM Simulation.

Table 4. SRAM area and dissipated power.

	#SET NAND	Area	Power
nanoNAND	1	172 nm²	3.5 pW
Array	206	35432 nm²	721 pW
Decoder	37	6364 nm²	129.5 pW
SRAM	1890	0.325 µm²	6.6 nW

A preliminary noise margin analysis for the nanoelectronic SRAM includes temperature and background charges influences. The temperature noise analysis was achieved by varying the operation temperature between 270 K and 330 K and observing both the input (V_i) and output (V_o) voltage levels. The V_o x V_i characteristic plot for varying temperatures is shown on Fig. 7. Fig. 8 shows the upper part of the plot with zoom in.

It is visible that higher temperatures do influence somewhat the device behavior. However, this influence is not great given that for 30 K temperature variation, alters the output voltage at 0.5 %. This analysis does not include any background charge.

The background charges analysis was obtained by the inclusion of random background charges in the SET's islands during the simulation. The amount of charges was varied between 0 % and 20 % of the elementary electron charge. During this analysis the device temperature was kept constant at 300 K. The results are shown on Fig. 9.

The insertion of random background charges shifts the high/low level transition of the device to the right. As shown in the graph, up to 10 % of random charges is not only tolerable, but also beneficial for the device, since it brings the noise margin closer to ideal values. The graph also shows that the nanoNAND employed in this work is more robust against random background charges, which happens because its architecture is original, i.e., it is not a copy of the CMOS-based NAND gate architecture [14].

6. Conclusions

This work presented, validated and analyzed the proper working of a completely nanoelectronic

SRAM. This approach solves the area and power consumption limitations that current applications face. Also, the architecture provides the possibility of a separate read and write addressing, allowing for more versatile applications with lower latency time for the memory.

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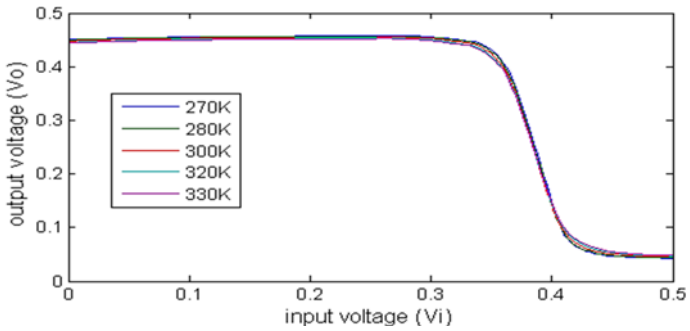


Fig. 7. Characteristic VoxVi transfer curve for varying temperature.

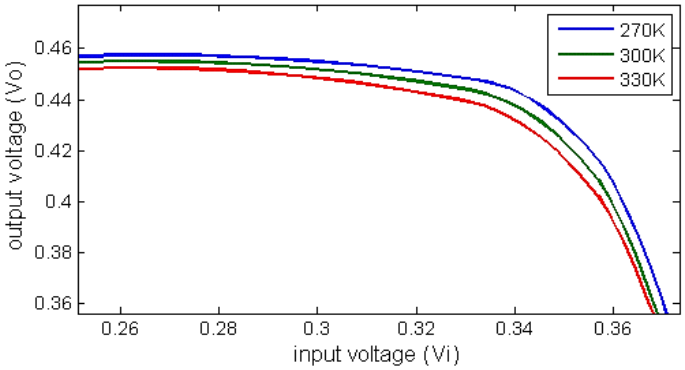


Fig. 8. Zoom of the characteristic curve.

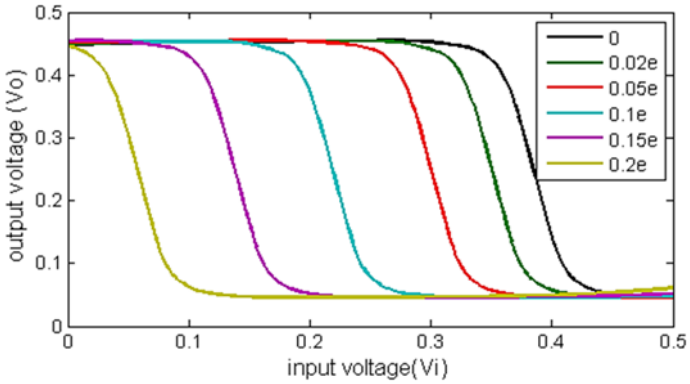


Fig. 9. Characteristic curve plot for varying random background charges percentage.

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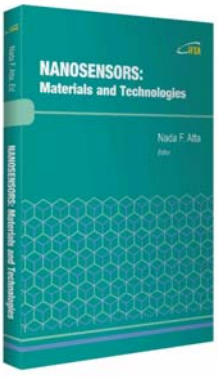
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NANOSENSORS:
Materials and Technologies

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Nanosensors: Materials and Technologies aims to provide the readers with some of the most recent development of new and advanced materials such as carbon nanotubes, graphene, sol-gel films, self-assembly layers in presence of surface active agents, nano-particles, and conducting polymers in the surface structuring for sensing applications. The emphasis of the presentations is devoted to the difference in properties and its relation to the mechanism of detection and specificity. Miniaturization on the other hand, is of unique importance for sensors applications. The chapters of this book present the usage of robust, small, sensitive and reliable sensors that take advantage of the growing interest in nano-structures. Different chemical species are taken as good example of the determination of different chemical substances industrially, medically and environmentally. A separate chapter in this book will be devoted to molecular recognition using surface templating.

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Atomistic Simulation of Structure and Dynamics in Crystallizing Germanium Thin Films

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Abstract: Low-temperature crystallization of germanium thin films has been simulated by means of molecular dynamics. Tersoff bond order potential was adopted for calculating the interactions between germanium atoms. Amorphous model was prepared by quenching the molten system at 1800 K. The model was consisted of about 1000, 5000 or 10000 atoms and free boundary condition was adopted. Then these amorphous systems were kept at temperatures, 400 K or 600 K, for 500,000 steps and crystallization was really observed. To investigate the atomistic process of crystallization the cross sectional view of the atomic configuration, the change of the mean potential energy, the radial distribution function and the trajectory of atomic displacement were evaluated. Boundary conditions between the sample and the substrate were investigated in detail.

Keywords: Germanium, Molecular dynamics, Crystallization, Amorphous, Radial distribution function, Tersoff potential.

1. Introduction

Metal induced crystallization has been extensively studied as a powerful method of crystallization. The present authors have been engaged in the study to fabricate the germanium thin films on the flexible substrates in the project to improve the yes/no device for the totally locked in state (TLS) patients, however it is not yet to be usable [1]. Problems are fitting and durability to use in daily life. In our experimental study germanium films are deposited at 60 □ and crystallized at 150 □ (423 K). However, the microscopic process of the mechanism of crystallization is not well understood in many cases. Molecular dynamics simulation using reliable interatomic potential is a powerful way to visualize microscopic processes of crystallization. A previous work has already been reported [2]. One of the present authors has been applied the molecular dynamics simulation on the studies of crystal defects and mechanical properties of metals [3]. The program code developed in the studies can be used in the present investigation.

2. Method of Simulation

The bond order potential function developed by Tersoff, *et al.*, is used in the simulation [4-5]. The potential energy depends on the bond length and bond angle. The potential energy is described as

$$E = \sum_i E_i, \qquad E_i = \frac{1}{2}\sum_{j \neq i} V_{i,j}, \tag{1}$$

$$V_{ij}(r) = f_{\mathrm{C}}(r)[\, f_{\mathrm{R}}(r) + b_{ij}\, f_{\mathrm{A}}(r)], \tag{2}$$

$$f_R = A\exp(-\lambda r)$$
$$f_A = -B\exp(-\mu r), \quad (3)$$

where b_{ij} is related to the coordination number and represent the many body nature of the potential. The truncation function $f_C(r)$ and other variables are described as

$$f_C(r) = \begin{cases} 1, & r < R \\ \frac{1}{2} + \frac{1}{2}\cos\left[\pi\frac{(r-R)}{S-R}\right], & R < r < S \\ 0, & r > S \end{cases}, \quad (4)$$

$$b_{ij} = \kappa_{ij}(1+\beta^n\zeta_{ij}^n)^{-1/2n},$$
$$\zeta_{ij} = \sum_{k\neq i,j} f_C(r_{ik})g(\theta_{ijk}), \quad (5)$$
$$g(\theta_{ijk}) = 1 + \frac{c^2}{d^2} - \frac{c^2}{d^2 + (h - \cos\theta_{ijk})^2}$$

The force acting on an atom is calculated by differentiating the expression for energy, Eq. (1), by distance *r*. The equation of motion for an atom is solved by integrating the potential numerically by the Verlet algorithm. The time interval for the numerical integration is chosen to be $\Delta t = 1.0\times10^{-15}$ sec, which is much smaller than the period of the atomic thermal vibration.

The molecular dynamics simulations are performed by using a Fortran code developed the present authors and results are visualized by Visual Basic 6 (Microsoft).

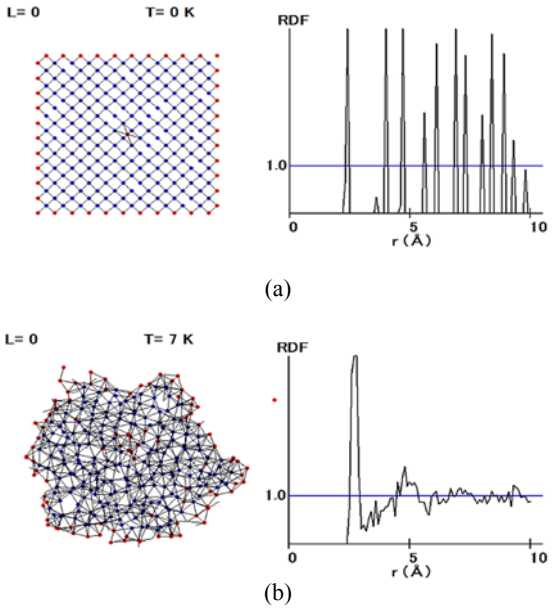


Fig. 1. Configuration of atoms (a) in perfect crystal and (b) in amorphous state. The radial distribution functions are shown in right hand side.

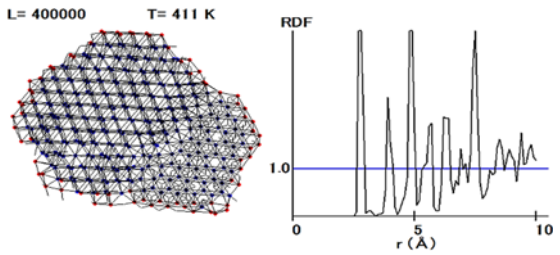


Fig. 2. Configuration of atoms and radial distribution function in crystallized state.

3. Results and Discussion

3.1. Particle-like Samples

For the simulation to investigate the fundamental mechanism of crystallization a small specimen consists of 1332 atoms is prepared. As an initial condition, atoms are arranged in diamond structure with {100} boundary surfaces as shown in Fig. 1 (a). The length of one side of cube is about 3 nm. The radial distribution function (RDF) of the structure is also shown in the right. The free boundary condition is adopted. Then the temperature is increased up to 1800 K. The molten state is quenched and amorphous state is realized.

The atomic structure and the RDF of amorphous state are shown in Fig. 1(b). A completely disordered structure of amorphous is seen.

The simulation of the low temperature crystallization starts from the amorphous state.

The temperature of the amorphous specimen was maintained at 411 K and 600 K. As an example of the structure of crystallized sample at 400 K is shown in Fig. 2.

It is seen that the sample is consisted of two grains and the RDF in right hand side shows a spike-like change characteristic of crystal is seen. The potential energy can be calculated by Eq. (1). The change of the potential energy is shown in Fig. 3. It monotonically decreases at the first 100 thousand steps, and the first crystallization is completed in this time domain. After that, the potential energy slightly increases and decreases again. Changes in grain structure occur in this region. The grain structures at typical time steps, (a) 100000, (b) 250000, (c) 400000, are also shown in the figure. The grain structure in the specimen is changing at the constant temperature. It is also seen that the outer shape of the sample also changes. It can be understood that the free surfaces of the specimen plays an important role in polycrystallization. In some cases, several tens of atoms were released from the sample to the outside, and crystallization occurred as a result of this. This may be related to collective motion of metal atoms promoting crystallization. Crystallization seems to have accidental features. Even in the simulation with the set temperature of 600 K, the same behavior was quantitatively observed.

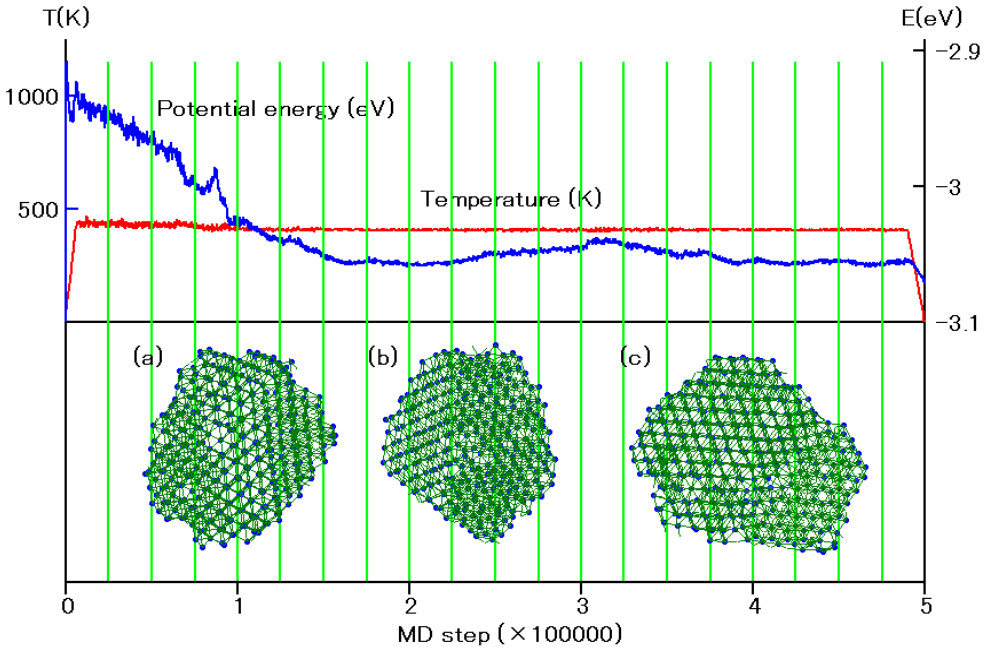
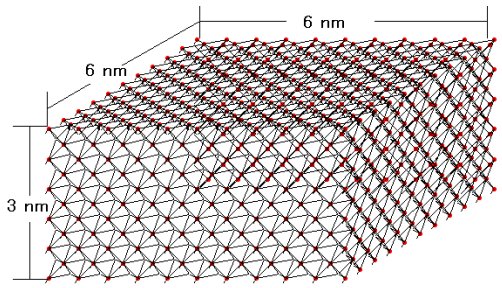


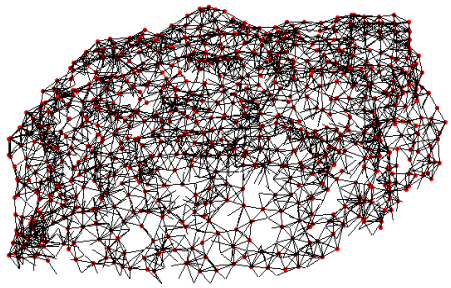
Fig. 3. Change of potential energy and typical grain structures at 400.

3.2. Plate-lile Sample A

A flat plate-like sample was prepared to simulate crystallization in the state close to a thin film. This is composed of 4852 atoms in the form of four particles arranged in the horizontal direction (Fig. 1 (a)) in the previous section. The temperature of this sample was raised to 1,800 K to bring it into a molten state, then quenched to realize an amorphous state (Fig. 4 (b)).



(a) Initial crystal



(b) Melted and quenched

Fig. 4. Preparation of plate-like sample A.

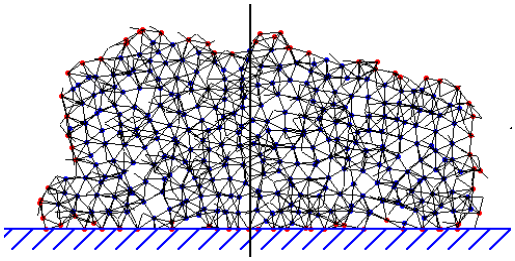
Simulation of polycrystallization was performed using this amorphous state as an initial state. Two types of boundary conditions are adopted between the substrate and the sample in the simulation:

1) The substrate and the sample are in close contact and atoms can slide on the surface,

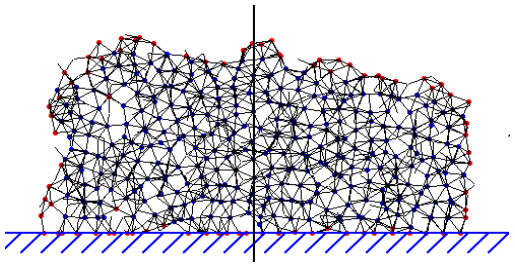
2) Loose contact with the base plate (allowing withdrawal within 10 Å).

In the boundary condition (1), crystallization has hardly progressed because atoms are mostly fixed at the lower end of the sample. On the contrary, in the boundary condition (2), it can be seen that polycrystallization is more advanced because of the boundary condition close to the free surface even at the lower end. In order for crystallization to occur, a degree of freedom in the three-dimensional direction may be necessary between the sample and the substrate. Namely, the boundary condition is very important for the crystallization of thin films. The details of local crystallization in larger sample are described and discussed in the next section.

Fig. 7 shows the temporal change (step) of the average potential energy of atoms in the sample, with the blue lines for the boundary condition (i) and the red lines for the boundary condition (ii). The upper graph shows the results for 400 K and the lower graph shows the results for 600 K, and both have similar behavior. In the boundary condition (i), the potential energy is almost constant. The relaxation of atomic structure does not seem to occur. On the contrary, it can be seen that in the boundary condition (ii), the potential energy repeats an increase and decrease at initial several 10000 time steps. After the initial violent rise and fall, it is relaxed to a lower level. It seems that after 60000 time steps energy is reduced by polycrystallization.



(a)



(b)

Fig. 5. Cross-sectional view of the plate-like sample. (a) initial smorphous state, (b) after annealing under boundary condition (1).

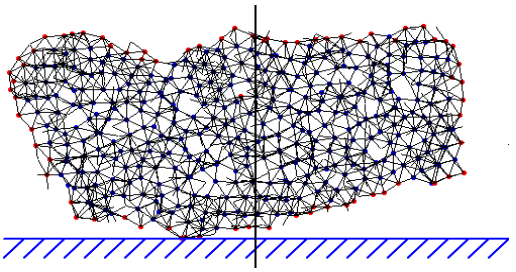


Fig. 6. Cross-sectional view of the plate-like sample after annealing under boundary condition (2).

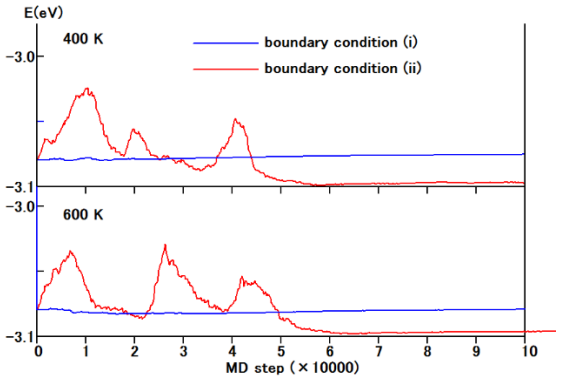


Fig. 7. Change of the mean potential energy.

The trajectories of the movement of atoms in the sample during the crystallization process under each boundary condition are shown in Fig. 8. Results for 400 K and 600 K are summarized. Small solid circles indicate the initial positions of each atom, and the curves following them indicate the trajectory of movement. In accordance with Fig. 7, the result of the boundary condition (i) is shown by blue lines and the result in the boundary condition (ii) is shown by red lines. In the boundary condition (i), it can be seen that small horizontal movements occur at both temperatures because only the motions parallel to the substrate are allowed. In the boundary condition (ii), large motions with rotation are seen at 400 K. At 600 K, large horizontal violent movements also occur.

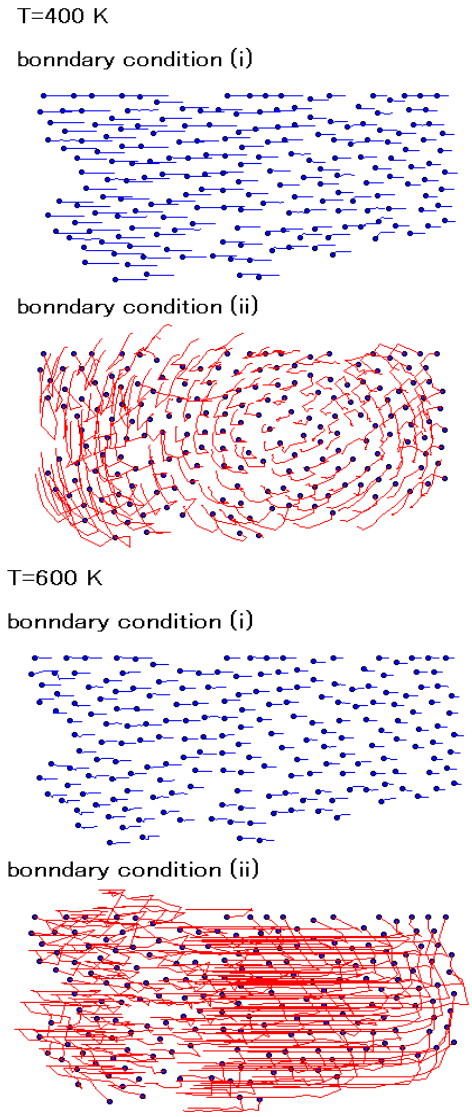


Fig. 8. Trajectory of atoms at 400 K and 600 K under the boundary conditions (i) and (ii).

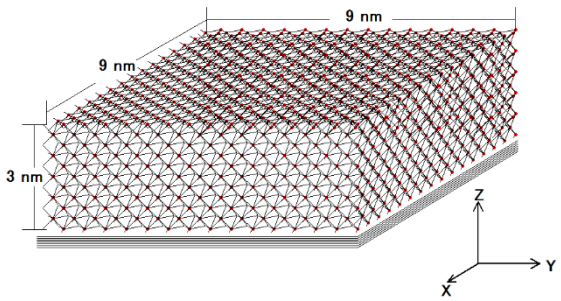
Investigating the microscopic behaviors of atoms as described above is useful in studying the dynamical nature of atomistic mechanism of crystallization.

3.3. Plate-lile Sample B

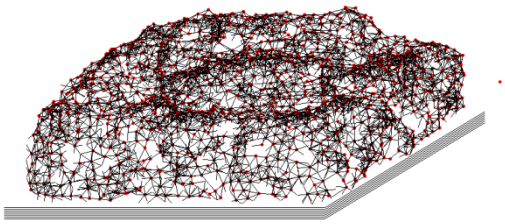
A Larger sample was prepared to study the local motion state of the atoms in the crystallizing processes. The initial crystal has the same thickness as

the sample A in the previous section and has an area about twice as large, composed of 10572 atoms.

The dimensional drawing is as shown in Fig. 9(a). As before, the temperature was raised to 1800 K to molten state and then rapidly cooled down (quenched) to prepare a sample in an amorphous state at the starting sample B (Fig. 9(b)). In order to quantitatively investigate the process of partial crystallization of plate-like samples, 25 spherical domains are set in the sample as shown in Fig. 10.



(a) Initial crystal



(b) Melted and quenched

Fig. 9. Preparation of plate-like sample B.

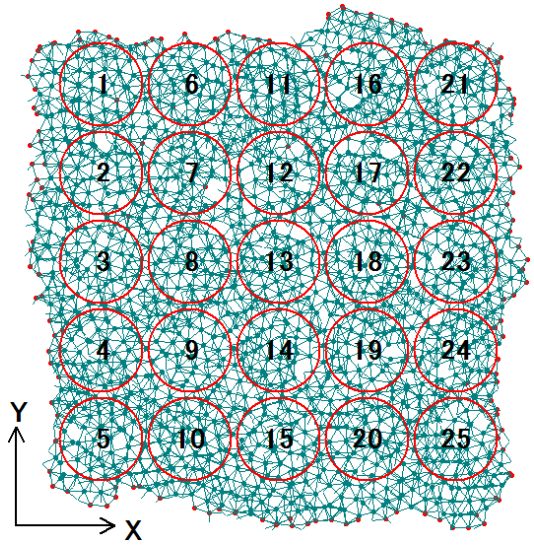


Fig. 10. Sample doains to track the atomic motion.

Each domain is spherical with a radius of 7 Å, which contains about 85 to 100 atoms. The arrangement and movement of the atoms contained in each region are tracked by molecular dynamics. Here, some of the results for 400 K annealing are described here.

As an example, Fig. 11 shows the changes of the atom array and the radial distribution function in domain 11. As the annealing progresses, the radial distribution function becomes sharp, and after 100000 steps, it shows nearly perfect crystal features. At the same time, it turns out that atomic arrangement is headed toward a regular array. In addition, in order to avoid complexity, atoms inside the region are not drawn, so there are parts where the space is seen bigger.

The trajectories of several selected atoms in the region are shown in Fig. 12. It is understood that the atoms are moving in random directions around the original positions.

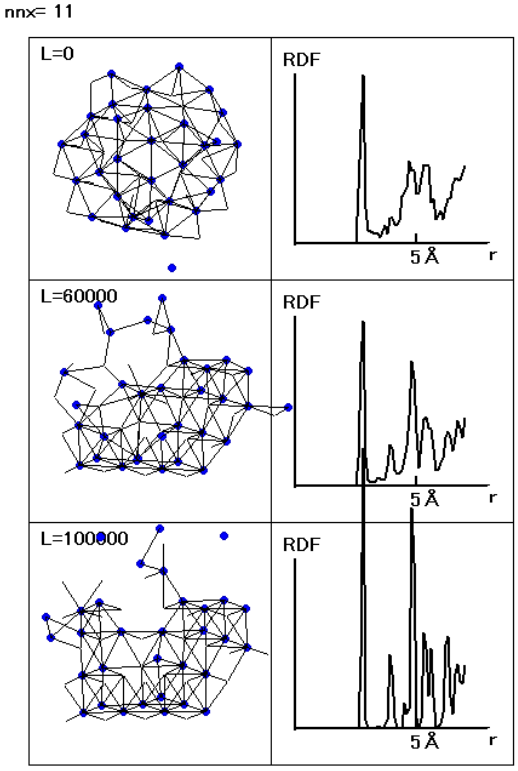


Fig. 11. AtomicConfiguration and RDF in domain 11.

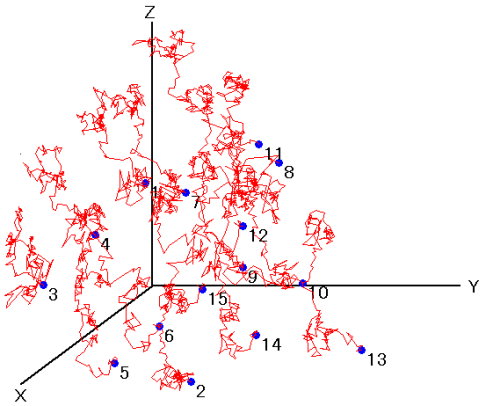


Fig. 12. Trajectory of atoms in domain 11.

Fig. 13 shows the temporal change of the displacement in the X direction. The numbers at the right end of each curve in the figure agree with the numbers attached to the atoms in the trajectory in Fig. 12. It is seen that the displacements of all atoms changes coherently with time through the annealing.

A similar analysis is performed for atoms in domain 19. Fig. 14 shows the changes of the atom array and the radial distribution function in domain 19. The radial distribution function does not change through 100000 steps and atomic arrangement does not show appreciable change. Namely, the crystallization does not happen in this domain.

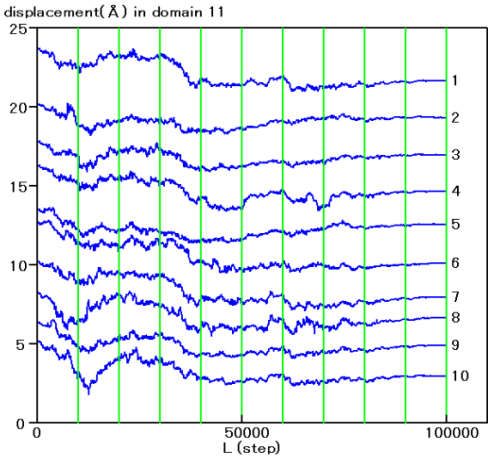


Fig. 13. Temporal change of displacement in X direction for atoms in domain 11.

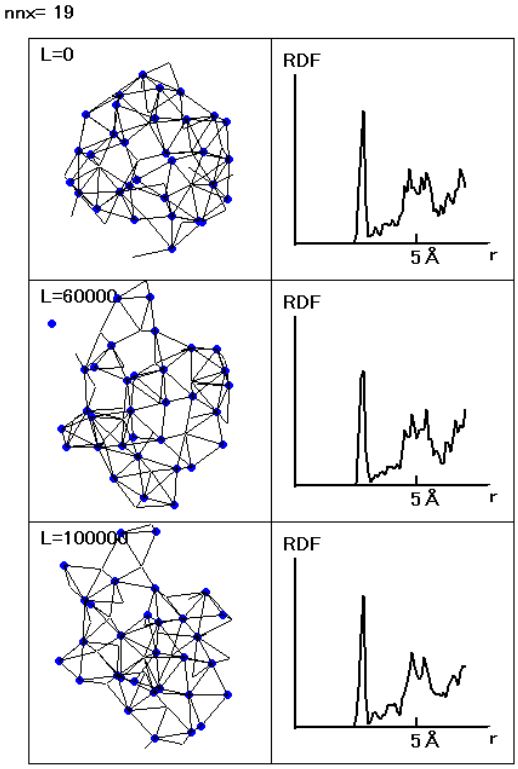


Fig. 14. AtomicConfiguration and RDF in domain 19.

The trajectory of atoms in domain 19 is shown in Fig. 15. Large displacements of atoms are seen of compared with Fig. 12. The temporal change of the displacement shown in Fig. 16 show rather irregular nature compared with the results for domain 11.

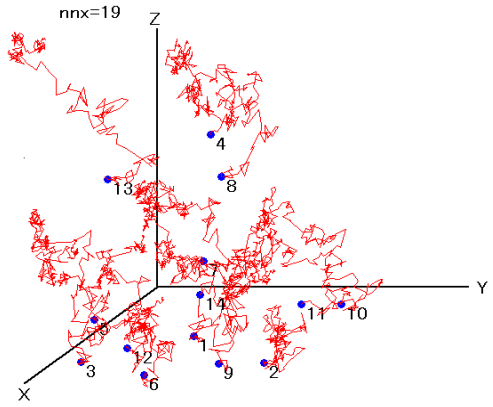


Fig. 15. Trajectory of atoms in domain 19.

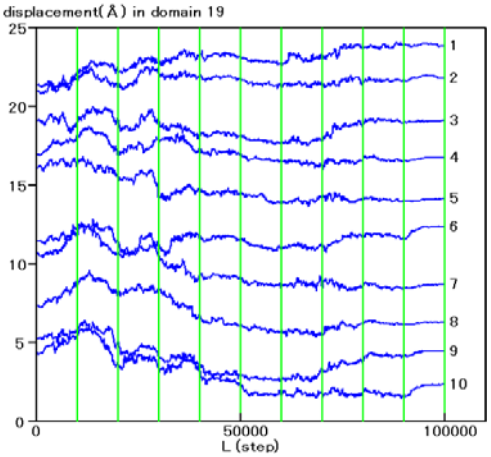


Fig. 16. Temporal change of displacement in X direction for atoms in domain 19.

Changes in the potential energy per atom in the domain 11 and 19 are compared in Fig. 17.

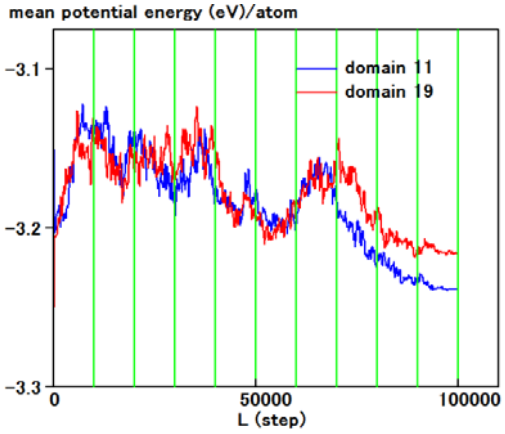


Fig. 17. Change of mean potential energy of Domain 11 and 19.

In both domains, the potential energy fluctuates drastically in the first half of annealing. After that, once it returns to the initial level, it rises again and then descends. The final energy is not so different from the initial value in the domain 19, but it is found to be low in the domain 11 where crystallization proceeds.

Similar inspections were performed in all 25 domains defined in Fig. 10, and it was found that crystallization proceeded in domain-1, -5, -6, -7, -11, -14, -15, -16, -21, and -24. Namely, crystallization was recognized in 40 % of domains. Here we set up a spherical domain with a radius of 7 angstrom as the first attempt, but it seems that the domains with a slightly flexible shape and size may be useful.

4. Conclusions

Low-temperature crystallization of amorphous Ge has been simulated by using the empirical Tersoff potential. The crystallization is observed at the temperatures 400 K and 600 K. The process of crystallization was monitored thorough the cross sectional view of the atomic structure and the RDF. Change in the potential energy associated with the crystallization was observed. Boundary conditions between the sample and the substrate were investigated in detail for the plate-like sample A, and a role of free space between the sample and the substrate was revealed. The non-uniform or heterogeneous nature of the crystallization was investigated in the larger plate-like sample B. The sample was divided to local domains and the structure and motion of atoms in the domains were compared. These results seem to be useful for the development of medical devices using germanium thin films.

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Surface-Potential Based Sub-Circuit Model of AlGaN/GaN HEMT Including Non-Quasi-Static Effects

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Abstract: In this paper, the non-quasi-static surface-potential-based large signal model of AlGaN/GaN HEMT yielding continuous static and dynamic characteristics in the whole operation range is described. The model includes some important physical phenomena affecting device DC and transient operation like two-dimensional electron gas quantization, polarization charge, electron velocity saturation, high-field mobility degradation, channel length modulation and the related effect of finite time for the channel charge to build-up. The non-quasi-static HEMT model is implemented in PSPICE in the form of the equivalent sub-circuit. An excellent fit between the new HEMT model and the device numerical simulation data obtained from a TCAD software is achieved for the DC, AC and switching characteristics of normally-on GaN HEMTs with various channel lengths ranging from 1 μm to 10 μm. It is also demonstrated that, unlike the NQS model, the quasi-static (QS) modeling approach results in significant errors in predicting the fast switching transient currents of longer channel GaN HEMTs.

Keywords: Surface-potential, Sub-Circuit, AlGaN/GaN, HEMT Model.

1. Introduction

With significant progress in the improvements of quality and performance of GaN HEMTs, the exploitation of full potential of these devices requires the advanced electrical models for circuit simulations. Most GaN HEMT compact models [1-2] are based on the quasi-static (QS) assumption that ignores the finite time for the 2DEG channel charge to build-up. The QS assumption results in negligible errors in ultra-short channel devices and/or when they operate at slow rate of change of the terminal voltages that gives enough time for the channel charges to redistribute. However, at very high signal frequencies and/or in case of longer channel GaN HEMTs, the QS models result in significant errors in time-domain device simulations. A few Non-Quasi-Static (NQS) GaN HEMT models taking into account the channel charge redistribution at fast voltage transients have been proposed so far [3-5]. However, they are either empirical models fitting their equations to measured data with mathematical optimization [3] or developed only for a small-signal analysis [4-5].

In this paper, we describe the unified large/small signal NQS model of AlGaN/GaN HEMT with Schottkey gate and its implementation in SPICE. It is based on the surface-potential (SP) modelling approach also used previously for deriving the NQS models of HEMTs and MOSFETs [6-7]. The GaN HEMTs with variable channel lengths L=(1 μm÷10 μm) are analyzed in order to emphasize the importance of the NQS channel effects. Note that GaN HEMTs with longer channels (L>1μm) are often encountered in high power devices [8] or for some specific experimental and testing purposes [9-10]. The accuracy of the NQS GaN HEMT modelling is validated in this study by comparisons with t.

2. The NQS HEMT Model

Fig. 1 shows the Surface-Potential based Sub-Circuit (SPSC) model of GaN HEMT that is implemented in PSPICE circuit simulator. Unlike the similar QS SP model [12] where the gate capacitor node is simply lumped with both the external source and drain nodes, the 2DEG channel of GaN HEMT is represented in the NQS SPSC model with the N-segmental equivalent non-linear RC line as shown in Fig. 1.

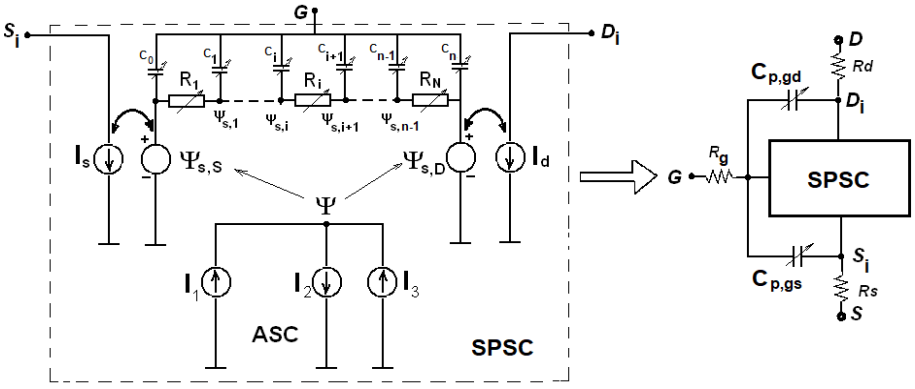


Fig. 1. The equivalent NQS SPSC model of GaN HEMT with added parasitic elements.

The core model also includes the auxiliary sub-circuit (ASC) computing the boundary surface potentials $\psi_{s,S}$ and $\psi_{s,D}$ at the source and drain ends of the channel, respectively, while the main sub-circuit (SPSC) calculates the drain and the source currents I_d and I_s, respectively, in SPICE simulations. The SPSC actually emulates the static and the dynamic operation of the intrinsic part of GaN HEMT structure. It can be embedded in the network of added extrinsic elements referring to the source/drain access regions, the gate Schottkey diode, the parasitic capacitances, inductances and resistances. In present study, only the parasitic gate-source and the gate-drain capacitances $C_{p,gs}$,$C_{p,gd}$, the gate resistance R_g and the source/drain access region ohmic resistances R_s, R_d are included in the NQS model as shown in Fig. 1. The channel segmental resistance R_i is analytically expressed as [13]:

$$R_i = \frac{w_i \cdot \left(1 - \boldsymbol{\lambda} \cdot V_{DS}^{\mathbf{m}}\right)}{W \cdot q \cdot \mu_n \cdot n_{s,i}} \tag{1}$$

where λ and m are the fitting parameters of the channel length modulation effect, $n_{s,i}$ is the channel charge density, μ_n is the electron mobility, $w_i = L/N$ is the segmental resistor length, L is the total gate length, W is the channel width and q is the electron charge. The longitudinal and vertical electric filed dependences of μ_n are modelled in (1) using the approximate physical expressions [13]. Note that the channel longitudinal electric field E_x affecting μ_n can be obtained from seeing Fig.1 as:

$$E_x = \frac{\psi_i - \psi_{i-1}}{w_i} \tag{2}$$

Finally, the channel charge density $n_{s,i}$ of the i^{th} segment was found to be quite accurately expressed with linear function [13]:

$$n_{s,i} \cong a \cdot \left(V_{gp} - \psi_i\right) + b, \tag{3}$$

where $V_{gp} = V_{gs} - V_{off}$ is the effective gate voltage, V_{off} is the channel cut-off voltage, ψ_i is the local channel potential, and a and b are the model fitting parameters.

The distributed line variable capacitors C_i are defined in the NQS model as:

$$C_i = \left(q \cdot \frac{W}{w_i} \cdot \frac{\partial n_{s,i}}{\partial V_{gs}} + \frac{C_{dep}}{N}\right), \tag{4}$$

where the first derivative term denotes the channel charge differential capacitance, while C_{dep} is the fixed gate capacitance of fully depleted AlGaN buffer layer. It can be shown from (3) and using the results presented in [12], that the derivative of $n_{s,i}$ in (4) can be quite accurately approximated by an analytical parametric function:

$$\frac{\partial n_{s,i}}{\partial V_{gs}} = a \cdot \left[1 - \frac{1}{1 + \exp\left(m \cdot V_{gp} - p \cdot V_{ds} + l\right)}\right], \tag{5}$$

where m, p and l are the new fitting parameters for modelling the variable channel capacitances C_i. Note that the parasitic capacitors $C_{p,gs}$ and $C_{p,gd}$ of the source/drain access regions can also be modelled with (4) and (5) by appropriate parameter adjustments and by taking $V_{ds}=0$ and $V_{ds}=V_{dg}$ for $C_{p,gs}$ and $C_{p,gd}$, respectively. Note that the voltage dependence of R_s and R_d as well as the drain-to-source parasitic capacitance, omitted in this study, have minor effect on the long-channel HEMT characteristics.

3. TCAD Simulations and Model Calibration

The validity of the NQS GaN HEMT model is accessed by comparisons of SPICE results with 2-D device simulations using TCAD software ATLAS from SILVACO [11]. Fig. 2 shows the schematic cross-section of an un-doped Schottkey gate $Al_{0.25}GaN_{0.75}$ HEMT structure that is simulated in this work.

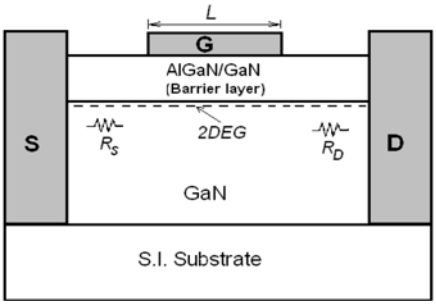


Fig. 2. A schematic cross-section of AlGaN/GaN HEMT.

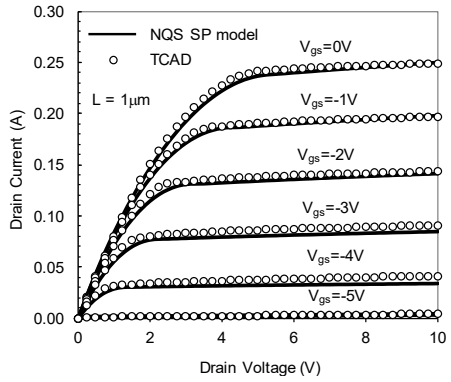
In simulations, we have adopted 400 μm, 4 μm, 32 nm and 5 eV for the device width, the length of source/drain access regions, the thickness of AlGaN barrier layer and the gate metal workfunction, respectively. The cut-off voltage of this device was found to be V_{off} = -5.5 V. Also, the Albrecht, *et al.* [14] low field electron mobility model in 2-DEG channel, the standard lateral field mobility model with velocity saturation and the ATLAS built-in polarization model for GaN devices [11] were also included in ATLAS simulations. Note that the thermal effects (device self-heating) are not included in present study.

Fig. 3 shows the comparisons between simulated and modelled the DC output characteristics of the device shown in Fig. 2 with various channel lengths L (1 μm, 6 μm and 10 μm). An excellent agreement between simulated and modelled curves is achieved by fine tuning the NQS HEMT model fitting parameters listed in [13] while keeping N=10 in all cases.

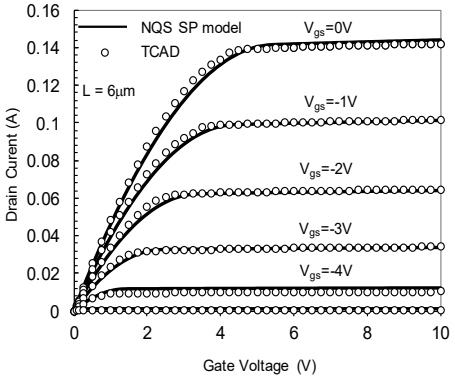
Following the DC model calibration, the parameters of voltage dependent capacitances C_i, $C_{p,gs}$ and $C_{p,gd}$ were extracted from fine tuning the modelled and simulated y-parameters obtained from ATLAS small-signal device simulations at low frequency (300 Hz) and for various V_{gs} and V_{ds}. Fig. 4 shows the good agreement between simulated and modeled the total gate input capacitance C_{GG} and the gate-drain parasitic capacitance C_{GD} versus V_{ds} and V_{gs} obtained for HEMT with L=1 μm.

4. Large Signal Modeling Results

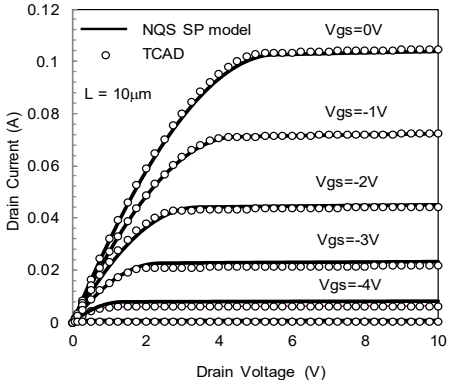
A successful calibration of the capacitance models enables the achievement of a good agreement between the simulation and modeling of the pulse transient currents in GaN HEMTs with various channel lengths (1 μm÷10 μm). The excellent agreement is obtained as shown in Fig. 5. In these simulations, the gate pulse 0 V to -5 V, the 5 V power supply and the 10 Ohms external resistor were assumed for single HEMT resistive invertor as shown in the inset of Fig. 5 (b).



(a)



(b)

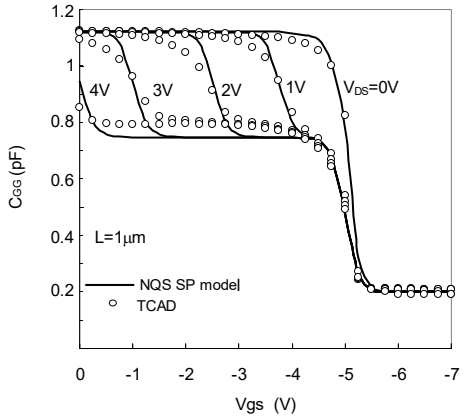


(c)

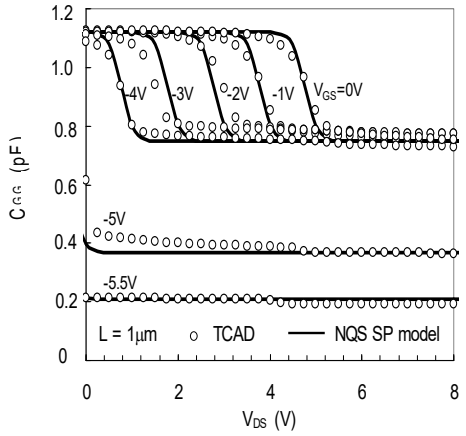
Fig. 3. Simulated and modeled the output characteristics of GaN HEMT with (a) L =1 μm, (b) L =6 μm and (c) L=10 μm.

Fig. 6 shows the NQS and QS modeling results in comparison with the TCAD mixed-mode simulations of the same invertor in case of HEMT with L=6 μm.

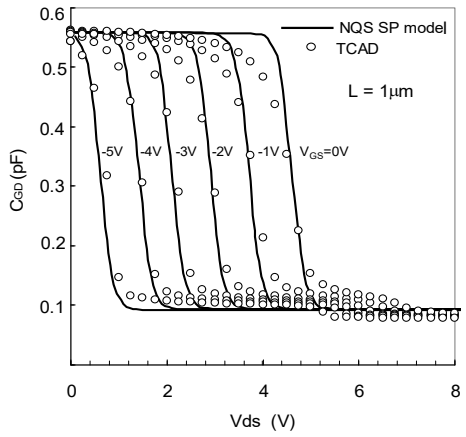
While the drain current transients are very well predicted by both models as observed in Fig. 6 (a), the QS model fails to correctly predict the source and the gate transient currents either by missing or overestimating the current spikes, respectively, as clearly shown in Fig. 6 (b) and Fig. 6 (c). The same drawback of the QS modelling approach is also found for all other simulated GaN HEMTs with L>1 μm.



(a)

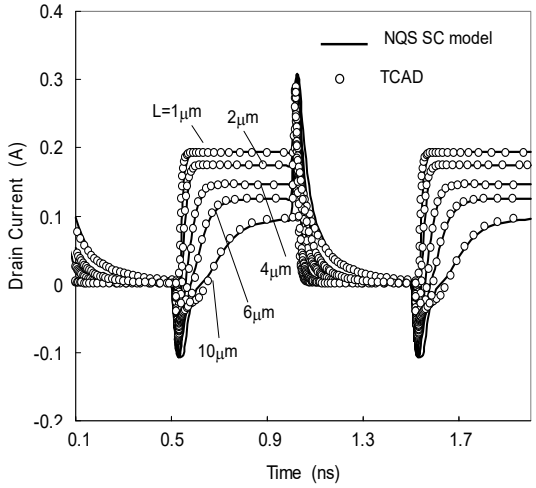


(b)

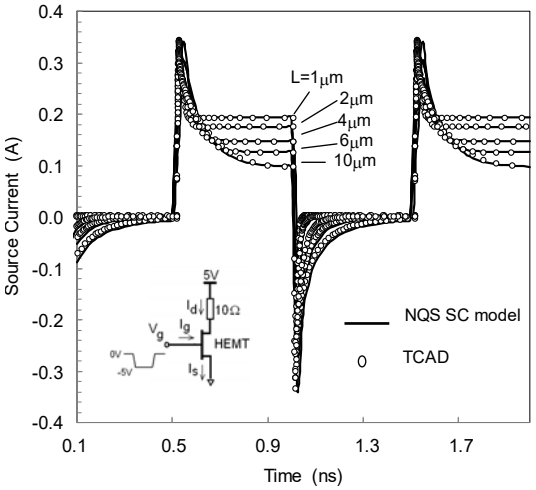


(c)

Fig. 4. Simulated and modeled the total gate input capacitance C_{GG} (a), (b); and the gate-drain capacitance C_{GD} (c) versus V_{DS} and V_{GS}.



(a)



(b)

Fig. 5. Simulated and modeled: (a) the drain and (b) the source pulse transient currents of GaN HEMTs with L=(1 μm÷10 μm). The currents were extracted from ATLAS mixed-mode and SPICE simulations of simple resistive HEMT invertor shown in the inset of (b).

5. Small-signal Modeling Results

The efficiency of the NQS model in small-signal analysis of GaN HMETs is demonstrated in Fig. 7.

It shows the comparison between the NQS modeled and TCAD simulated frequency dependences of imaginary and real parts of the input and the transfer admittances $\mathbf{y}_{11}$ and $\mathbf{y}_{12}$, respectively, of GaN HEMTs with L=1 μm, 6 μm and 10 μm at V_{gs}=0 V and V_{ds}=2 V. Because of their gate areal dependences, the absolute values of R_g and C_{dep} had to be adjusted in each case of L_g for obtaining the best fit. With increasing L_g, however, the value of gate ohmic resistance R_g decreases while the input gate capacitance C_{dep} increases, thus limiting the absolute rise of the imaginary part of $\mathbf{y}_{11}$ and $\mathbf{y}_{12}$ with frequency as shown in Fig. 7 (b) and Fig. 7 (c).

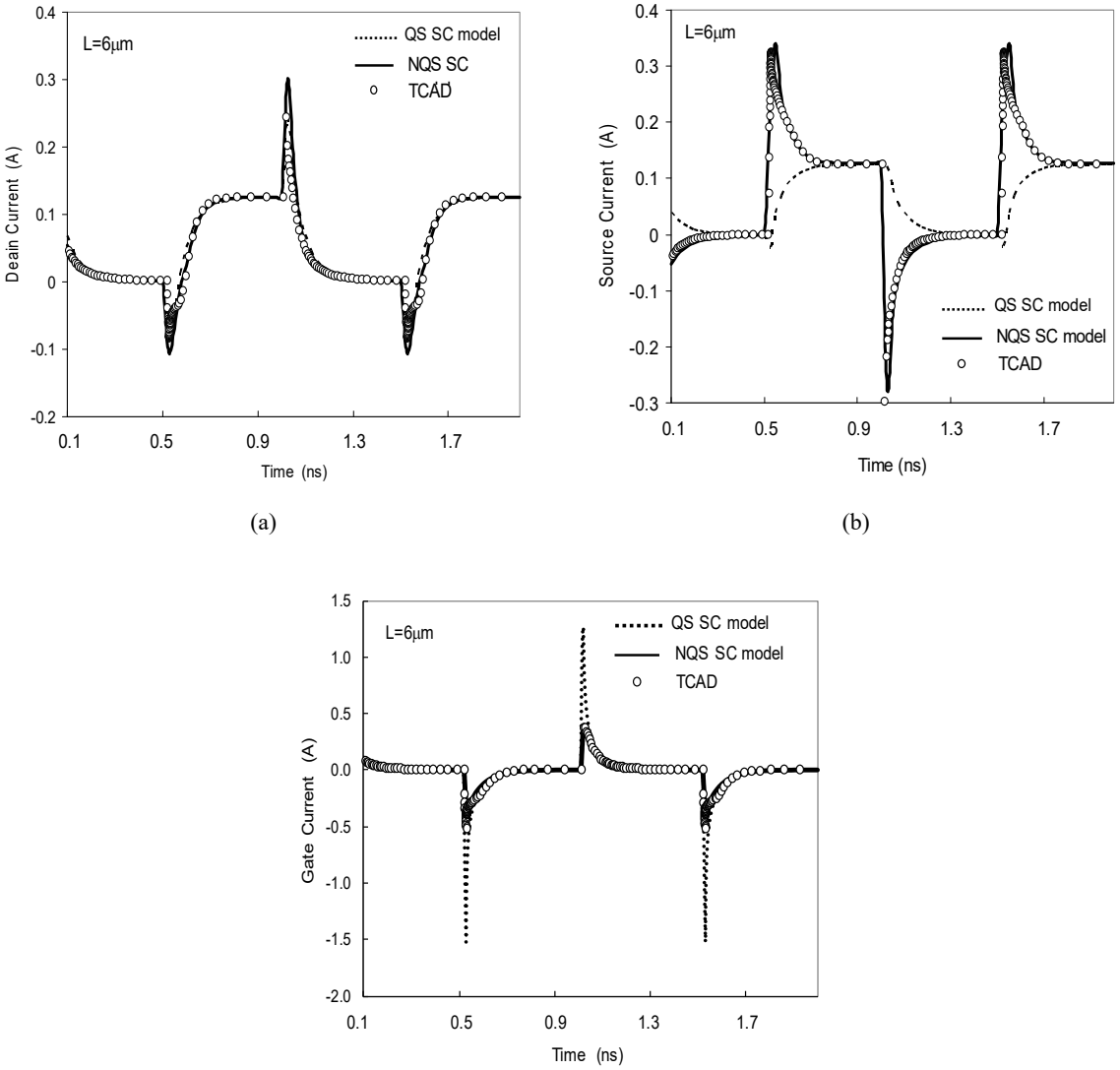


Fig. 6. Comparisons between the TCAD mixed-mode simulations and the NQS and the QS modeling of pulse transient currents (a) I_d, (b) I_s and (c) I_g of GaN HEMTwith L= 6 μm.

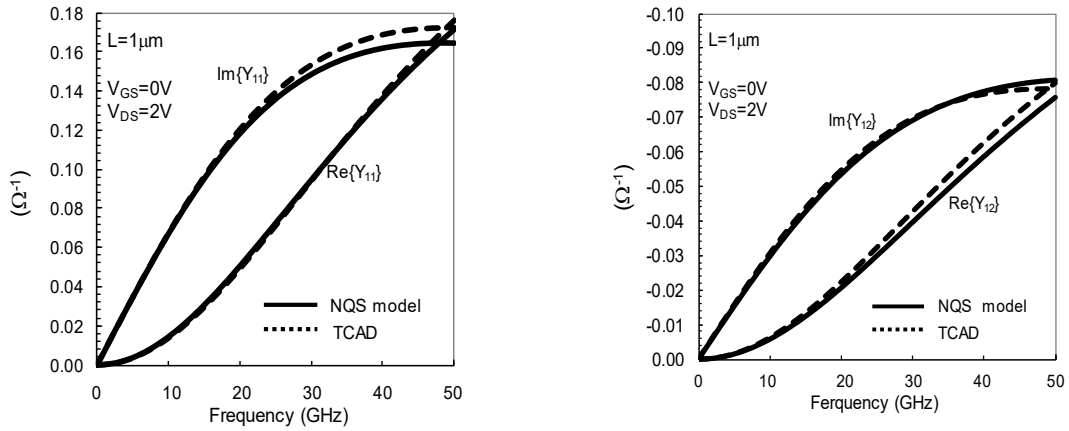


Fig. 7 (a). Simulated and modeled the imaginary and the real parts of $\mathbf{y}_{11}$ and $\mathbf{y}_{12}$ small-signal admittances versus the frequency obtained for GaN HEMT with L=1 μm at V_{gs}=0 V and V_{ds}=2 V.

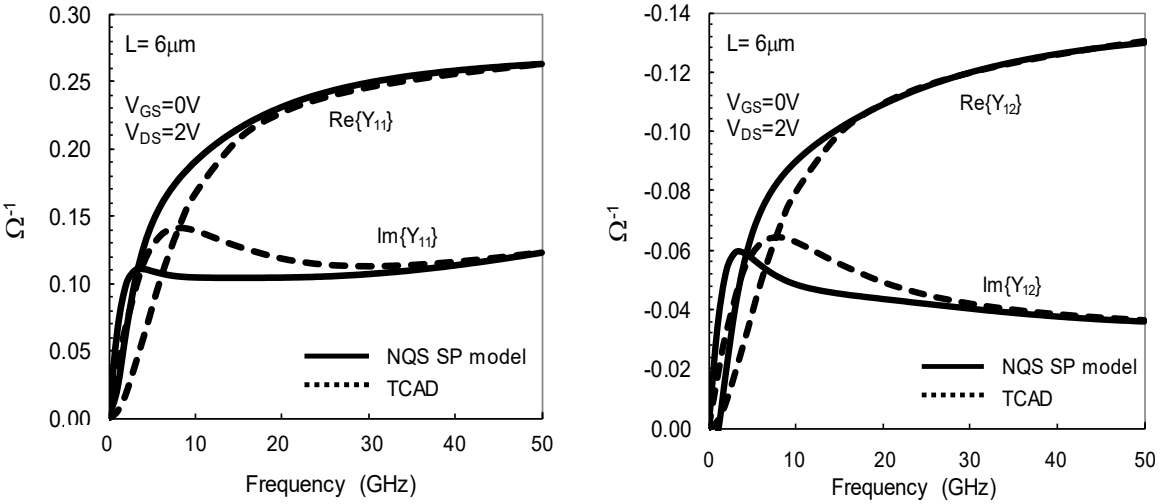


Fig. 7(b). Same as in Fig. 6(a) but for HEMT with L=6 μm.

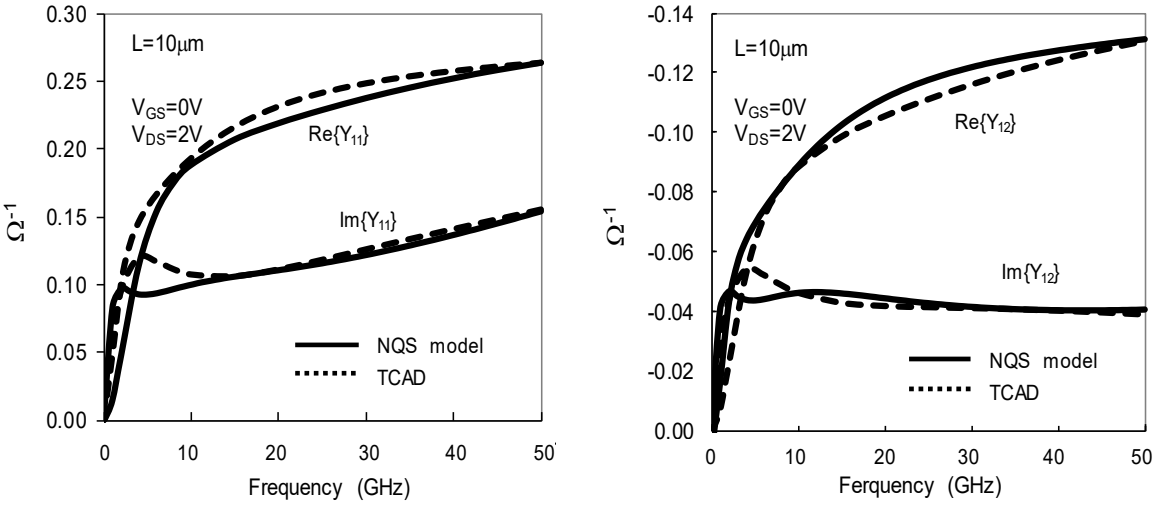


Fig. 7(c). Same as in Fig. 6(a) but for HEMT with L=10 μm.

6. Conclusions

A unified large/small signal non-quasi-static model of AlGaN/GaN HEMT with Schottkey gate is described and implemented in SPICE in the form of sub-circuit. High accuracy of the NQS model is demonstrated for both large and small signal analysis of long channel GaN HEMTs based on the comparison with two-dimensional mixed-mode numerical device simulations.

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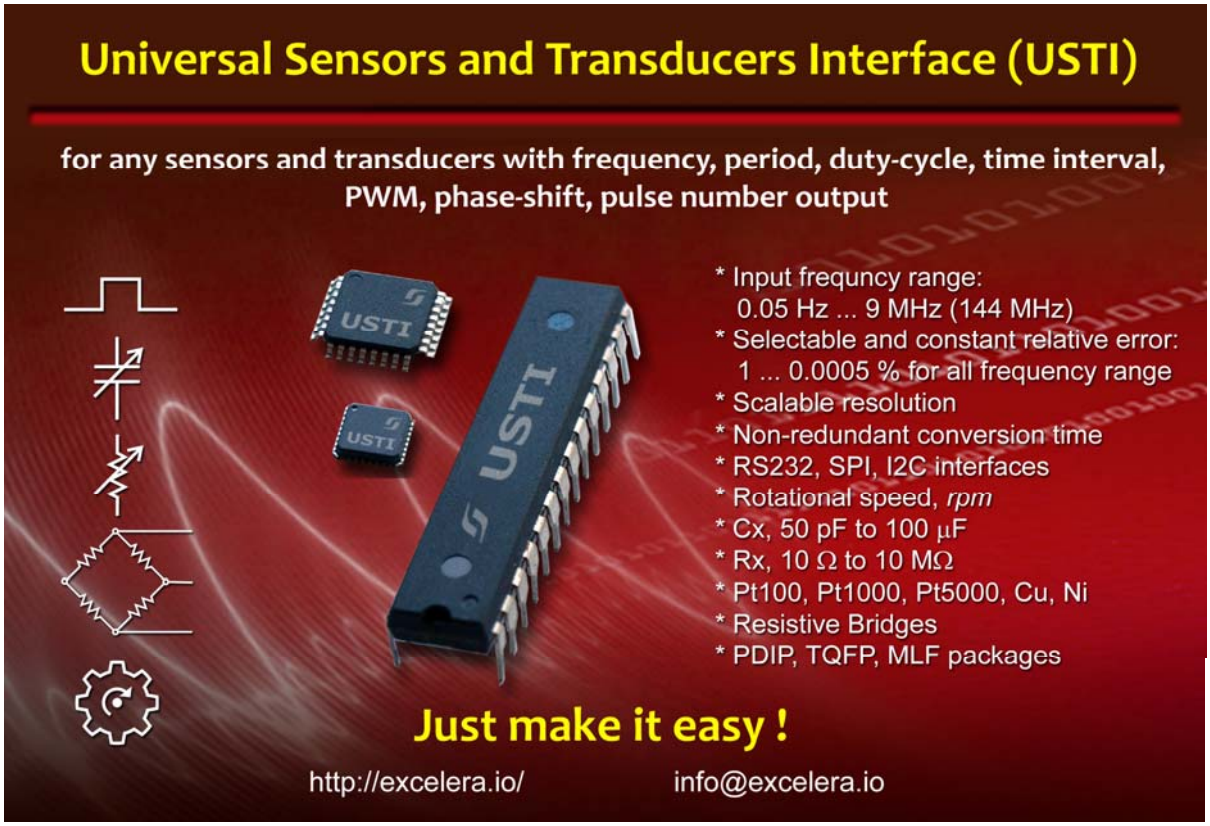
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Tailored Plastic Chip Electrode for Fabrication of Amperometric Glucose Sensor Using GOx@ZIF-8(AuNPs) as Support

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Abstract: An innovative protocol has been established for the encapsulation of glucose oxidase (GOx) and gold nanoparticles (AuNPs) together into the cavity of ZIF-8 metal organic framework and subsequently utilized for glucose sensing application in aqueous media using plastic chip electrode as an effective platform. ZIF-8 possess high stability both physically and chemically. Its large surface area and tunable cavity size is supportive to accommodate both the GOx and AuNPs. The as-synthesized microstructure is meticulously characterized by various physico-chemical techniques which approves that AuNPs are uniformly distributed within ZIF-8 cavity. The existence of AuNPs not only increases conductivity but also enhance the activity of GOx and enable both glucose oxidation and oxygen reduction reaction in tandem fashion. Plastic chip electrode acts as a superior bulk electrode for fabrication of such glucose sensor in aqueous media. Further, the as synthesized material shows commendable stability with very low-level detection of glucose in aqueous media (60 nM of glucose).

Keywords: Plastic chip electrode, ZIF-8, Gold nanoparticle, Amperometry, Enzymatic glucose sensor.

1. Introduction

Diabetes mellitus is currently considered as one of the most widespread chronic ailments which mainly occurs due to unhealthy lifestyle like obesity and lack of physical activity. The major threat is that it affects blood glucose levels directly which may consequences to serious health issues like kidney failure, cardiac arrest, degeneration of neurons [1]. This solemn threat to health has significantly increased in recent time due to rapid urbanization and hence people acquires such modern lifestyle. Patients having this chronic disease are advised by doctor to monitor their blood glucose level at a regular interval and prescribed insulin shot periodically for long-term management of their blood glucose level [2]. However, available methods of monitoring are associated with pain and troublesome due to possibilities of causing injections. Hence, there is an urgent need for non-invasive glucose monitoring [3-5]. It is almost 55 years passed, since Clark and Lyon first proposed the concept of glucose sensing in 1962 and still there is no sign of diminishing speed of latest technology in this sector. More generally, the advancement of amperometric glucose sensor devices

till 1962 can be separated into three generations. First-generation devices were based on the simple principle which is consumption of the atmospheric O_2 co-substrate and the production of H_2O_2 which was to be detected as a function of glucose concentration. Second generation devices had been prepared by substituting atmospheric O_2 with another electron mediator. Latest third generation devices have mainly focused with non-invasive mediator free detection of glucose from saliva/sweat. This whole voyage of advancement has been extensively reviewed by various authors [6-8]. The most vital and fundamental concept to develop mediator free glucose biosensor is to facilitate direct electron transfer between the electrode and the active centre of redox protein [9]. Although, the task is rather difficult to accomplish as the redox active protein (Flavin adenine dinucleotide [FAD]/$FADH_2$) and the prosthetic group of glucose oxidase (GOX) are deeply buried inside the rigid and non-conducting layer of GOX. Electron mediator species is thus utilized externally to facilitate this catalytic reaction artificially [9-10].

Scientific community shows promising interest over metal organic framework (MOF) due to its large surface area, unique design, and most importantly uniform and tuneable pore sizes [11]. Zinc-imidazole framework 8 (ZIF-8), classified under zeolitic MOF, was reported to be an excellent chemical moiety having specific pore size to accommodate small to large biomolecule and protect them from major external stimuli [12-20]. Metal nanoparticles (MNPs), in the other hand, possess excellent chemical and physical properties and a useful tool to fabricate mediator free biosensor. Generally MNPs have been used frequently to design such biosensor for twin purpose as it significantly increases the surface conductance of the electrode to mediate charge easily to the electrode surface and in the same time, enhances the surface area so that the electron tunnelling distance is sufficiently low for mediating of charge [21-26]. Recent reports of Dong, *et al*. shows preparation of ZIF-8 nanostructure composite, encapsulated with GOx and PVP stabilized NiPd as an effective catalyst for glucose sensing [27]. Among numerous nanoparticles, Au nanoparticles (AuNPs), stabilized by citrate, shows promising interest to scientific community due to its exceptional properties. One of this is high conductivity of AuNPs which helps to mediate charge from the electrolyte to electrode surface. Another important reason to choose AuNPs is due to highly dispersed in water causing zero interference with biological species [28-31]. Plastic chip electrode, a cheap and viable bulk conducting electrode, had been fabricated by our group few years ago and till now it is extensively used for various of applications in the field of chemistry and biology. It is an important opportunity to avoid costly electrode to fabricate biosensors as the viability of PCE is proved to be exactly same compared to other market available electrodes.

In this work, we report the applicability of plastic chip electrode to fabricate a mediator free glucose sensor. synthesis of GOx@ZIF-8(AuNPs) by encapsulation of gold nanoparticles and glucose oxidase together into the cavity of ZIF-8 and utilize for the catalytic oxidation of glucose. Citrate stabilized Au nanoparticle was synthesized and reported in our previous work [32]. Here it has been encapsulated successfully onto ZIF-8 matrix along with glucose oxidase. The catalyst was utilized in amperometric glucose sensor having a detection limit as low as 60 nM of glucose, accrediting glucose monitoring from sweat. In sort, the present catalytic protocol is more efficient and robust for the low-level detection of glucose (60 nM) in aqueous media based on our knowledge.

2. Experimental

2.1. Materials and methods

All the chemicals were of analytical grade and used without further purification. $HAuCl_4.3H_2O$, trisodium citrate dehydrate, Glucose oxidase from aspergillus niger (GO_x), 2-Methylimidazole were purchased from sigma Aldrich and used as received. $Zn(NO_3)_2.6H_2O$ was purchased for SRL chemicals and used as received. GO_x@ZIF-8(AuNPs) nanocomposite was synthesized at room temperature in aqueous media. To prepare GO_x@ZIF-8(AuNPs) nanocomposite, AuNPs and GO_x (aspergillus niger) were added in the reaction mixture of the ZIF8- metal organic framework.

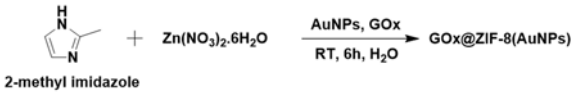
Plastic chip electrode was prepared in reported method and had been used for all electrochemical experiments. The electrode was rinsed with ultrapure water and dried at room temperature. All the experiments were done in three electrode electrochemical setups comprising PCE as working, Pt wire (0.1 mm diameter) as a counter and Ag/AgCl (sat. KCl) as a reference electrode. All the electrochemical measurement was by Metrohm Autolab 302 potentiostat/galvanostat. The GOx@ZIF-8(AuNPs) slurry was prepared by dispersing 10 mg of material in 1mL of pH 7.4 buffer and sonicated for 15 minutes. 10 μL of as prepared solution was drop-casted over PCE surface. 5 μL 0.5 % nafion is added to the mixture as a binder.

The crystal structure of the product was characterized by XRD (PAN Analytical Empyrean Series 2 X-ray diffraction system). The morphology and microstructure of the synthesized materials were investigated by FESEM (JEOL JSM-7100F,) and HRTEM (JEOL JEM-2100). FT-IR was done at Parkin-Elmer G-FTIR. Detail synthetic procedure of GO_x@ZIF-8(AuNPs) nanocomposite is as follows. For all electrochemical measurement Metrohm Autolab 302 potentiostat/galvanostat is used.

2.2. Synthesis of GO_x@ZIF-8(AuNPs)

ZIF-8 was synthesized by previous reported method. 23 gm of 2-methlyimidazole (109 mili moles)

was taken in 420 mL of ultrapure mili-Q water. 50 mg of GOx (8170 units in 50mg) was added in the same solution. This mixture turned pale yellow in colour due to dissolved GO_x and labelled (A). 1.20 gm of $Zn(NO_3)_2.6H_2O$ (1.54 mili moles) was dissolved in another 380 mL of ultrapure milli-Q water separately and labelled (B) Gold nanoparticles (AuNPs) were prepared by our previously reported protocol [32]. Trisodium citrate dehydrate was used as stabilizing as well as reducing agent in aqueous media. As synthesized AuNPs were stored at 4˚C temperature for further use. 10 mL of citrate stabilized AuNPs was taken separately (C). The mixture of B & C was added to the mixture A under constant stirring of 700 rpm at room temperature and the reaction mixture was continuously stirred for 3 hours. In the very beginning of the reaction, solution was transparent and yellow in colour which started to turn hazy after few minutes of stirring. After completion of 3 hours the mixture was allowed to stand for overnight and then supernatant was decanted. It has been observed that the yellow colour of the mixture disappeared after the successive addition but no deep red colour of AuNPs appeared. This give initial confirmation on encapsulation of both GO_x and AuNPs together inside ZIF-8 moiety. The settled solid part was centrifuged and washed with 50 mL of water for 3 times to remove any excess GO_x and AuNPs (not encapsulated). Further it was dried under vacuum and purple colour solid composite was recovered, preferably assumed the formation of GO_x@ZIF-8(AuNPs) nanocomposite. The synthesized probe was characterized by FT-IR, Powder XRD, FE-SEM, STEM to confirm the artefact. The scheme is depicted below in Scheme 1.



Scheme 1. Preparation of Gox@ZIF-8(AuNPs).

2.3. Tailoring of Plastic Chip Electrode

Plastic chip electrode was fabricated in reported method [33]. A simple composite of 60:40 of graphite and poly methyl methacrylate (PMMA) was taken in chloroform. For this case, we had prepared a composite of 6 g of graphite powder and 4 g of PMMA in 25 mL of chloroform. The composite was stirred constantly with a glass rod and ultrasonicated for 15 minutes. A thick slurry of graphite-PMMA composite was poured into a specific template (10 cm × 10 cm glass plate) containing a lamination sheet and dried overnight. The bulk electrode was peeled out from the template and cut into pieces having a size of 3 cm × 0.8 cm (length × width). A circular area of 5 mm diameter was cut in a lamination sheet by plotter cutter and respective electrode was placed to that circular area and lamination was done using a laminator to get fixed surface area having 5 mm diameter. The fabricated electrode was washed with milli-Q water for immobilization of catalyst. 10 µL of as synthesized material, dispersed in pH 7.4 buffer, was drop-casted and dried in room temperature. 5 µL of 0.5 % nafion is added for firm binding of the material to electrode surface. Further, the tailored electrode was utilized for amperometric measurement.

3. Results and Discussions

3.1. Characterization of Materials

The citrate stabilized AuNPs and GO_x inside ZIF-8 material shows very distinctive structural features. Its phase was determined by X-Ray powder diffraction (P-XRD) after vacuum drying. P-XRD pattern of as synthesized GO_x@ZIF-8(AuNPs), is shown in the Fig. 1 (red colour) and is compared with the simulated powder XRD data of the ZIF-8 (blue colour), furnished in same figure. It is clearly observed that the P-XRD peaks of the synthesized GO_x@ZIF-8(AuNPs) matches well with the simulated ZIF-8, indicating no change in the native structural property of the ZIF-8 due to encapsulation of AuNPs and GO_x. As synthesized GO_x@ZIF-8(AuNPs) has been confirmed by its cubic shape (JCPDS: 00-062-1030, $a = b = c =$ 17.0116 Å, $\alpha = \beta = \gamma =$ 90°).

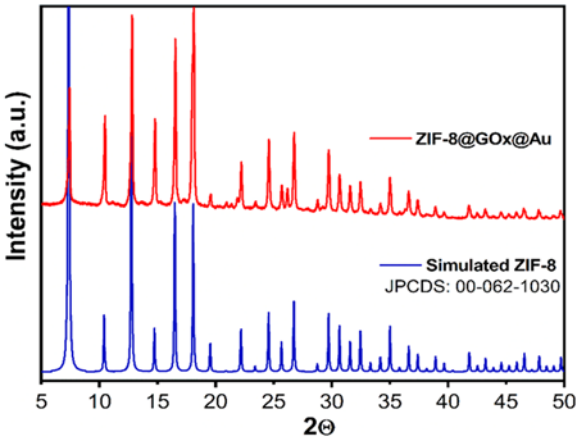


Fig. 1. XRD patterns for simulated ZIF-8 (JCPDS: 00-062-1030) and as synthesized GOx@ZIF-8(AuNPs).

The morphology of GO_x@ZIF-8(AuNPs) was examined by field-emission scanning electron microscopy (FESEM). Fig. 2(a) represents assembled star shaped morphology of ZIF-8 microstructure at low magnification. Whereas high magnified FE-SEM image shows assembly of rod like star morphology (Fig. 2(b)). GO_x has definitely played a crucial role in controlling the morphologies as GO_x has an affinity towards imidazole containing building block (ZIF-8) arises from intermolecular H-bonding and hydrophobic interaction [27]. Further, TEM was performed for detailed investigation of the synthesized microstructure and is depicted in Fig. 2(c). The image

shows the presence of highly crystalline distinctive lattice fringes, probably due to plane of Au nanoparticles over the surface of ZIF-8 moiety which also perfectly correlates with the XRD result. For further investigation, R-TEM was performed and upon increasing the resolution, (111) plane of Au was observed which also correlated with P-XRD data.

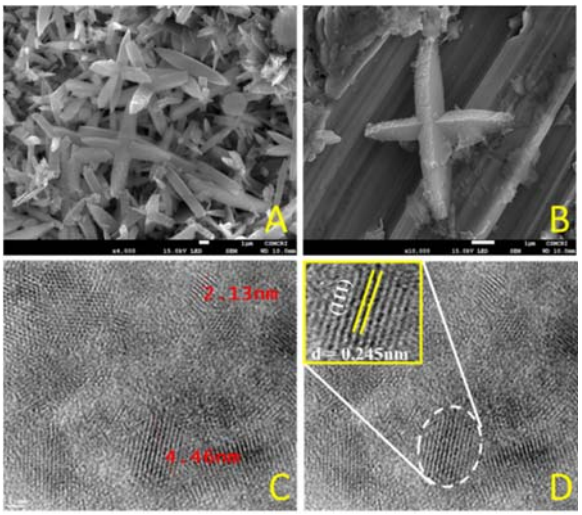


Fig. 2. FESEM image of 5 nm gold coated GO_x@ZIF-8(AuNPs) (a) crystalline growth (b) single particle showing large surface area (c) High resolution HRTEM image of Au lattice fringes (d) STEM-EDX line profile of GOx@ZIF-8(AuNPs) showing almost equal distribution of AuNPs.

To, prove the presence of GO_x in its native structure inside the ZIF8 cavity, Fourier Transform Infrared Spectroscopy (FT-IR) had been performed. GO_x has characteristic IR peaks at 1647 and 1426 cm^{-1} due to stretching vibration of –C=O group present in peptidic bond of amide-I and in-plane bending vibration of N_5H in FAD group respectively [34]. It is clearly seen from Fig. 3 that 1654 cm^{-1} peak of amide-I is slightly shifted to 1647 cm^{-1} as it is highly sensitive towards the structural modification [35].

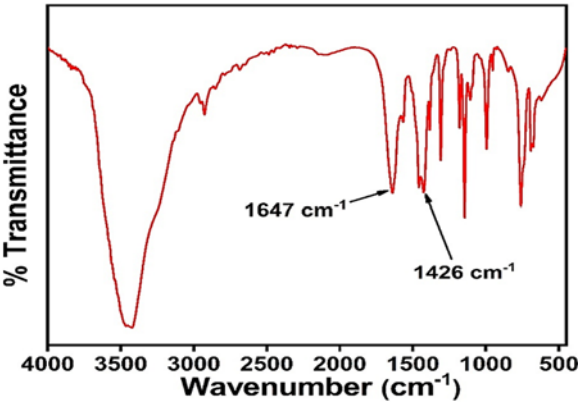


Fig. 3. FTIR Spectra of GO_x@ZIF-8(AuNPs)possessing two distinguishable peaks at 1647 cm^{-1} for -C=O stretching of Amide I and 1426 cm^{-1} for plane bending of FAD group.

Presence of both peaks at 1647 and 1426 cm^{-1} signify the presence of GO_x. These results clearly suggest that the GO_x does not degrade and possess its native structure inside the cavity of ZIF-8, showing biocatalytic activity.

3.2. Electrochemistry of GOx@ZIF-8(AuNPs)

Cyclic voltammetry (CV) measurement was carried out at a scan rate of 50 mV/S to evaluate the electrochemical property of GO_x@ZIF-8(AuNPs). For this purpose, three composites: ZIF-8, GOx@ZIF-8 and GO_x@ZIF-8(AuNPs) were scanned potentiodynamically. Prior to use, PCE was sonicated in milli-Q water for 15 minutes and then then dried at room temperature. 5 mg of each composite was dispersed in 1 mL of 0.1 M pH 7.4 PBS buffer by ultrasonication for 10 minutes and 10 µM from the aliquot was drop casted onto the PCE having a diameter of 5 mm. The electrode was kept covered to avoid external dust and was stored overnight at room temperature for drying. The modified electrode, projected as working electrode, was then immersed in N_2 saturated 0.1 M pH 7.4 PBS buffer for CV measurement. Pt wire (0.1 mm diameter) was taken as a counter electrode, whereas Ag/AgCl (sat. KCl) was taken as a reference electrode. CV was measured in the range of -0.2 to -0.7 V vs Ag/AgCl (sat. KCl) at a scan rate of 50 mV/S. Relatively higher scan rates are always preferred to assess the reversibility of electrochemical reaction. The result is depicted in Fig. 4. Both the ZIF-8 and GOx@ZIF-8 exhibits typical non-faradaic capacitive nature due to double layer capacitance and hence indicative of absence of any redox species (Fig. 4, red and blue dashed lines).

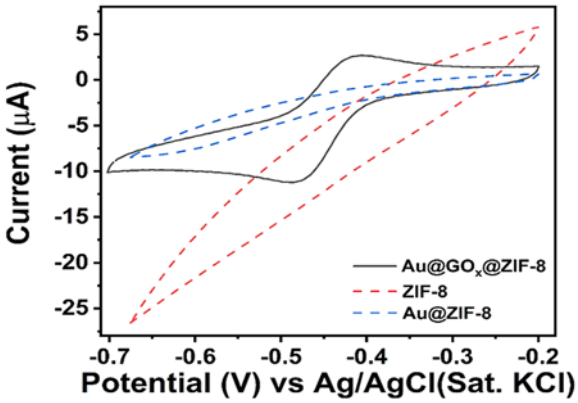


Fig. 4. Cyclic Voltammetry of ZIF-8@GO_x (blue dashed line), ZIF-8 (red dashed line) and GO_x@ZIF-8(AuNPs)(Black line) at a scan rate of 0.05 V/S in N_2 saturated 0.1M pH 7.4 PBS.

CV response of GO_x@ZIF-8(AuNPs) composite shows immense faradaic behaviour with visible sharp peaks in both cathodic and anodic potential at

E_{pa}= - 414 mV and E_{pc}= - 474 mV, having a peak separation of ΔE_p= 60 mV, which is consistent with reported value of E_{pa}= - 419 mV and E_{pc}= - 473 mV, [9] represents significantly high electron transfer rate of the reversible redox equilibrium of the FAD/$FADH_2$ redox couple. The encapsulation of Au nanoparticle is thus playing an importance role, not only by shortening the electron tunnelling distance but also increasing the sensitivity of the system upto 10-folds. The surface plasmon resonance energy of Au nanoparticle is so high that it can establish effective interaction with biomolecules resulting an immense increment in the output [36].

3.3. Calibration Plot

The amperometric measurement was performed in potentiostatic method. The experiment had performed by successive addition of 10 mM glucose to the air saturated pH 7.4 buffer solution at a characteristic potential of – 0.47 V vs Ag/AgCl (sat. KCl) (Fig. 5). Stair shaped change in current had been observed with quick steady state upon successive addition of glucose had been observed upon zooming, had been depicted inset of Fig. 5. The change of current creates a drift and the drift became stable after certain time due to formation of H_2O_2. Calibration plot is considered to be one of the most important characteristics of an electrochemical sensor and to do so the steady state current had been plotted with the concentration. A two-slope plot has been obtained due to formation and saturation of H_2O_2 formed. The result is depicted in Fig. 6.

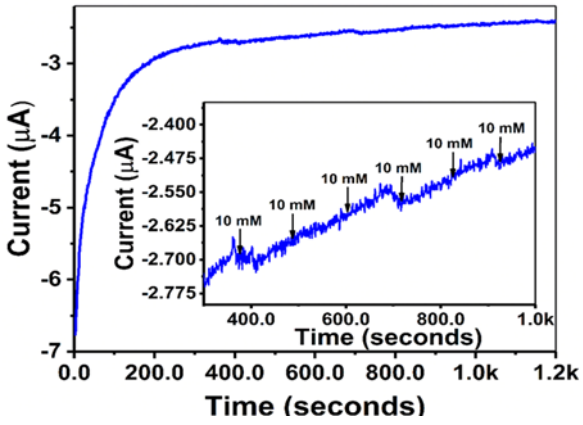


Fig. 5. Typical steady state amperometric measurement of catalytic glucose oxidation at -0.45 V vs Ag/AgCl (sat. KCl) with successive addition of 0.1 mM glucose. Calibration plot of concentration versus (full and linear region) current has been depicted inset.

Two different slopes with two different regression coefficients had been observed. Both the coefficients show excellent linearity of the fabricated sensor. A low-level detection of 60 nM of glucose had been observed for this biosensor which is quite good for such point of view to detect glucose from sweat/saliva. Moreover, we have used plastic chip electrode which is also extremely chip platform for detection rather than conventional costly electrodes. We observed that the current achieved steady state gradually after 15 successive dilution. The reason behind achieving such steady state is due to the increment of dissolved oxygen which disturbs the equilibrium of FAD/$FADH_2$. Although This low detection limit can be attributed to our claim of measuring blood glucose from sweat which encourages non-invasive, point of the care device.

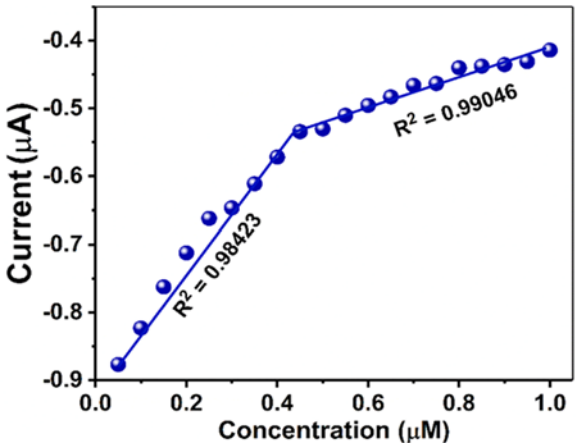


Fig. 6. Calibration plot of estimation of glucose concentration showing two distinct slopes having excellent regression coefficients.

4. Conclusions

In this paper, we have encapsulated AuNPs and GOx inside and ZIF -8 cavity and the synthesized composite is drop-casted over homemade plastic chip electrode for detection of glucose. The as synthesized composite was synthesized in gram scale and can be up scale to any desired limit. The composite material was thoroughly characterized by various physico chemical techniques. The characterization reveals that the synthesized material is highly crystalline in nature AuNPs is well dispersed, inside very stable framework. The presence of highly conducting AuNPs and GO_x on GOx@ZIF-8(AuNPs) nanocomposite, facilitate the consecutive oxidation of glucose. Plastic chip electrode had been used for first time for any biosensor application which will be a landmark for the preparation of economical biosensor preparation. Presence of Au nanoparticle increases the sensitivity of the system upto 10-fold with low level of glucose detection *i.e.* 60 nM in aqueous media. The result can be accredited towards fabrication of non-invasive glucose sensor mainly from sweat/saliva. Overall, the present methodology demonstrates an efficient, robust, economical and tolerable nanocomposite for glucose sensing in aqueous media by electrochemical pathway and can be an excellent alternative of market available glucose sensor.

Acknowledgements

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Effective Radiation Damage Models for TCAD Simulation of Silicon Bipolar and MOS Transistor and Sensor Structures

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Abstract: The special library of radiation damage models for physical parameters and electrical characteristics of bipolar and MOS transistor and sensor structures taking into account neutron, gamma and proton irradiation is developed and built-into Sentaurus Synopsys software tool. For different BJTs/HBTs, MOSFETs and radiation sensors the good agreement to simulated and experimental electrical characteristics is achieved. The RMS error is not more than 10-20 %.

Keywords: Bipolar and MOS transistors, Radiation sensors, Neutron, Gamma, Proton irradiation, Radiation induced device parameter degradation, Device modeling, TCAD software.

1. Introduction

The electronic devices employed in spacecraft, high-energy physics, RF and telecommunication, radiation measurement in technique and technology, diagnostics in medicine, military and other applications are subjected to different types of irradiation (neutrons, electrons, gamma rays, protons, heavy particles and others). However, the significant number of defects generated in semiconductor device structures after irradiation attracts the degradation of device parameters and increases the complexity of the design phase before the devices even have been fabricated.

To facilitate this problem the special strategy "radiation hardened by design" is used. It is realized at two levels: device scheme and modeling.

At the scheme level the hierarchy of bipolar and MOS components, circuits, systems on chip is introduced and built-into the device scheme. All these elements carry out the functions of sensing, measuring, control and monitoring of radiation influences and electrical regimes to provide the reliable operation range of electronic device under irradiation conditions.

At the modeling level the TCAD (Technology Computer-Aided Design) programs are used to predict the radiation induced degradation of characteristics of electronic components with different geometry and/or operation conditions. The increasing knowledge of radiation induced defects received in recent years allows implementing the physical models with realistic defect parameter sets into the TCAD software tools. So the TCAD device simulation becomes the integral part of every IC and/or sensor system chip development project taking into account radiation influence.

2. State-of-the-art

The BJT/HBT [1-3], MOSFET [4-7] and special bipolar and MOS radiation sensor [8-11] structures

were simulated with respect to radiation influence. The analysis of published works shows that in most projects for BJTs/HBTs and MOSFETs the universal commercial TCAD software tools Sentaurus Synopsys [12] and ATLAS Silvaco [13], also the special rad-oriented system Cagenda [14] were used. For bipolar and MOS radiation sensors and dosimeters the software tools Geant [15], FLUKA [16], FOTELP [17], and PENELOPE [18] were used to simulate the interactions of particles and/or radiation with a given materials. In all mentioned simulators, only gamma and single events models demonstrate the satisfied results agreed with measurements. Moreover the investigations demonstrate that in many cases the presently available gamma radiation models lead to significantly different results especially for novel device structures. In several works the authors have used the special fitting procedure of defect parameter set to correct the simulated results [19]. It is usually performed manually due to the complexity and the corresponding time consumption of the simulation [11]. So further work is need to increase the accuracy and efficiency of the device simulation taking into account gamma radiation effects.

Unfortunately, the radiation damage models for neutrons and protons used in the different version of TCAD device simulators are incomplete. For silicon devices subjected to neutron or proton irradiation not only ionization but displacement damage effects must be taken into account.

In this work, we try to solve the problems mentioned above[1]. The set of effective radiation damage models for gamma, neutron and proton irradiation is developed and included into TCAD Sentaurus tool as a complete library. It is very handy for the device designers to have a full set of radiation models concentrated in one software tool instead of the set of models distributed to the different version of TCAD tools.

3. TCAD-RAD Subsystem

In our previous work [20], the universal TCAD-RAD subsystem was developed. It consists of two parts: standard Sentaurus Synopsys software core [12] and the special library of radiation models for physical parameters and electrical characteristics of BJT/HBT and MOSFET structures taking into account neutron, gamma-rays and proton irradiation (see Fig. 1). Note that the models for neutrons and protons were not included in TCAD formerly.

The LIBRARY consists of 4 segments:

Common controller carries two functions:

1) Selection for given type of irradiation the set of radiation-dependent physical parameters and their models which are responsible for device electrical characteristics degradation;

2) Conversion the energy or dose rate of particles into total dose D and/or fluence Φ;

Gamma radiation models are based on carrier ionization effects. The adequate models of radiation-dependent parameters (N_{ox}, N_{it}, S_0, μ) for novel Si BJT/ SiGe HBT and for MOSFET/SOI MOSFET with high-k gate oxide structures are added [21];

Neutron models are based on displacement effects. The adequate models of radiation-dependent parameters (τ, μ, n/p) are included. They take into account the dependencies on neutron fluence, doping levels, injection effectivities of electrons and holes [22];

Proton model was developed by authors [23]. It is based on additive approach combined the ionization and displacement effects influence on device structure.

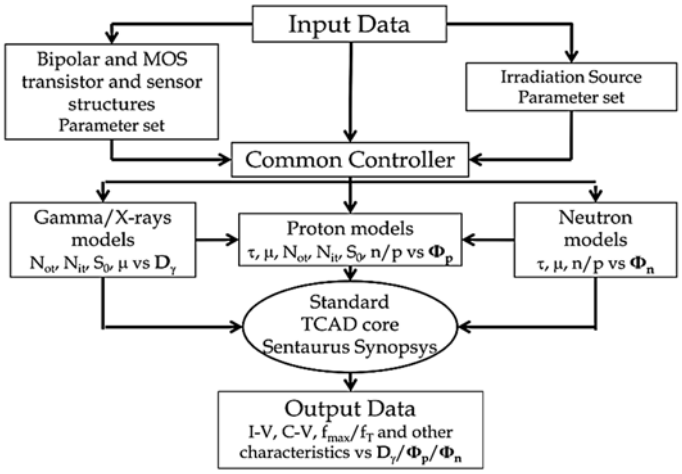


Fig. 1. TCAD-RAD Subsystem taking into account gamma, neutron, proton irradiation influence on electrical device characteristics.

[1] The radiation models based on Monte-Carlo approach 0-0 are not discussed in this paper. They are the subject of original research.

4. Library of Radiation Models

The basic physical parameters describing the carrier transportation (μ_n, μ_p), surface (S_n, S_p) and volume (R_n, R_p) recombination, charge collection in bulk (Q_n, Q_p) and oxide (Q_{ox}) volumes, and on semiconductor/oxide interfaces (Q_{it}) are radiation-dependent.

So the library of physical parameter models for different types of irradiation is the key element of the TCAD-RAD software tools. In the wide-used commercial TCAD tools [12-13] the library of radiation models is poor and not always applicable for practical requirements.

In this work the version of Synopsys Sentaurus RAD tool with the complete library of radiation-dependent physical parameter models valid for gamma rays, neutron and proton irradiation is presented (see Fig. 2).

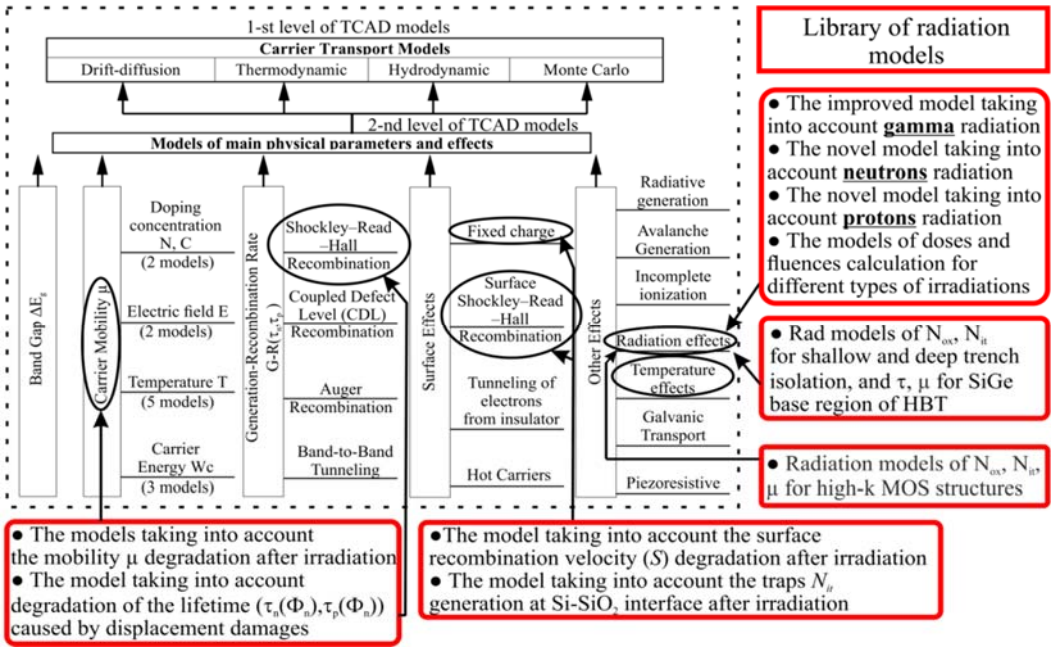


Fig. 2. Radiation models of device electro physical parameters included in the TCAD-RAD system.

a. Gamma radiation models. Irradiation of BJTs/HBTs, bulk/SOI MOSFETs and bipolar and MOS sensor structures by gamma-rays results in the generation of electron-hole pairs in bulk silicon regions; the increase of surface recombination velocity (S) and volume recombination rate (R); creation of traps at the Si-SiO_2 interfaces (N_{it}); collection of positive charge in the gate/STI/BOX oxide (Q_{ox}); decrease of carrier mobility (μ).

For BJTs/HBTs it leads to base and collector leakage currents increase, current gain and maximal/cut-off frequencies degradation; for MOSFETs – to gate/drain leakage current increase, threshold voltage (V_{th}) and subthreshold slope (S) degradation.

In the commercial TCAD version only one degradation factor – the space charge in SiO_2 oxide (Q_{ox}) dependence on gamma dose is taken into account correctly.

Therefore, in order adequately to take into account all the factors caused by gamma radiation influence on the characteristics of Si BJTs/SiGe HBTs and bulk/SOI MOSFETs it is necessary additionally to introduce into TCAD tool the physical expressions for the concentration of traps N_{it} and the surface recombination velocity S at the interfaces Si-SiO_2 depending on the absorbed dose of gamma radiation $D\gamma$:

$$N_{it}(D_\gamma) = a_{it} \cdot D_\gamma^{\,b_{it}}, \qquad (1)$$

where a_{it}, b_{it} are the fitting parameters that have different values for EB spacer and STI/DTI surfaces.

The model parameters a_{it}, b_{it} are defined from experimental dependencies of Si-SiO_2 interface traps concentrations on absorbed dose D_γ [24] (see Fig. 3).

The surface recombination velocity is proportional to the density of traps at Si-SiO_2 interfaces [25-26]:

$$S(D_\gamma) \cong \sigma v_{th} N_{it}(D_\gamma), \qquad (2)$$

where $\sigma = \sqrt{\sigma_n \cdot \sigma_p}$, σ_n, σ_p are the capture cross-sections for electron and hole traps; v_{th} is the thermal velocity.

The modified dependence on radiation dose for the charge carrier mobility μ_{eff} was introduced. The model takes into account the mobility decrease caused by radiation induced surface states on the SiO_2/Si interfaces:

$$\mu_{\text{eff}}(\text{D}) = \frac{\mu_0}{1 + \alpha N_{it}(D)}, \quad (3)$$

where μ_0 is the pre-rad mobility, $N_{it}(D)$ is the silicon-oxide interface trap density, α is a fitting parameter.

Note that the developed models of radiation-dependent parameters (N_{it}, S, Q_{ox}, μ) for novel deep submicron SiGe HBT [23] and high-k gate SOI MOSFET [21], [27] structures differ from the corresponding models for conventional BJT and MOSFET structures. For example in Fig. 4. the radiation-dependent parameter N_{it} at HfO_2, BOX and STI interfaces of 45 nm MOSFET with HfO_2 gate oxide is presented.

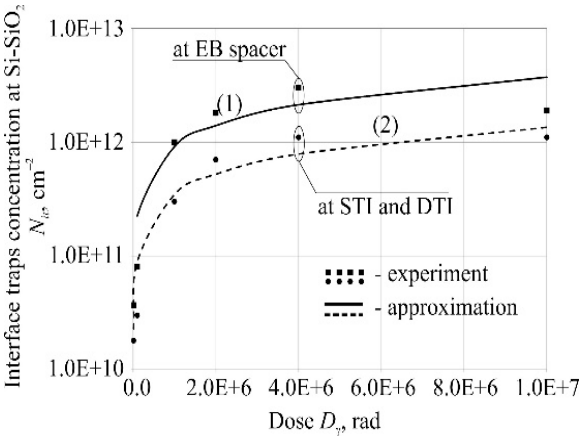


Fig. 3. Dependence of traps concentration at Si-SiO_2 interfaces of EB spacer and shallow and deep trench isolation on absorbed dose D_γ.

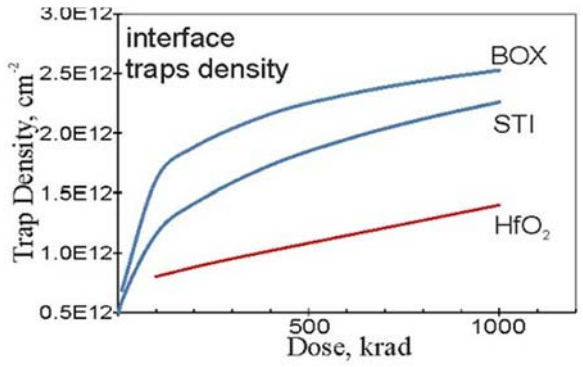


Fig. 4. Trap densities N_{it} at different interfaces of 45 nm MOSFET with HfO_2 gate oxide structure.

The dependences of recombination velocity $S(D_\gamma)$, the traps concentration $N_{it}(D_\gamma)$ at Si-SiO_2 interfaces of EB spacer and STI/DTI and carrier mobility $\mu(D_\gamma)$ on absorbed dose were included in the Synopsys Sentaurus using the physical model interface (PMI).

b. Neutron radiation models. The silicon physical parameters, such as the lifetime of the minority charge carriers (τ), mobility (μ) and the concentration of nonequilibrium charge carriers (n/p), are degraded after impact of neutrons in consequence of the displacement defects formation [28]. The decrease of the minority carrier lifetime is the main factor that influences on the device characteristics. For BJTs/HBTs it is the increase of base current, reduction of the current gain and cut-off/maximum frequencies.

For MOSFETs it is the transconductance g_m and saturation current I_{sat} decrease, and the shift of threshold voltage ΔV_{th}.

In all the commercial versions of TCAD the minority carrier lifetimes τ_n, τ_p are not depended on radiation influence.

So for simulation of minority carrier lifetime decrease due to displacement effects after neutron irradiation the following equation was introduced:

$$\frac{1}{\tau_\phi} = \frac{1}{\tau_0} + \Phi_n \cdot K_\tau, \quad (4)$$

where τ_0, τ_Φ are the minority carrier lifetimes before and after irradiation; Φ_n is the neutron fluence; K_τ is the coefficient of radiation-induced alteration of carrier lifetime.

It was shown experimentally that for modern npn and pnp Si BJTs/SiGe HBTs the parameter K_τ in (4) depends on the doping concentration N_{dop} and the injection efficiency $\delta = n_{min}/n_{maj}$ (where n_{min}, n_{maj} are the minority and majority carrier concentrations) [29-30]. Therefore, the special equation for K_τ (δ, N_{dop}) was introduced [23].

The expression (4) for the lifetime with alteration coefficient K_τ (δ, N_{dop}) was added to the standard Shockley-Read-Hall recombination model using the PMI. Along with the radiation effects, the developed model (4) takes into account the dependence of the lifetime on the temperature. The combined influence of radiation and temperature is the important factor for modern Si BJTs and SiGe HBTs working in harsh conditions.

In Fig. 5 the current gain damage factor $d = \beta(\Phi_n)/\beta(0)$ for the SiGe HBT 8WL after neutron irradiation is presented. It is seen that the improved model (4) provides better results than the classic Gregory model [31].

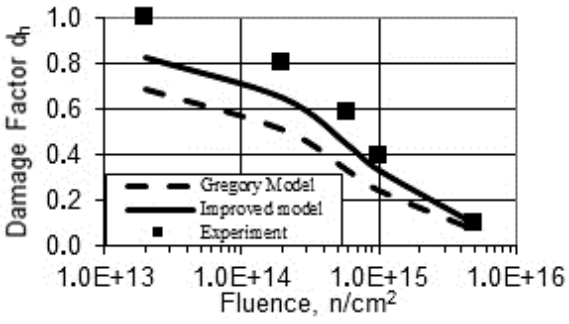


Fig. 5. The current gain damage factor for the SiGe HBT 8WL after neutron irradiation.

c. Proton radiation model. The proton irradiation involves simultaneously the ionization and

displacement damages in semiconductor device structures. Conformably to TCAD modeling of BJT/HBT and MOSFET structures the radiation model for protons was first developed in our works [23], [32]. It is based on additive approach combined two models: model for gamma rays describing the ionization effects and model for neutrons describing the displacement effects. Both models were discussed above.

For the correct modeling of the Si BJT/SiGe HBT and MOSFET characteristics, it is necessary to determine the values of the neutron fluence Φ_n and the gamma dose D_γ equivalent to proton fluence Φ_p. For this purpose, the following equations were used:

$$\Phi_n = K_D \cdot \Phi_p ;\ D_\gamma = K_{I_p}(E) \cdot \Phi_p , \qquad (5)$$

where $K_D = \delta_{cp}(E)/\delta_{cn}(E)$, K_D is the proportion coefficient; $\delta_{cp}(E)$, $\delta_{cn}(E)$ are the energy-dependent non-ionization energy losses (NIEL) for protons and neutrons respectively [28]; $K_{i_p}(E)$ is the proton linear energy transfer (LET) in material with the same energy [33]. The special converter was developed and included in model library for realization of the procedure (5).

5. Simulation Results

The potentialities of TCAD-RAD subsystem are illustrated by means of examples of Si BJTs/ SiGe HBTs and SOI MOSFETs which are used for rad-hard BiCMOS ICs design (see Fig. 6 – Fig. 15).

a. Neutron irradiation. The radiation-hardness of two devices after neutron irradiation was analyzed with developed model. The discrete Si npn BJT 2T378 with following parameters: current gain $\beta = 70$, cut-off frequency $f_T = 1.9$ GHz and maximal frequency $f_{max} = 5.1$ GHz is used in microwave amplifier hybrid ICs. The BJT structure for TCAD simulation is presented in Fig. 6.

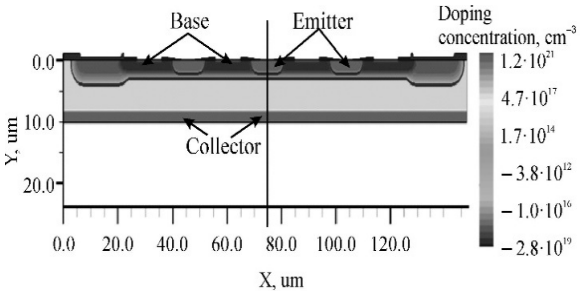


Fig. 6. TCAD interpretation of the Si BJT 2T378 structure.

The 2 um p-MOSFET (L = 2 um, W = 72 um, t_{ox} = 30 nm, t_{Si} = 80 nm, t_{BOX} = 400 nm, $N_{ch} = 2.4 \cdot 10^{16}$ cm^{-3}) was used as a part of the detector for strong neutron background in high-energy physics experiments at CERN [34]. The MOSFET structure for TCAD simulation is presented in Fig. 7.

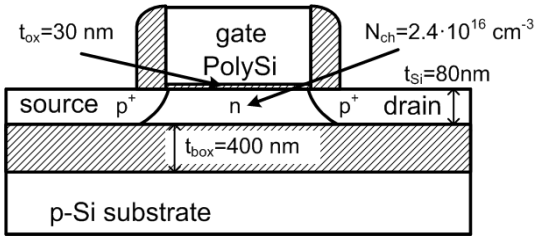


Fig. 7. Cross-section of 2 um SOI p-MOSFET (L/W = 2/72 um, t_{ox} = 30 nm, t_{Si} = 80 nm, t_{BOX} = 400 nm).

In Fig. 8 experimental and simulated results for the current gain of the Si BJT characteristics before and after neutrons irradiation are shown. It is seen that the radiation hardness is limited by fluence $\Phi_n = 4 \cdot 10^{13}$ 1/cm^2 at which the pick values of current gain decrease twice.

In Fig. 9 experimental and simulated I_dV_g characteristics in OFF regime (V_{ds} = 50 mV) for the 2 um SOI p-MOSFET are shown. It is seen that the threshold voltage shift is ΔV_{th}=1.2 V, and the drain leakage current is not sensitive to neutron irradiation fluence up to $2.2 \cdot 10^{14}$ cm^{-2} in OFF regime.

For both examples the simulation error is not more than 15 %.

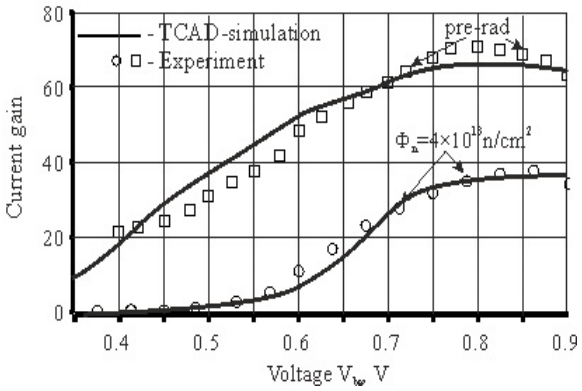


Fig. 8. Current Gain of Si BJT 2T378 with f_T/f_{max}=2.0/5.1 GHz after neutron irradiation.

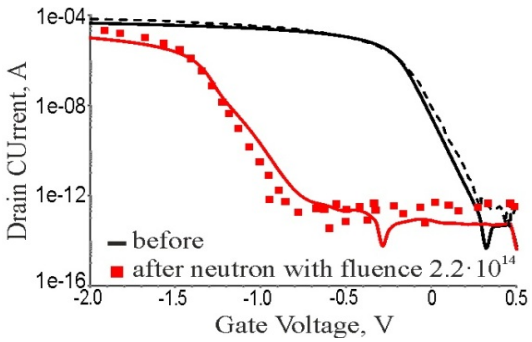


Fig. 9. I_dV_g characteristics of 2 um SOI p-MOSFET after neutron irradiation with fluence $2.2 \cdot 10^{14}$ cm^{-2}.

b. Gamma irradiation. Three examples illustrate the results of the radiation hardness modeling after gamma irradiation for modern deep submicron devices with bipolar and MOS structures.

The SiGe HBT with parameters $\beta = 450$, $f_T = 100$ GHz, $f_{max} = 200$ GHz fabricated by 0.13 μm BiCMOS 8HP technology was investigated [35]. The Gummel I-V characteristics of I_b and I_c for different gamma doses are presented in Fig. 10 and confirm the experimentally observed fact that in SiGe HBTs only the base current is growing after irradiation; at the same time the collector current does not change their values. It is seen a good agreement between simulated and measured characteristics in dose range up to 30 Mrad.

The 45 nm high-k SOI n-MOSFET (W = 0.45 um, $t_{HfO2} = 2$ nm) before and after gamma irradiation [36] was modeled (Fig. 11). It is seen that the SOI MOSFET drain leakage current is growing after radiation influence. The total I_d leakage current is caused basically by parasitic STI channel induced by gamma irradiation. The maximum value of I_{dleak} is limited as 1.0 μA, so the transistor radiation hardness is limited by dose 1.0 Mrad.

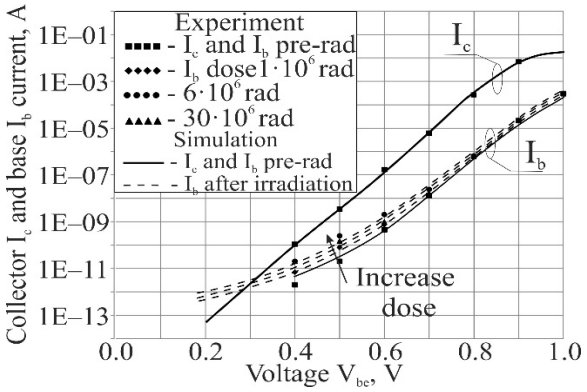


Fig. 10. Gummel characteristics of I_b, I_c for SiGe HBT 8HP after gamma irradiation.

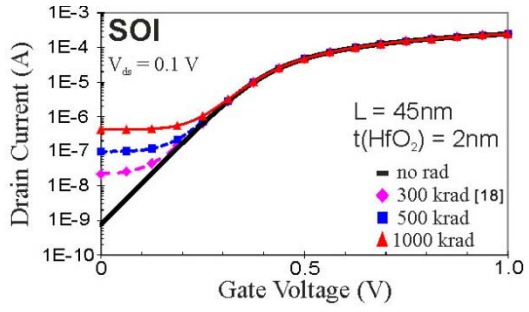


Fig. 11. I_dV_g characteristics of 45 nm SOI high-k MOSFET after gamma irradiation (W=0.45 um, t_{HfO2}=2 nm).

The third object of gamma influence investigation is CMOS image sensors. For this purpose the thick oxide field effect transistors (FOXFET) are used (see. Fig. 12). The n-FOXFET structure with L/W=0.84/300 um, t_{ox}=150 nm was modeled before and after gamma irradiation in ON and OFF regimes. The values of interface state density N_{it} and trapped charge density N_{ot} were taken from experimental work [37]. In Fig. 13 FOXFET subthreshold characteristics are presented. For image sensors the most critical parameter is the dark current. It is seen that the drain leakage current increases significantly with absorbed dose, so the maximal value of gamma dose is limited by 100 krad.

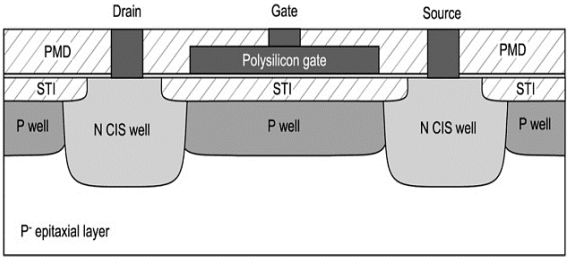


Fig. 12. Cross-sectional view of n-FOXFET structure with L/W=0.84/300 um and thick STI gate oxide t_{ox}=150 nm.

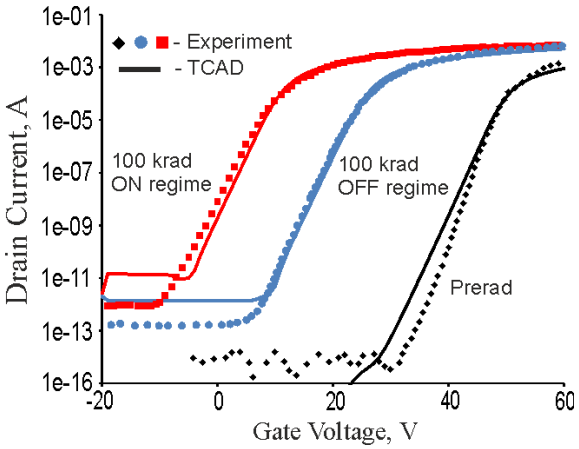


Fig. 13. FOXFET subthreshold characteristics before irradiation and after 100 krad.

c. Proton irradiation. Fig. 14 and Fig. 15 illustrate the results obtained using the developed models taken into account proton irradiation effects.

The 180 nm SiGe HBT with $\beta = 250$, $f_T = 120$ GHz, $f_{max} = 100$ GHz [38] was selected for proton radiation hardness investigation with the Synopsys Sentaurus. The comparison of simulated results with experimental data for current gain is presented in Fig. 14 for the irradiated and non-irradiated device. Using 50 % current gain fall down criteria the proton irradiation upper limit is defined as $5 \cdot 10^{13}$ 1/cm^2.

In Fig. 15 the measured [39] and simulated I_dV_g characteristics of 0.25/8 um SOI n-MOSFET before and after proton irradiation are presented. The protons cause a stronger impact than gamma radiation so in comparison with Fig. 11 for gamma irradiation we can

see in Fig. 15 not only leakage current increase but also threshold voltage shift. As a result the transistor radiation hardness in this case is limited by dose 500 krad.

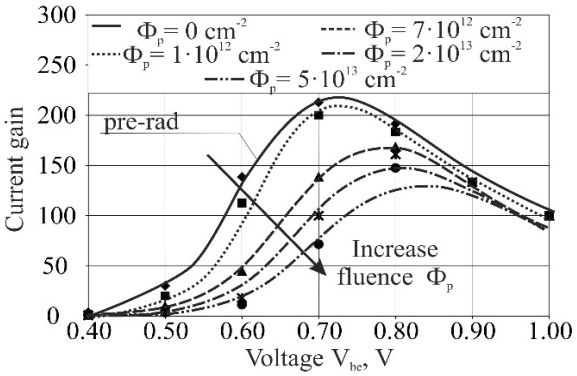


Fig. 14. Current Gain of SiGe HBT 7HP with A_E=0.2x4.52 um^2 f_T/f_{max}=150/180 GHz after proton irradiation.

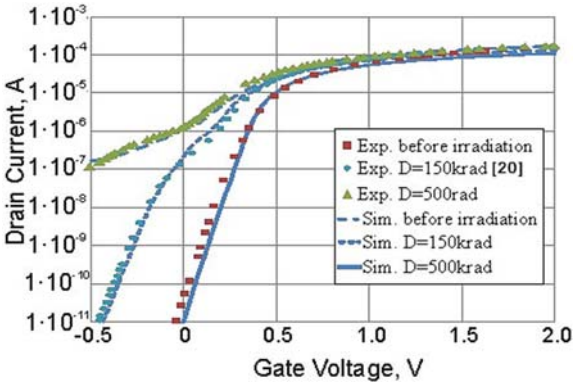


Fig. 15. SOI n-MOSFET characteristics after proton irradiation (L/W = 0.25/8 um, t_{ox} = 7.5 nm, t_{Si} = 50 nm, t_{BOX} = 190 nm).

6. Conclusions

The universal and complete library of radiation-dependent physical parameter models for Si BJT/SiGe HBT, bulk/SOI MOSFET and bipolar and MOS detector structures simulation taking into account neutron, gamma and proton irradiation was developed in the framework of Synopsys Sentaurus TCAD.

The following novelties were introduced into commercial TCAD physical model library:

1) New segment of neutron radiation models which include: improved equations for electron and hole carrier lifetime taken into account the dependence on neutron fluence, doping concentration and injection efficiency; improved equation for carrier mobility dependence on neutron fluence;

2) New segment of proton radiation model based on additive approach combined displacement and ionization damage mechanisms. Two partial models for neutrons and gamma rays are used to calculate simultaneously. The special converter was developed to determine the values of neutron fluence Φ_n and gamma dose D_γ equivalent to proton fluence Φ_p;

3) Segment of gamma radiation models was essentially improved:

- The modified dependence on dose for carrier mobility $\mu_{eff}(D_\gamma)$ was introduced;
- The surface recombination velocity $S(D_\gamma)$ for Si-SiO_2 interfaces was included;
- Approximations of experimental dependencies for traps concentrations $N_{it}(D_\gamma)$, $N_{ot}(D_\gamma)$ at the Si-SiO_2/Si-HfO_2 interfaces and in bulk volumes separately for gate oxide, p-n spaces, BOX, STI/DTI structures were introduced for modeling of conventional bipolar and MOS transistors and sensors, modern deep submicron Si BJTs/SiGe HBTs and bulk/SOI high-k MOSFETs.

Good agreement between simulated and experimental I-V and f_T/f_{max} characteristics for all the devices was achieved. The simulation error is not more then 10-20 %.

The possibilities of TCAD-RAD subsystem with the developed radiation models were illustrated by means of examples of Si BJTs/SiGe HBTs, and bulk/SOI MOSFETs and bipolar and MOS sensors which were used for BiCMOS ICs design taking into account radiation influence.

Acknowledgements

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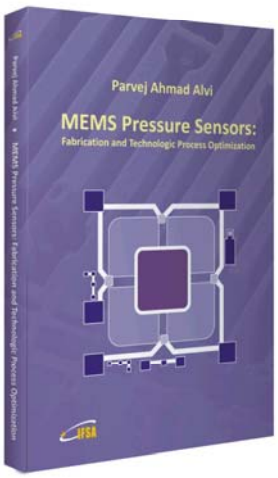
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Parvej Ahmad Alvi

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120 mV-Startup Boost Converter for Thermal Energy Harvesting System

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Abstract: This work presents an ultra-low startup voltage boost converter for thermal energy harvesting. The proposed architecture is composed of an LC-tank oscillator, a 3-stage charge pump and a DC to DC boost converter. A test chip is implemented in a 0.18 μmCMOS technology. The minimum input voltage is 120 mV and output voltage can achieve above 1 V. The output produces regulated 1.2 V and supplies 302 uA current for charging NiMH battery to rated voltage 1.2 V when input voltage is in range from 140 mV to 230 mV. The conversion efficiency is 34 % at minimum input voltage. A maximum efficiency of 60 % can be successfully performed. By incorporating the boost converter and a thermoelectric generator (TEG), a miniaturized module is demonstrated for energy harvesting applications.

Keywords: Boost converter, Conversion efficiency, Energy harvesting, Charge pump, Thermoelectric generator.

1. Introduction

In the past few years, a miniaturized transformer has been developed for the implementation of low-voltage DC to DC boost converter. However, the conversion efficiency is generally low for an input voltage, making it less attractive for applications. In this work, a fully electrical startup circuit is presented. We use native device to implement this circuit so it can easily operate at ultra-low voltage. Furthermore, we combine charge pump with boost converter which demonstrates a minimum input voltage of 120 mV and maximum efficiency of 34 % for thermoelectric energy harvesting applications.

The paper is organized as follows. Section 2 introduces the architecture and operation of the proposed converter. Detailed circuit implementations for each block and experimental results are presented in Sections 3 and Sections 4. Sections 5 shows layout and floor plan. Finally, a concluding remark is given in Sections 6.

2. Architecture and Circuit Design

Fig. 1 shows the block diagram of energy harvesting system, which consists of six function blocks: a LC-tank oscillator, a charge pump, a duty cycle control, a taper buffer, a boost converter and a charge control. As the input voltage V_{in} exceeds the minimum value for startup, which is approximately 120 mV, the LC-tank becomes operational and provides a pair of 300 mV pulse to charge pump, then charge pump starts to charge to 500 mV as duty cycle control's power supply. Duty cycle control is able to produce a clock which amplitude is 500 mV and duty cycle is 75 % in order to drive boost converter successfully. When boost converter startup, it can boost from ultra-low input voltage to 1.3 V output voltage to make charge control circuit normally work. Charge control circuit is like Low drop regulator (LDO), it can regulate the output voltage and additionally provide a protection mechanism to avoid battery over charging.

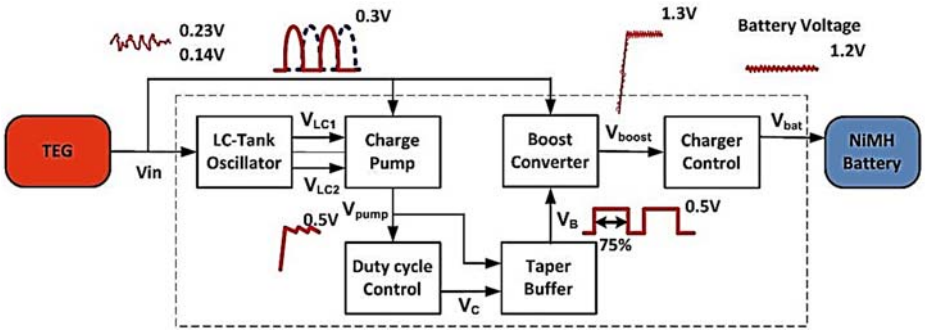


Fig. 1. Block diagram of energy harvesting system.

Finally, this chip give a fixed output voltage 1.2 V and current 300 μA to NiMH charge for storing energy.

3. Circuit Implementation

3.1. LC-Tank Oscillator

Since V_{DD} is ultra-low, charge pump needs enough high amplitude signal to charge to 0.5 V for duty cycle control. So, we use LC-Tank Oscillator. It can provide higher output amplitude $V_{DD} + \Delta V$ for charge pump. Fig. 2 shows loading equivalent LC-Tank Oscillator, C_1, C_2 for the inductance parasitic capacitor, C_C, C_L, R_L is next stage charge pump's coupled capacitor, loading capacitance, loading resistor. For operating low voltage, we use native device M_1, M_2 to cross couple to form a negative resistor. If this negative resistor is greater or equal than inductance's parasitic resistor, making oscillator produce energy is not consumed by parasitic resistor, so LC-Tank can resonates continuously to provide a stable clock signal.

3.2. All Native Differential Drive Charge Pump

There are a lot of techniques for improving charge pump in recent year. Charge pump was developed from Dickson Charge Pump which is limited by threshold voltage reduction for each device. The use of the Static Charge Transfer Switches improves output voltage to avoid threshold voltage drop by connecting gate voltage to the high voltage at the next stage, but make MOS cannot be complete turned off. Dynamic Charge Transfer Switches not only decrease the threshold voltage reduction, but also turn MOS on and off properly. However, output voltage is boosted in one of the two phases only. Differential Drive Charge Pump operates in full cycle of control signal and reduces threshold voltage drop at same time, it has more conversion efficiency in recent years. So we choose Differential Drive Charge Pump as the proposed circuit's charge pump, moreover, Fig. 3 shows the proposed charge pump, we use all native device other than NMOS or PMOS, make it be suitable for operating at low ultra-voltage. In addition to, we apply accumulation-mode MOS varactor which is higher capacitance than common MIM capacitor at low voltage. It can save chip area to reduce cost.

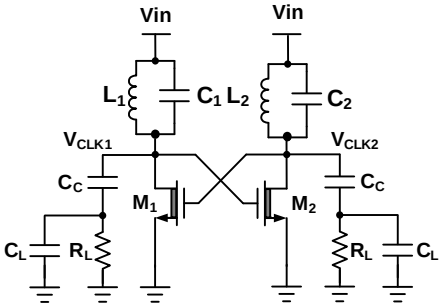


Fig. 2. Loading equivalent LC-Tank Oscillator.

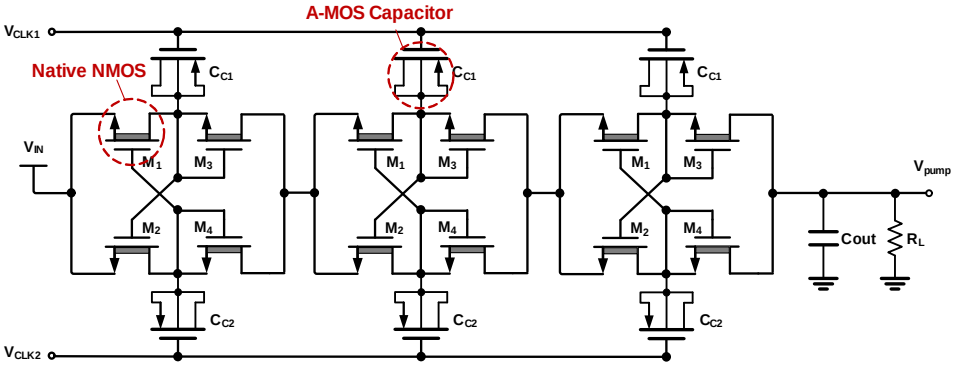


Fig. 3. All Native Differential Drive Charge Pump.

3.3. Duty Cycle Control

Fig. 4 shows a ring oscillator. First, we need a clock amplitude which is 0.45~0.55 V to control next stage boost converter's power NMOS switch only if boost converter startup successful. So, we use a simple structure ring oscillator to provide a clock for boost converter. Besides, we employ a combined logic circuit which consists of a D Flip-Flop, a NAND gate through transmission gate constituting to help boost converter rise greater output voltage. They are displayed in Fig. 5. Following, we connect D Flip-Flop's input D and inverse output Q-. It will produce a half frequency signal Q. Connecting CLK, Q, Q- to NAND gate, it adjust to turn on upper or lower transmission gate conduct input signal to provide a 75 % duty cycle for boost converter. Fig. 6 shows signal waveform.

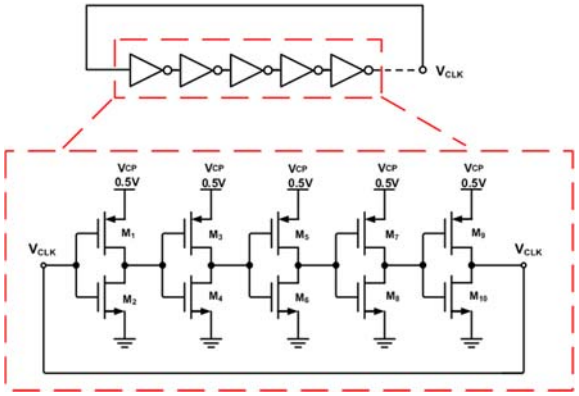


Fig. 4. Ring Oscillator.

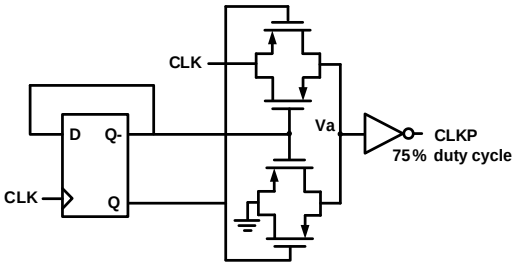


Fig. 5. D Flip-Flop and NAND gate.

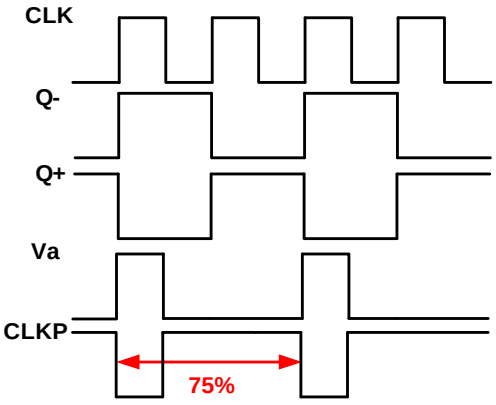


Fig. 6. Signal Waveform.

3.4. Taper Buffer

Fig. 7 shows Taper Buffer. We need to use a taper buffer to enhance its driving capability because boost converter's power MOS is large size. This circuit we simply series even stages inverter to avoid changing signal logic. Additionally, we employ dynamic threshold control technology which connects MOS's source and gate to increase output current efficiently. When NMOS turn on, NMOS's V_{BS} is high, according to body effect Formula (1). Thus, we can know that threshold voltage decreases and saturation current increases.

$$Vth = Vth0 + \gamma(\sqrt{|2\emptyset_F + V_{SB}|} - \sqrt{|2\emptyset_F|}) \qquad (1)$$

3.5. Boost Converter

Fig. 8 shows the traditional boost converter. We employ this converter as main boost circuit which is driven by previous stage providing a 75 % duty cycle clock. Additionally, we use NMOS as a power MOS because NMOS has lower threshold voltage than PMOS in process that can reduce previous stage's load. This circuit operates discontinuous conduction mode (DCM) because we need to boost to higher voltage from ultra-low input voltage. The DCM can provide a higher boost ratio and we will derive its formula in later.

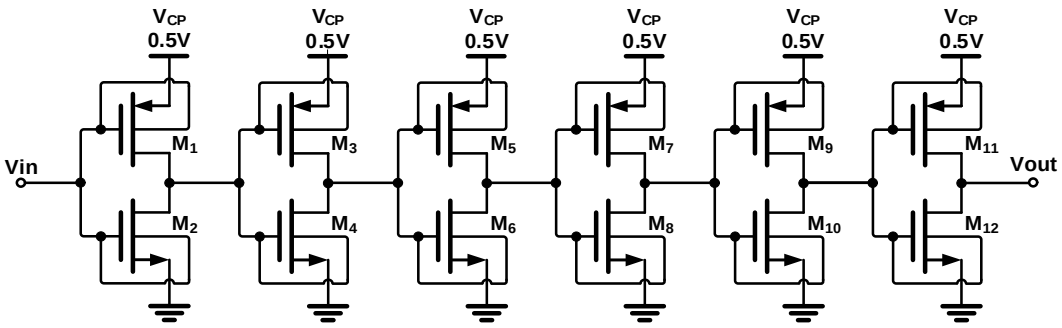


Fig. 7. Taper Buffer.

Finally, we replace diode with diode-connected NMOS to implement this converter because NMOS is easily designed and controlled.

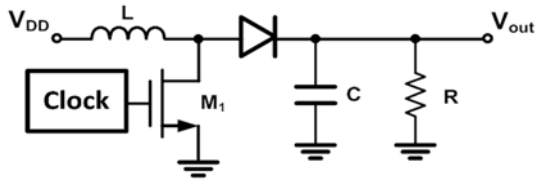


Fig. 8. Boost Converter.

Next, we introduce the principle of operation. First, in Fig. 9, you can see boost converter operates at charged period, and the inductor-current flow through the power MOS M_1 to ground. At the same time, the inductor starts to store energy.

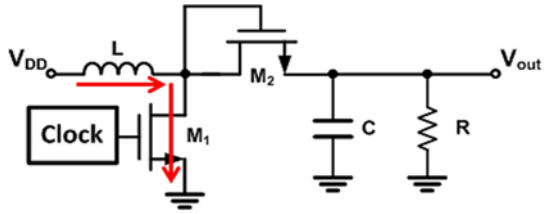


Fig. 9. Boost Converter in charged period.

The inductor-current start to increase linearly that can be calculated by using familiar relationship:

$$\Delta I_L(+) = \frac{V_L}{L} \times T_{on} = \frac{V_L}{L} \times D \times T_S \qquad (2)$$

The quantity $\Delta I_L(+)$ is the inductor ripple current, V_L is inductor-voltage, D is duty cycle, the period T_{on} is state that NMOS turn on. During this period, output load current is supplied by output capacitor C.

Fig. 10 shows that boost converter at discharged period, and the inductor-current flow through diode-connected NMOS to output load. Because inductor resists current change, it happens Lenz's law that make the inductor-voltage boost. Finally, the inductor-voltage plus V_{DD} can reach higher output voltage.

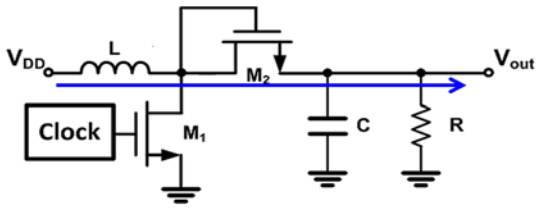


Fig. 10. Boost Converter in discharged period.

The inductor-current decrease during the NMOS off state is given by:

$$\Delta I_L(-) = \frac{V_{out} - V_{DD}}{L} \times T_{off} = \frac{V_L}{L} \times D_2 \times T_S \qquad (3)$$

The period T_{off} is the NMOS turn off period, D_2 is the complementary duty cycle D. Because $\Delta I_L(+)$ must be equal to $\Delta I_L(-)$, we can give an equation for V_{out} is:

$$V_{out} = V_{DD} \times \frac{T_{on} + T_{off}}{T_{off}} = V_{DD} \times \frac{D + D_2}{D_2} \qquad (4)$$

Now we calculate the output current which is average over the complete switching cycle of the inductor-current during the D_2 interval:

$$I_{out} = \frac{V_{out}}{R} = \frac{1}{T_S} \times [\frac{1}{2} \times (\frac{V_L}{L} \times D \times T_S) \times D_2 \times T_S] \qquad (5)$$

Then, simplifying I_{out} equation can obtain an equation for V_{out} is:

$$I_{out} = \frac{V_{out}}{R} = \frac{V_{DD} \times D \times D_2 \times T_S}{2 \times L} \qquad (6)$$

We now have two equations, one for the output current, and one for output voltage. Then solve each equation for D_2 and set the two equations equal to each other. The resulting equation can be used to derive an expression for discontinuous conduction mode output voltage V_{out} is:

$$\frac{V_{out}}{V_{in}} = 0.5 + 0.5\sqrt{1 + \frac{2D^2 R_{load} T_S}{L}} \qquad (7)$$

Thus, we can change many parameters duty cycle D, inductance L and the clock period T_S to adjust boost ratio which we need.

Next, we will introduce inductance value which we how choose. A boost converter can be designed to operate in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) for load current. Thus we can calculate output current to determine inductance value. First, define output current as the minimum current to maintain continuous conduction mode, normally referred to as the critical current. It is easier to perform the derivation using the inductor current. The minimum average inductor current to maintain continuous conduction mode is given by:

$$I_{min} = \frac{\Delta I_L}{2} \qquad (8)$$

Second, calculate L such that the above relationship is satisfied. To solve the above equation, we use $\Delta I_L(+)$. The worst case condition for the boost converter is at input voltage equal to one-half of the output voltage because this gives the maximum ΔI_L. Now, we substitute and solve for L_{min}:

$$L_{min} \geq \frac{1}{2} \times V_{in} \times T_S \times D \times I_{min} \qquad (9)$$

The above equation can be simplified to shown:

$$L_{min} \geq \frac{V_{out} \times T_S}{16 \times I_{out}} \quad (10)$$

Using the inductor value which is just calculated ensures operation for output load current above the critical current. For example, if we want to operate DCM, we can select inductor value is less than L_{min} to correspond with requiring output current.

Conversion efficiency is very important for boost converter. Generally, diode-connected M_2 threshold voltage is mainly influenced factor because it will have a voltage drop which cause large power consumption. Traditional, we usually connect M_2 body with ground and its threshold voltage which is 793 mV will be very high result from body effect. Moreover, even if we connect to source to avoid body effect influenced, its threshold voltage still has 515 mV. Both threshold voltages are shown in Fig. 11. Thus, we design an improved boost convert which is displayed in Fig. 12. In this converter, we extra add a diode-connected NMOS M_3 connect original diode-connected NMOS M_2 body. While M_3 turn on, its drain voltage conduct to M_2 body then M_2 source-bulk voltage V_{SB2} will be negative that can make M_2 threshold voltage be lower. So this converter can increase conversion efficiency successfully by reducing M_2 voltage drop. Simulation is shown in Fig. 13.

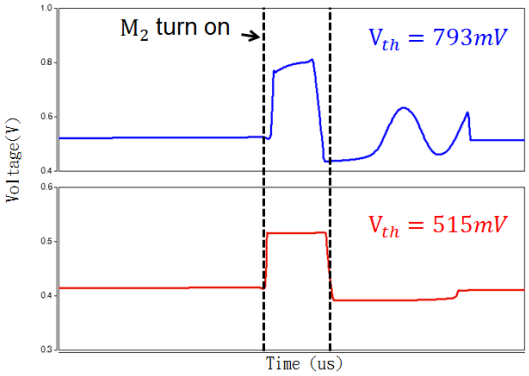


Fig. 11. Threshold voltage simulation.

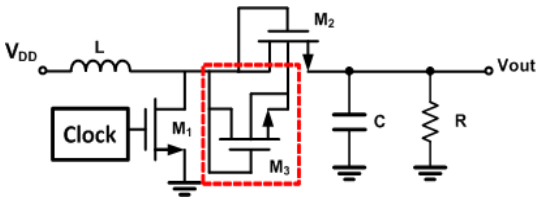


Fig. 12. Improved Boost Converter.

Fig. 14 shows signal simulation, we can see original diode-connected NMOS M_2's drain-source V_{DS}, drain-body V_{DB} and source-body V_{SB} are not exceeded 1.8 V while input voltage is 0.2 V. Thus, this harvesting system has no any component reliability problem because NMOS's any two terminals relative voltage is not too high to cause component destroyed.

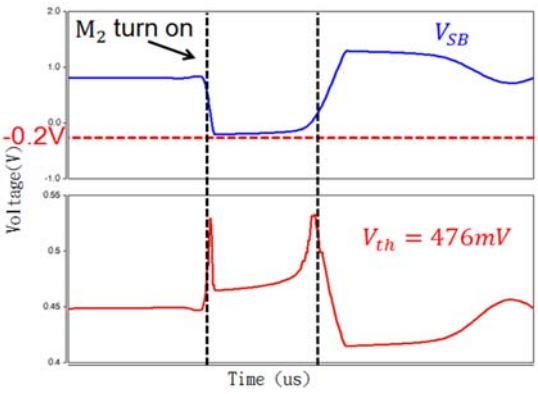


Fig. 13. Improved diode-connected NMOS's V_{th}.

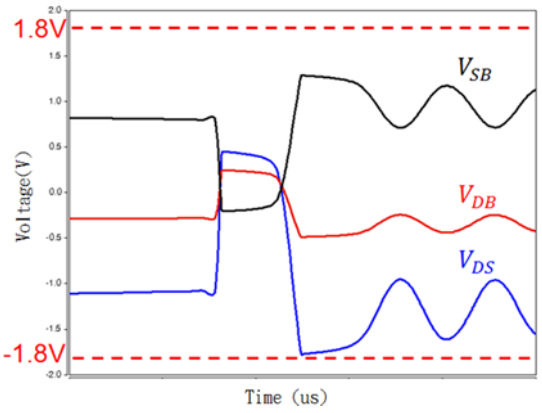


Fig. 14. Diode-connected NMOS M_2 V_{SB}, V_{DB}, V_{DS}.

3.6. Charge Control

Fig. 15 shows Charge Control. We use boost converter's output voltage as this circuit power supply. Operation shows in Fig. 16. We employ an operational amplifier (op) as a comparator to control PMOS switch. If the battery is not full charge, op will provide a high signal to turn off M_3, then current mirror turn on and copy a 300 μA current to charge the battery until the battery reach 1.2 V. When the battery's voltage is 1.2 V, op provide a low signal to make M_3 turn on. At the same time, current mirror turn off and use remained current to charge the battery. It can protect the battery to avoid overcharge that maybe damage the battery.

Next, the bandgap voltage reference circuit is composed of a BJT, six stages proportional to absolute temperature (PTAT) and a current reference circuit. So the voltage reference V_{ref} is fixed output voltage and can be insensitive to process, temperature, supply voltage. Furthermore, owing to lower V_{boost} which is only 1.3 V, current reference circuit is that cascode

three-level other than four-level in order to operate all MOS in saturation region.

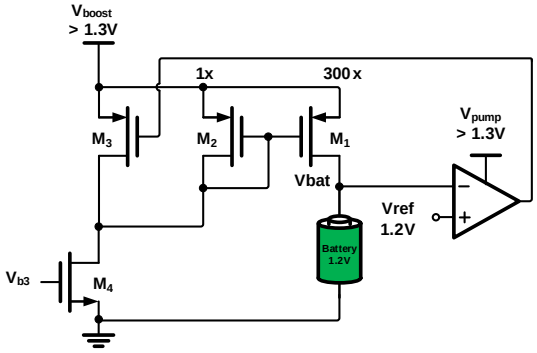


Fig. 15. Charge Control.

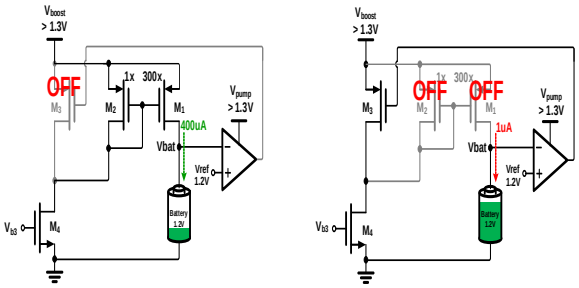


Fig. 16. Charge Control operation.

4. Experimental Results

Fig. 17 shows LC-tank measurement. As expected, it can provide a complementary clock to charge pump successfully and its amplitude achieves approximately double input voltage which range from 140~230 mV, clock frequency also has 5 MHz.

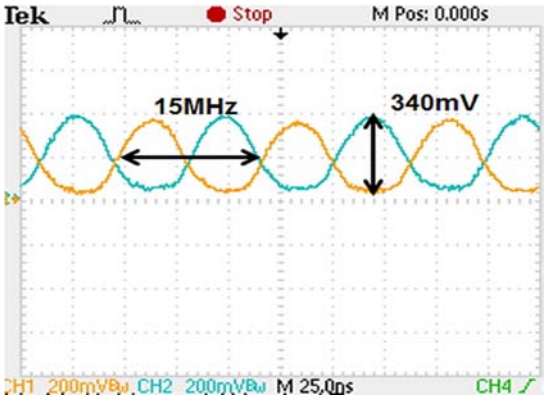


Fig. 17. LC-tank Measurement.

Fig. 18 shows Charge Pump and Duty Cycle. As usual, Charge Pump is able to boost input voltage to 500~600 mV in input voltage is from 140 mV to 230 mV, and as a stable power supply for next stage duty cycle control. Duty Cycle Control can normally produce a clock which amplitude reaches 500~600 mV and clock frequency is 5 MHz that is very important because clock signal frequency will influence next stage boost converter's boost ratio seriously.

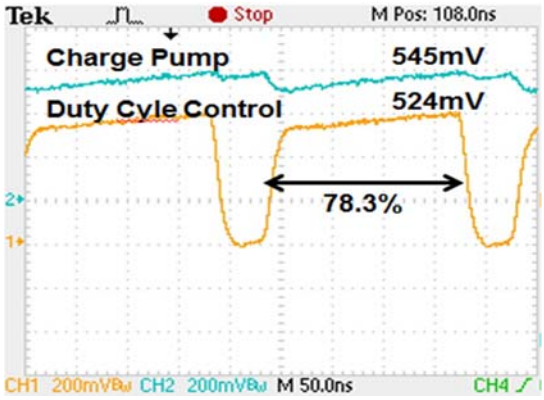


Fig. 18. Charge Pump and Duty Cycle Control Measurement.

Fig. 19 shows Boost Converter measurement in input voltage 140 mV and it can successfully boost input voltage to 1.33 V for final stage Charge Control in 57 ms later. And, its operating voltage 140 mV is minimal because we decrease input voltage under 140 mV at this time; Boost Converter's output voltage is not enough to 1.3 V that makes next stage Charge Control doesn't startup normally. Fig. 20 shows boost converter output voltage curve, you can see input voltage 0.14~0.23 V is most suitable because its output voltage is enough 1.3 V above. If input voltage is too small, its input power is not enough supply for boost converter which is not operating normally, and input voltage is too high, it will be influenced by clock's frequency. Because clock's frequency is too high, boost ratio is not as expected which can be verified by Formula (7). So boost converter also don't work normally. Finally, we test this chip's boost converter's output current in changing load, you can observe it's curve which shows in Fig. 21 correspond with ohm' law. It represents this chip is able to adjust output current in different load and provide a stable output current to load.

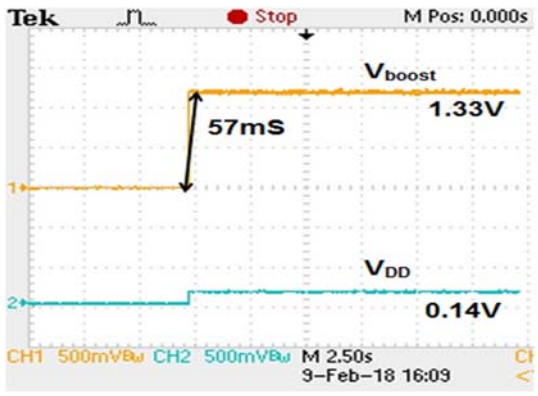


Fig. 19. Boost Converter Measurement.

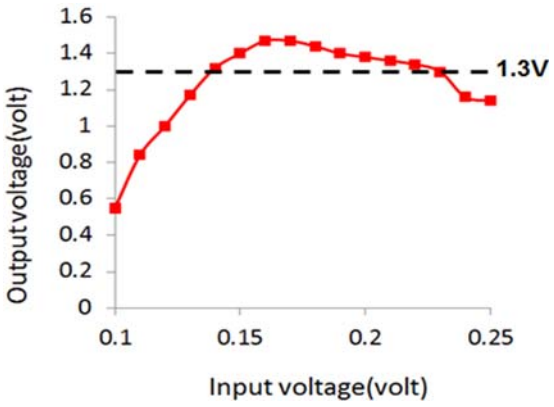


Fig. 20. Boost Converter Output Voltage Measurement.

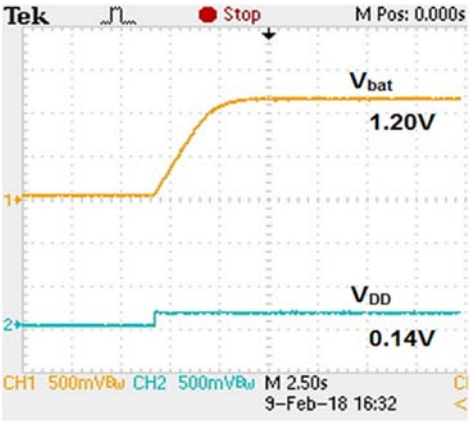


Fig. 22. Charge Control Measurement.

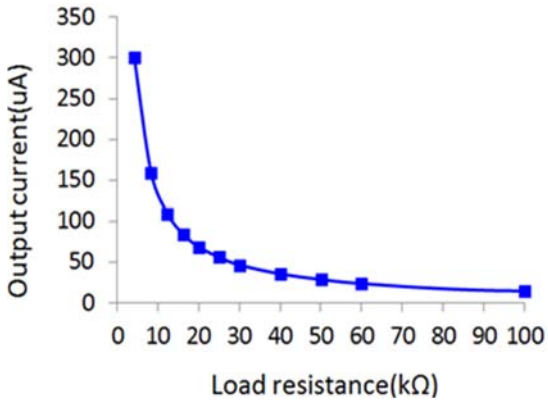


Fig. 21. Boost Converter Output Current Measurement.

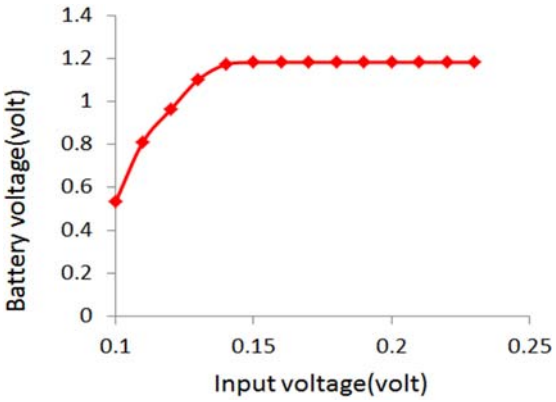


Fig. 23. NiMH battery charged voltage with input voltage.

Fig. 22 shows Charge Control measurement in input voltage 140 mV and it can successfully charge to NiMH battery to 1.2 V. Fig. 23 show NiMH battery charged voltage in different input voltage. You can observe battery voltage can be charged to 1 V when input voltage is about 0.12 V. Go on increasing input voltage to 0.14 V or higher, battery charged voltage can be successfully to 1.2 V.

Eventually, the measurement of the proposed chip is summarized in Table 1 along with state-of-the-art results from recent publications for comparison. [1-2] and [3] reference are charge pump as main boost circuit for low voltage application, and they use technology forward body biasing, backward control and dynamic body biasing respectively.

Table 1. Comparison with Low-Startup Voltage DC-DC Converter.

No.	[1]	[2]	[3]	[6]	[9]	[10]	This work
Process	65-nm CMOS	130-nm CMOS	180-nm CMOS	180-nm CMOS	CNFET	130-nm CMOS	180-nm CMOS
Min. Startup Voltage	0.18 V	0.15 V	0.32 V	0.12 V	0.10 V	0.07 V	0.12 V
Output Voltage	0.74 V @Vin=0.12 V	0.619 V @Vin=0.18 V	2.65 V @Vin=0.40 V	1.2 V @Vin=0.12 V	1.2 V @Vin=0.12 V	1.25 V @Vin=0.07 V	1.2 V @Vin=0.14 V
Output Current	7.5 uA @Vin=0.12 V	21 uA @Vin=0.18 V	3.359 uA @Vin=0.40 V	220 uA @Vin=0.12 V	120 uA @Vin=0.12 V	12 uA @Vin=0.10 V	302 uA @Vin=0.14 V
Efficiency	--	72.5 % @Vin=0.45 V	89.0 % @Vin=0.32 V	30.0 % @Vin=0.12 V	27.0 % @Vin=0.12 V	58.0 % @Vin=0.08 V	34.0 % @Vin=0.14 V
Off-chip component	None	Capacitor	Capacitor	Inductor	Inductor	PCB Inductor	Inductor Capacitor

You can observe the purposed circuit can operate in lower input voltage compare and provide a larger output to above three. Next, [6, 8, 10] are inductive type DC/DC boost converter as main boost circuit which is similar with the purposed circuit. Compared to [6] and [9], the purposed circuit can supply larger output current for next stage application and have lightly higher conversion efficiency. In [10], it can operate in lower input voltage than this work, but it uses more advanced process. Moreover, its output current is less lower than the purposed circuit. Thus, the purposed circuit will be able to be applied to a wide range of circuit compared with above reference.

5. Layout

Fig. 24 shows layout and floor plan. Core circuit is located center, and MIM capacitor is filled of main circuit above and below because it can be able to symmetry to reduce mismatch.

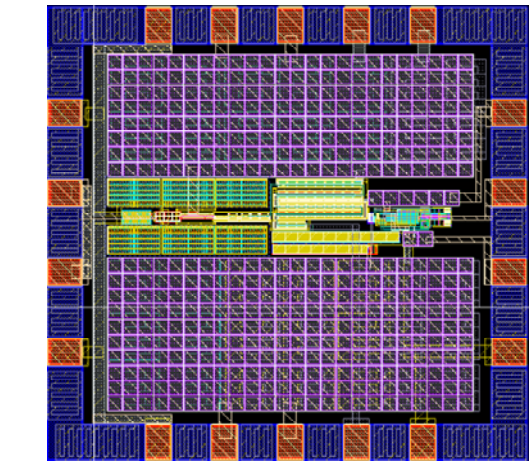


Fig. 24. Layout and Floor plan.

6. Conclusion

In this paper, the proposed harvesting system uses boost converter as a mainly boost circuit and charge pump as auxiliary circuit for startup successfully. Its operating input voltage range can be at 0.14~0.23 V and maximum conversion efficiency is about 34 %. Additionally, we use accumulation-mode MOS varactor to reduce whole chip area which can also reduce cost. In the future, the proposed harvesting system be designed a large output current 302 μA expect for objected battery, this harvesting system will be able to be applied to minimal biomedical circuit directly.

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The Algorithm and Software Implementation of the Thermal Transient Testing Technology Applied in High-Power Electronics

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Abstract: Thermal transient testing technology is currently the most effective method for obtaining thermal characteristic parameters of high-power electronics and the structure functions can be used to evaluate the long life-time reliability. This paper briefly outlines the basic theory of the thermal transient testing technology, and then focuses on two key algorithms in the implementation of this technology: deconvolution and transformation of thermal network model algorithms. Meanwhile, a software system of the thermal transient testing applied to power semiconductor devices is established. Mathematicians used to solve the problem of data accuracy in network model transformation. By comparing the commonly used deconvolution algorithm, it is concluded that the thermal characteristic parameters of the device calculated by Bayesian deconvolution based on Richardson-Lucy algorithm have better accuracy. Finally, the measurement data of power semiconductor devices tested by mature commercial thermal transient testing equipment is set as an example to verify the accuracy and effectiveness of the proposed software system.

Keywords: High-power electronics, Structure function, Thermal transient testing technology, Deconvolution, Thermal network model transformation.

1. Introduction

High-Power semiconductor devices due to high voltage, high current, and excellent switching performance, have gradually been applied to high voltage and high power density applications, for example, IGBT (Insulated Gate Bipolar Transistor) devices are used in the electric traction and high voltage direct current transmission system. Thermal characteristic have always been a quite important concern in the application of power semiconductor devices. 55 % of the failure of electronic devices is caused by heat-related problems [1]. Therefore, it is quite important to accurately measure the thermal parameters of power electronics and analysis its thermal behavior.

For high-power IGBT devices, junction temperature and thermal resistance are two critical thermal characteristics. Many electrical parameters of the device are related to the junction temperature,

which is also affected by its thermal resistance. Thus, accurately measuring the junction temperature and thermal resistance of high-power IGBT devices not only helps to optimize the heat dissipation structure of the device package, but also guides users to give full play to the device performance and prolong its service life. This has become a common concern for the manufacturers and users.

There are two most commonly used methods to obtain the thermal resistance or thermal behavior of power electronics: Traditional steady-state method and transient thermal method [2]. Traditional steady-state method takes a thermocouple to get the case temperature to calculate the thermal resistance. The thermal resistance measured by this method is the behavior of whole packaging, such as the junction to case or heatsink or ambient thermal resistance. It is not easy to obtain more details within packaging. The transient thermal method is to get the thermal behavior of the thermal dissipation path when the heat delivery from the chip to heatsink and the transient thermal impedance measure by this method denotes the thermal resistance and capacity change along with the heat path. Moreover, the transient thermal impedance can be transformed by mathematical transformations to structure functions to get the thermal resistance and capacity of each layer accurately [3]. Thus, the thermal transient testing technology can comprehensively analyze thermal properties of each layer structure within the device from chip to heat sink on the path of heat conduction, construct equivalent thermal model of devices, and provide reliable data base for the research on thermal characteristic of the device [4].

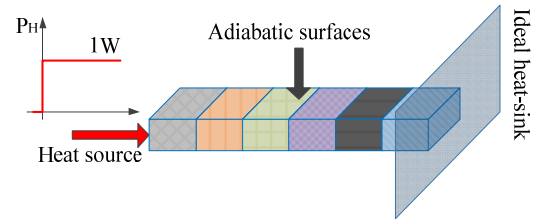
Hence, in order to give full information of the thermal characteristic parameters of high-power electronics, a complete set of software analysis and test system is proposed in this paper. The system can accurately measure the thermal characteristic parameters, and provide reliable data foundation for life expectancy, extreme operation and over-temperature protection [5]. The result has important reference value and practical significance.

2. Methodology

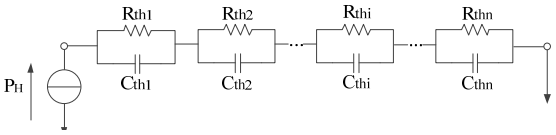
Fig. 1(a) shows a simple packaging model composed of different materials. The model is placed on an ideal heat sink and other surfaces are thermal adiabatic. Thus, the thermal conduction is considered as one-dimensional. When a constant power P_H is applied to the model, the model can be equivalent to the n-order RC network shown in Fig. 1(b). Among them, the thermal transient response function $a(t)$ of the model under the power P_H is

$$a(t) = P_H \cdot \sum_{i=1}^{n} R_{thi}(1-\exp(-\frac{t}{\tau_i})), \quad (1)$$

where P_H is generally the unit power, R_{thi} denotes the thermal resistance of the heat transfer model equivalent to an RC network, t is the time, τ_i represents the time constant and can be calculated by thermal resistance R_{thi} and thermal capacity C_{thi}. The thermal resistance and capacity of each layer is determined by its material properties and geometry [6]. Normally, the geometry of power electronics is not so explicit in application that we should get the transient thermal impedance through measurement [3].



(a) Simple one-dimensional heat transfer model



(b) The equivalent RC network

Fig. 1. Heat transfer model and its equivalent RC network.

When the applied power step denotes as a unit power, the time t in Formula (1) is logarithmic and the Formula (1) can be derived to obtain the convolution formula shown in Formula (2).

$$\frac{d}{dz}a(z) = R(z) \otimes w(z) + n(z), \quad (2)$$

where $\otimes$ is the convolution operator, the $w(z)$ represents the constructor which can be calculated by the following formula

$$w(z) = \exp(z - \exp(z)) \quad (3)$$

The thermal transient response function $a(z)$ in Equation (1) can be obtained by measuring the change of temperature-sensitive parameters of the device in the cooling process and combining the relationship between the temperature-sensitive parameters and the junction temperature and thermal impedance. In addition, the time constant spectrum is clear in Formula (4) is the constructor is given.

$$R(z) = \frac{d}{dz}a(z) \otimes^{-1} w(z), \quad (4)$$

where $\otimes^{-1}$ is the deconvolution operator.

It should be noted that the actual measured thermal transient response signal is usually mixed with a

certain noise signal $n(z)$. These noise signals can affect the results of thermal transient tests that must be taken into account when analyzing.

$$\frac{d}{dz}a(z) = R(z) \otimes w(z) + n(z) \tag{5}$$

The basic process of this technology is shown in Fig. 2 below. We can see that the precondition of the thermal transient testing technology is that the transient thermal impedance given as shown in Formula (1). Thermal transient response signal $a(z)$, time constant spectrum $R(z)$, constructor $w(z)$ and noise $n(z)$ in the Formula (1) are all expressed as function of logarithmic time z. In order to get the $R(z)$ from $a(z)$, the derivative and deconvolution should be conducted on $a(z)$. Then, split $R(z)$ into a number of segments having Δz width and compute the thermal resistance and heat capacity parameters of the Foster model. Considering the heat capacity of Foster model with no clear physical meaning, hence thermal network model transformation algorithm is used to transform the Foster model to Cauer model, which can reflect the actual heat capacity transfer process. Finally, the structure function of the device can be obtained by accumulating the thermal resistance and heat capacity parameters of the Cauer model in stages, or taking the derivative after accumulating [7].

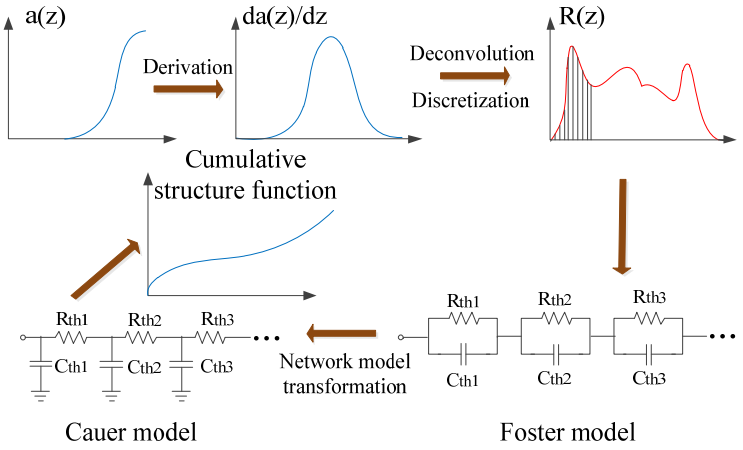


Fig. 2. The process of the thermal transient test technology.

2.1. Deconvolution Algorithm

Up to now, there are two deconvolution algorithms that have been successfully used in the thermal transient testing technology: Fourier deconvolution and Bayesian deconvolution.

2.1.1. Fourier Deconvolution

The Fourier deconvolution algorithm is based on the convolution theorem, which transforms the problem in the time domain to the frequency domain for operations. We have the equivalent formula

$$\begin{aligned} M^*(\Phi) &= V(\Phi) \cdot W(\Phi) + N(\Phi) \\ &= V^*(\Phi) \cdot W(\Phi) \end{aligned} \tag{6}$$

Thus theoretically we can obtain the required function by a simple division as shown in Formula (7).

$$R(z) = IFFT \| \frac{M^*(\Phi)}{W(\Phi)} \| \tag{7}$$

Because the noise corresponds to the high frequency component in the signal spectrum. Although the noise signal has smaller amplitude relative to the measured signal, the high-frequency components of the constructor are some very small items with a smaller magnitude. After the division operation, the noise signal will be amplified, resulting in many differences between the deconvolution reconstruction signal and the original signal, sometimes even resulting in unacceptable results. Therefore, it is necessary to properly handle the noise problem during the application process.

2.1.2. Bayesian Deconvolution

Different from the Fourier deconvolution, Bayesian deconvolution is based on Bayes' theorem and total conditional probability formula. It can avoid the noise problem in Fourier deconvolution algorithm. The procedure described by [8] is suitable for the time-constant spectrum identification has been proven. These applies the following iterative formulas

$$R^{i+1}(z) = R^i(z) \cdot (w(z) \oplus \frac{da(z)/dz}{w(z) \otimes R^i(z)}), \tag{8}$$

$$R^{i+1}(z) = R^i(z) \frac{w(z) \oplus (da(z)/dz)}{w(z) \oplus (w(z) \otimes R^i(z))} \tag{9}$$

The deconvolution algorithm using the iterative formula shown in Equation (8) is called Richardson-Lucy algorithms, and shown in Equation (9) is the Positive iterative deconvolution. Whether Formula (8) or Formula (9), the amplitude of the reconstructed signal will be amplified during each iteration. In order to make the reconstructed signal as close as possible to the original input signal, the correction *I* needs to be introduced to improve the formula.

$$R^{i+1}(z) = R^{i}(z)(w(z) \oplus \frac{da(z)/dz}{w(z) \otimes R^{i}(z)}) * I \,, \qquad (10)$$

$$R^{i+1}(z) = R^{i}(z) \frac{w(z) \oplus (da(z)/dz)}{w(z) \oplus (w(z) \otimes R^{i}(z))} * I \qquad (11)$$

2.2. Network Model Transformation Algorithm

Because the Foster network model describes the node-to-node thermal capacity without explicit physical meaning, the Foster network model needs to be converted into a Cauer network model that describes the thermal capacity between the nodes and reference nodes. The existing network model transformation algorithm has been relatively mature, and the detailed conversion process is given in [7]. However, due to the limitation of software accuracy, truncation error and operation error occur when the network model conversion operation is performed. The obtained structure function is inconsistent with reality. Therefore, appropriate calculation software should be selected during processing to avoid this situation.

The method that have been published and used to solve the data accuracy problem of the network model conversion process in the thermal transient testing technology is the GMP (GNU MP Bignum Library) open source math library mentioned in the JESD 51-14 standard. However, GMP library functions are written in C language. When calling in interpretive language programming software, you need to write a special interface function, or directly use it in the C language-based software. No matter which way the use should have the basic knowledge of programming. The simulation verified that using Mathematica, a multi-precision calculation software, not only can achieve the same accuracy as GMP, but also is simpler and easier to operate than GMP. This greatly reduces the difficulty of algorithm implementation.

Based on the above theory, this paper establishes a software system of thermal transient testing technology as shown in Fig. 3, which is used to measure the thermal characteristic parameters of power electronics.

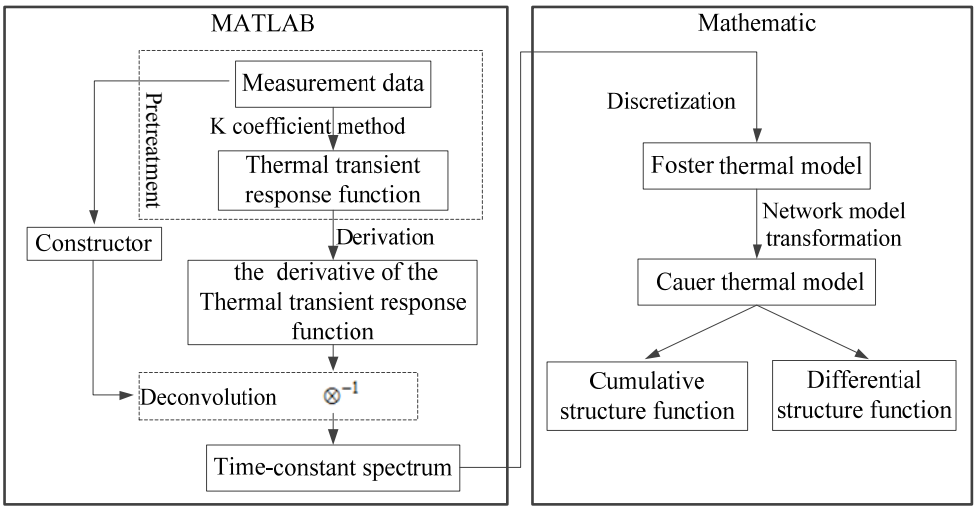


Fig. 3. The Thermal transient testing software system.

3. Case Study

Taking the thermal transient response signal of power electronics measured by commercial thermal transient tester as an example, and the time constant spectrum calculated by the equipment as a reference value. This article compares two kinds of common deconvolution algorithms. Meanwhile, the thermal transient testing software system established in this paper is used for simulation analysis to verify the validity and accuracy of the system. In order to make the results comparable, the simulation parameters are set with the testing equipment parameters.

3.1. Deconvolution Algorithms Comparison

In order to compare the accuracy of thermal transient test results when different deconvolution algorithms are applied, this paper uses different deconvolution algorithms to deal with the same measurement data. The time constant spectrum

deviation Δ is defined as the criterion for measuring the accuracy of the algorithm. The simulation results are shown in Table 1 and Fig. 4.

$$\Delta = \frac{\sum [X(z) - \overline{R}(z)]^2}{n} \tag{12}$$

Table 1. The deviation of time constant spectral calculated by different deconvolution methods.

Deviation	Fourier deconvolution	Bayesian deconvolution	
		Richardson-Lucy algorithm	Positive iterative deconvolution
Δ	0.00131	0.000199	0.000963

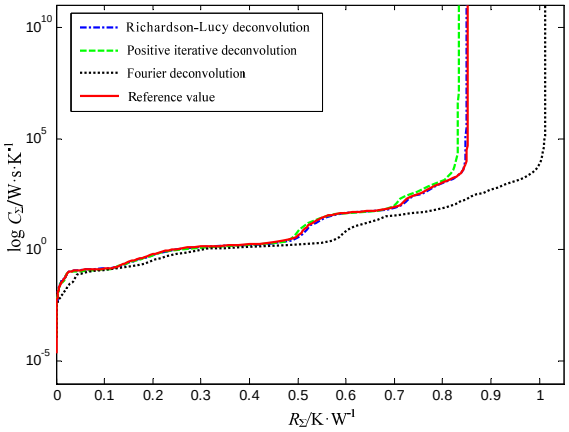


Fig. 4. The structure function of different deconvolution algorithms.

Table 1 shows that the result of Richardson-Lucy algorithm is closer to the reference value. The deviation of Richardson-Lucy algorithm is 0.000199, which is far less than the Fourier deconvolution, and less than the positive iterative deconvolution. The result also shows that compared with the Fourier deconvolution algorithm and the Bayesian deconvolution based on the Positive iterative deconvolution, the structure function using the Bayesian deconvolution based on the Richardson-Lucy algorithm is most consistent with the reference value.

3.2. The Simulation Verification of Software System

Taking the measurement data of a high-power semiconductor device as an example, the thermal transient testing software system established in this paper is used for simulation calculation. The device under test is a single IGBT chip submodule from press pack IGBT. The collector side of the submodule is cooled by heatsink and emitter side is thermal insulation during the transient thermal impedance measurement [9]. And then, the measured thermal impedance is used to obtain the structure function curves which is shown in Fig. 5 and Fig. 6.

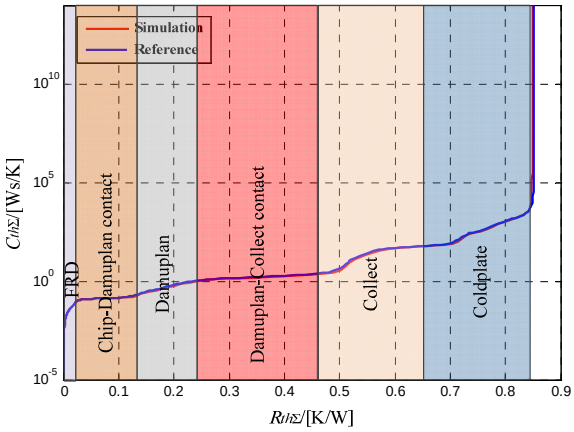


Fig. 5. Cumulative structure function.

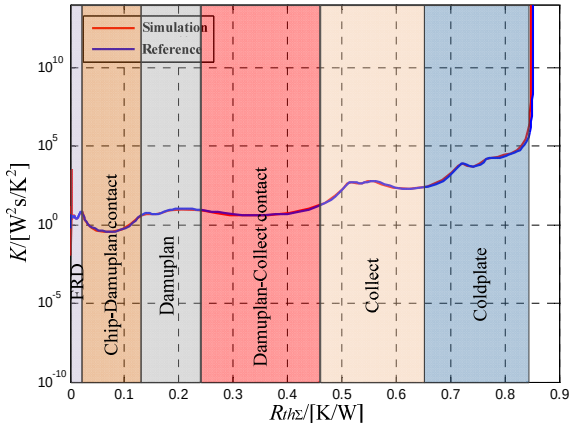


Fig. 6. Differential structure function.

Choosing the structure function curve obtained from the thermal transient testing equipment as a reference, it can be seen that the simulation results through the software system mentioned above are in good agreement with the reference values. The error between them is very small. Therefore, the software system established in this paper can obtain the thermal parameters of the device accurately and effectively. Furthermore, the internal structure of the device can be identified by combining two structure functions. Each layer structure is marked with different colors respectively.

The software established in this paper contains five main parts as shown in Fig. 7 below. Firstly, the transient thermal impedance should be loaded in the program and then make a derivation on it. After that the deconvolution is used to get time constant spectra and then transform to Foster thermal network model by discretization. Finally, we should transform the Foster thermal model to Cauer thermal model to get the cumulative and differential structure functions.

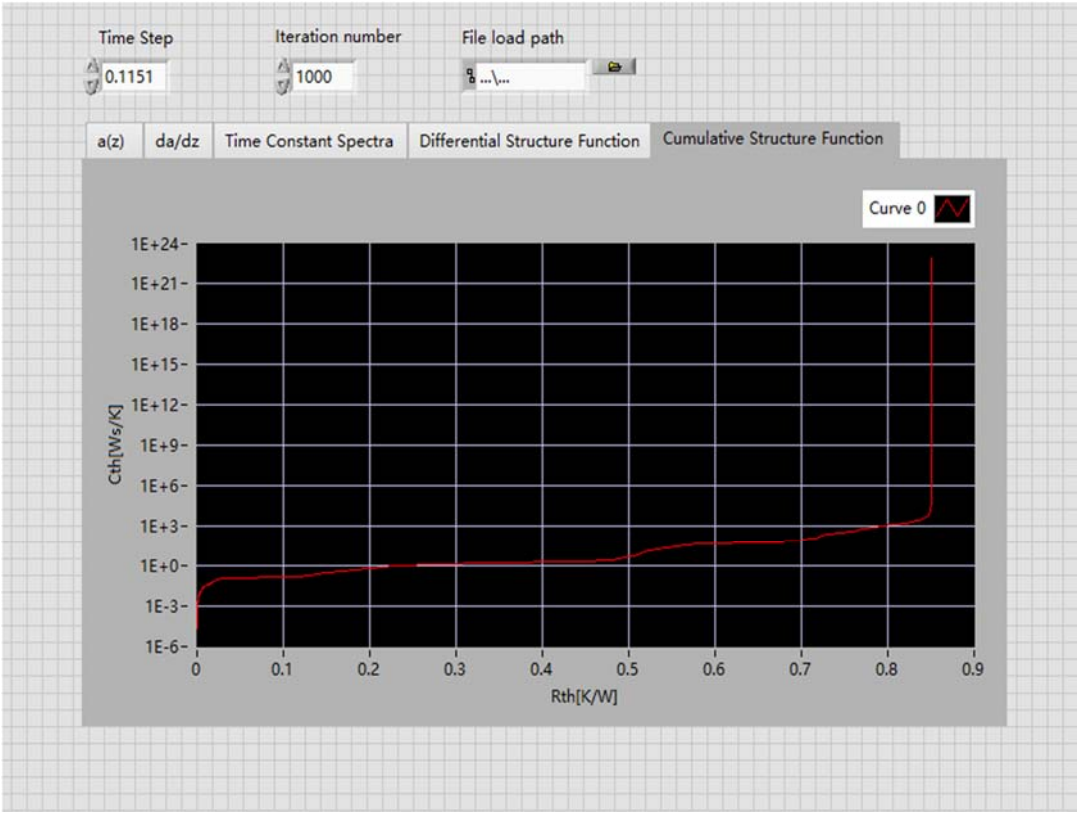


Fig. 7. The proposed software to realize the transient thermal technology.

4. Conclusions

A complete set of software system of the thermal transient testing applied to high-power semiconductor devices is established in this paper based on the research status of thermal transient testing technology at home and abroad. Aiming at the problem of deconvolution algorithm, this paper compares the commonly used deconvolution algorithm to get the conclusion that the Bayesian deconvolution algorithm based on Richardson-Lucy algorithm obtains the most accurate structure function. In response to another key issue: data accuracy in the process of network model conversion, it is proposed to reduce the difficulty of implementing the algorithm by using Mathematica to achieve the same effect as GMP. Finally, taking the actual measured data measured by a mature commercial thermal transient test equipment for power semiconductor devices as an example, the validity and accuracy of the system established in this paper are verified.

Acknowledgements

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Sergey Y. Yurish



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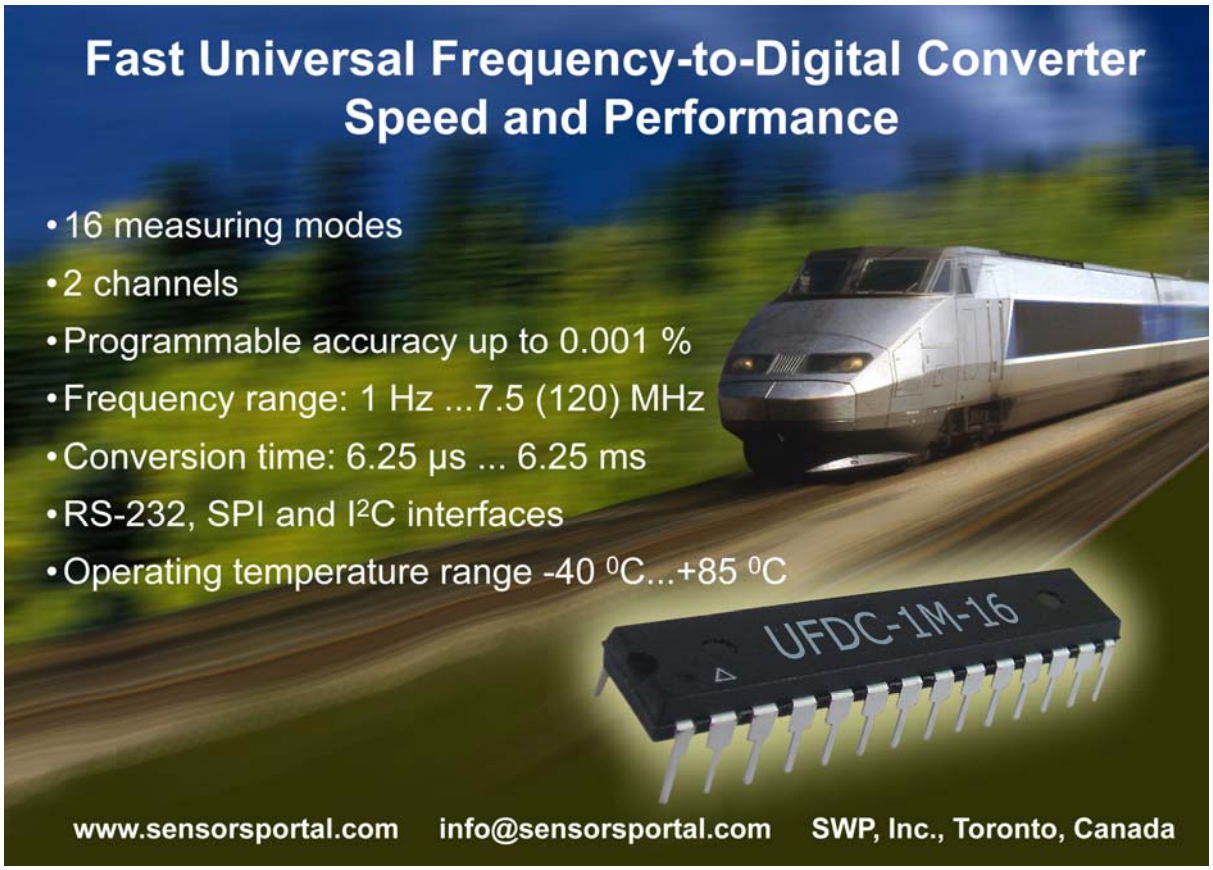
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Power and Area Efficient Intelligent Hardware Design for Water Quality Applications

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Abstract: The paper presents a power efficient and computationally less intensive intelligent hardware using artificial neural network for water quality applications. A compact Hardware Neural Network algorithm has been developed that takes four water quality parameters as the input vector and perform classification of the parameters using a Multilayer Perceptron Network. The computational complexity in the implementation of logistic function has been reduced at a mathematical level by use of approximation methods such as Padé approximation for exponential function and non-linear approximation for sigmoid function. The network improves accuracy of the output by learning by back-propagation of the error. Results show that non-linear approximation method is 34.13 % power efficient and utilizes 15.53 % less number of hardware resources in comparison to Padé. ASIC implementation is compact and has 99 % less power consumption as compared to FPGA implementation of the same algorithm.

Keywords: Artificial Neural network, Activation function, ASIC, Power efficient, Water quality, FPGA, Computational complexity.

1. Introduction

The aim of the paper is to present a power efficient and computationally less intensive intelligent hardware using artificial neural network for water quality applications. The whole system is designed to be power efficient and will be contained in a handheld device which gives an output in a very easily legible way by classifying the water sample being tested into one of the three classes – potable, agricultural and non-usable.

The classifications and the parameters boundaries are taken as per the standards given by the World Health Organisation Drinking Water Quality Standards [1]. A Hardware Neural Network algorithm has been developed that takes four water quality parameters, viz., pH, Oxidation Reduction Potential (ORP), Dissolved Oxygen (DO) and Total Dissolved Solids (TDS) as the input vector and perform classification of the parameters using a Multilayer Perceptron (MLP) Network.

Artificial Neural networks (ANN) have traditionally been implemented using software only or hardware-software co-design approaches for computational simplicity and accuracy [2]. A complete hardware based design, on application specific integrated circuit (ASIC) design approach, involves a trade-off between the accuracy of the calculation vs. the complexity, and power consumption.

A complete hardware based implementation of ANN has been explored by Faiedh, *et al.* [3] using

asynchronous handshaking technique which gives a delayed response. Generally ASIC design approach has proven to be computationally complex but power efficient and area required for design is also reduced drastically as the application specificity of the integrated circuit rules out unnecessary or redundant components from the IC making it suitable for a handheld device. In the present design, both ASIC and field programmable gate array (FPGA) based design methodologies are implemented and performance is compared.

ANNs are most commonly expected to perform one of the four tasks:

- *Classification* of input data sets into predefined classes.

- *Prediction* of future output based on a set of current input-output mappings.

- *Clustering* data into groups based on prior knowledge about the data.

- An ANN can be trained to remember particular data patterns and then *associate* input data pattern with the ones in the memory or discard the data pattern.

An ANN neuron is modelled as:

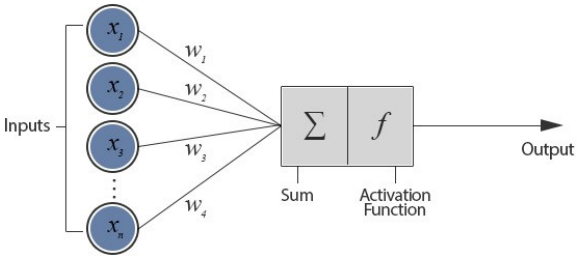


Fig. 1. Model of a neuron of an ANN. Image Source: [4].

The input points on above figure are analogous to synaptic connections on a nerve cell. For an n-dimension input vector [x_1, x_2, x_n] each input is multiplied by a synaptic weight [w_1,w_2, …….w_n]. These products are hereafter summed up in the nerve centre and the final sum is passed through an activation function (a threshold function, stepwise linear function or sigmoid function) that defines the final output of the neuron. A multitude of such neurons form a layer of parallel processing centres which can work on a huge range of inputs. The outputs of one such layer of neurons serves as the input to many such subsequent layers of neurons, thus implementing a huge parallel processing capability to the system. The outputs are then compared with the expected outputs and the errors are measured. The weights of the synapses are thus altered in accordance with the error. This is the basic learning process of a neuron.

Fig. 2 shows a typical architecture for an ANN.

- **Input Layer** – It contains those neurons that receive the input data that is to be processed by the ANN.

- **Hidden Layer(s)** – These are the layers of units between the input and the output layers. The hidden layers take the data from the input layer and perform the computations such that it can give useful information to the other hidden or output layer.

- **Output Layer** – This consists of the neurons or units that give output depending on the learning that has taken place inside the ANN.

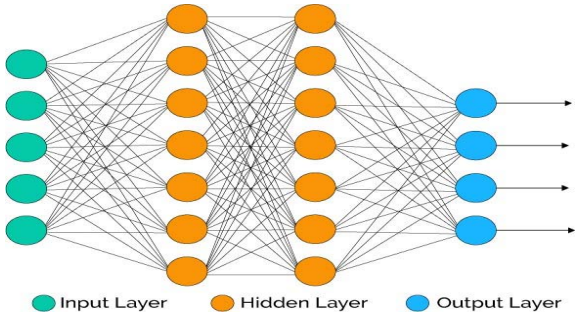


Fig. 2. A typical ANN Architecture; Image Source [13].

2. ANN Implementation

2.1. Software vs. Hardware

Traditionally, ANNs have been implemented on software which requires a complete processing system. That means a lot of unnecessary hardware is engaged but not utilised. Also when the software code has to decode down to a hardware level to be able to interact with the real world, it has to go through multiple abstractions of computer architecture. This renders the process to become time consuming and also limits the usability of the ANN. Thus, an Application Specific Integrated Circuit (ASIC) or System-on-Chip (SoC) based implementation of an ANN algorithm makes the system much more resource and time efficient because of the application specific nature of the hardware. A direct hardware implementation also improves the speed of the system. An application specific IC is also economical because of its specificity.

Hardware implementation of ANN's offer a simpler development cycle for powerful machine intelligence. Application specific nature of these hardware offer better performance, but at the cost of programmability. Moreover, physical resource (Silicon area) utilisation is also minimal in this approach. The trade-off between application specificity and program flexibility is a part and parcel of VLSI design.

While implementing a logic on hardware, there are two approaches: - *Analog and Digital.* Morgan, *et al.* [5] present the key advantages that a digital approach has over analog.

Biological mechanisms which function on inaccurate components serve as models for ANN algorithms. Thus, analog circuits having infinite resolution (continuous sampling) should serve as the better implementation option. Practically though, there is a limit to the representation of the smallest resolution on a circuit. i.e. the sampling rate of a circuit

must be finite. Moreover, a multitude of ANN algorithms model biology very poorly and thus frequently need wide dynamic range to bring about convergence to useful solutions. Popular stochastic algorithms such as backpropagation (BP) require 12 – 16 bit of range or roughly four orders of magnitude between the largest weight value and the smallest weight change [6-7]. Resolution required to achieve convergence cannot be obtained from analog circuits [5].

Calculation of functions can be done by device physics by clever analog designing, but these designs are more dependent on circuit size than scalable CMOS (Complementary Metal Oxide Semiconductor) digital designs. Particularly, thermal noise power can be assumed to be proportional to inverse of the length unit (λ). Thus, for very small circuits the noise levels can be very high and render the circuit unreliable. Hence, as circuits sizes decrease, digital approach offers better prospects for performance improvement.

Connectivity between elements on a chip is a big limitation. Particularly, for ANN's, they require huge multiplexing. Multiplexing analog signals is a design and resource intensive process. Interconnecting analog circuits at board level is pretty tricky because of radiated noise, power supply isolation problems, crosstalk, etc. Digital connections, on the other hand, tend to be rather reliable, comparatively. Since, a neural network generally consists of more than one neuron, crosstalk needs special consideration when implementing computational multiplexing. Digital circuitry demands more Silicon area.

When implementing changes in algorithm, analog circuit requires major redesign efforts. Digital circuits can accommodate such changes by implementing a different logic array.

Since most other computational units are digital, nowadays. A digital circuit also improves compatibility to other systems, as compared to an analog circuit. Also ANN's are subject to Amdahl's Law[1], as per which, the speed improvements of an analog neuron will stay untapped if the remaining network is implemented by slower digital implementations.

2.2. ANN Architectures

On most neural networks, each neuron in a hidden layer is connected to each unit in the previous (input) layer and the subsequent (output) layers. ANNs can be implemented in a number of architectures. In 1943, McCulloch and Pitts presented the first ever model of an artificial neuron, called the perceptron [8]. A layer of perceptrons can perform some tasks. Thus a single layer of perceptrons can form a network. We term such a network as a Single Layer Perceptron. An arrangement of a series of a Single Layer Perceptron is called a Multi-Layer Perceptron (MLP). MLPs are also called feedforward networks.

2.3. Activation Function Design

The most computationally complex part in hardware implementation of an ANN is the implementation of the activation function as it involves complex non-linear mathematical calculations.

Various techniques have been used in proposed ANN design to cut down on computational complexity in order to achieve less power consumption. Accuracy is improved by the learning cycle of the network.

The computational complexity in the implementation of logistic function has been reduced at a mathematical level by use of approximation methods such as Padé approximation for exponential function and non-linear approximation for sigmoid function.

(1) In first method, we use logistic activation function Eq. (1) as the activation function implemented using IEEE 754 floating point representation for Multi-Layer Perceptron architecture.

$$y = \frac{1}{1 + e^{-x}} \tag{1}$$

Padé approximation Eq. (2), as proposed by ZbigniewHajduk's [9] work has given fairly accurate network outputs despite compromising marginally on mathematical accuracy as compared to other expansions such as Taylor series or McLaurin series. However, the Padé approximation for exponential function is valid only for the input values lying in the interval $0 \leq x \leq 1$.

$$e^x = \frac{1680 + 840x + 180x^2 + 20x^3 + x^4}{1680 - 840x + 180x^2 - 20x^3 + x^4} \tag{2}$$

This limits the application of the approximation for our project. Fig. 3, shows schematic diagram for Padé approximation using Look up table (LUT) blocks of Xilinx Zynq700 board.

(2) In second method, we implement an approximation of the Sigmoid function as proposed by Zhenzhen Xi [10]. Herein, a Look up table (LUT) based approach is followed, which is particularly suited for FPGA implementation of the sigmoid function. The total domain of the sigmoid function is broken up into shorter intervals and the curve in those intervals is approximated by curve fitting method to simpler polynomials. For our application, since we normalise the input values in the range of [-1, 1], hence, we take up the intervals [-2, -1], (-1, 1)

[1]Amdahl's Law – The performance gain of a faster execution mode is limited to the time for which the execution mode is being used.

and [1, 2). The polynomials for the said intervals are given Eq. (3), Eq. (4) and Eq. (5), respectively:

$$y = 0.0467 * x^2 + 0.1239 * x + 0.2969 \quad (3)$$

$$y = 0.2383 * x + 0.5 \quad (4)$$

$$y = -0.0467 * x^2 + 0.2896 * x + 0.4882 \quad (5)$$

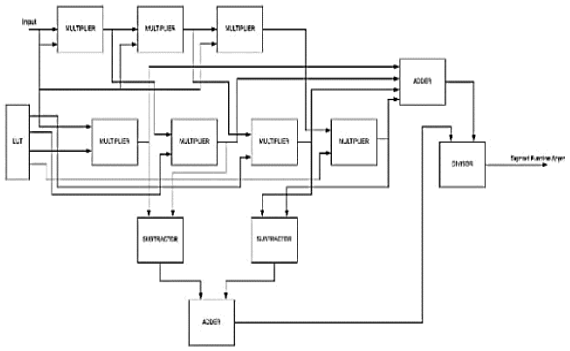


Fig. 3. Schematic Diagram of neuron using Padé Approximation.

Fig. 4 above shows schematic diagram for Non-linear approximation using the LUT blocks of a Xilinx Zynq 7000 series board.

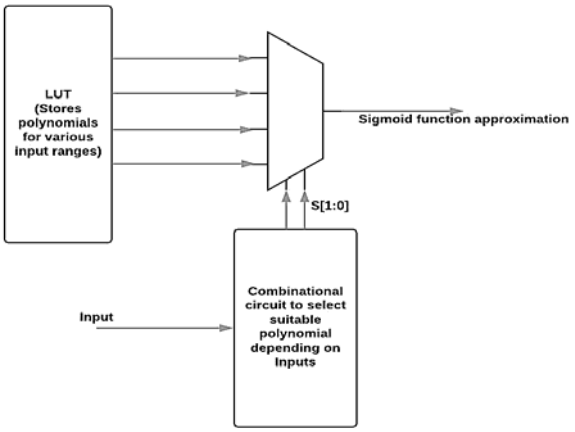


Fig. 4. Schematic diagram of for nonlinear approximation.

2.4. Learning Algorithm

The learning algorithm for this network is chosen to be backpropagation. As propounded by Rumelhart, *et al.* [11], the aim of backpropagation is to obtain a set of weights so as to minimise the difference between the desired output and the actual output of each neuron, given a particular input vector. The total error E is given by:

$$E = \frac{1}{2}\sum_c \sum_j (y_{j,c} - d_{j,c})^2, \quad (6)$$

where c indicates the case (input-output pair), and j indicates the output unit, y is the actual state of the output unit while d is the desired state of that output unit. The partial derivative of E with respect to each weight in the network is computed to minimise the error using gradient descent algorithm. The partial derivative is simply the sum of the partial derivatives of each case. Thus, we calculate $\partial E/\partial y$ for each case:

$$\frac{\partial E}{\partial y_j} = y_j - d_j \quad (7)$$

Applying chain rule to compute $/\partial x_j$:

$$\frac{\partial E}{\partial x_j} = \frac{\partial E}{\partial y_j} \cdot \frac{dy_j}{dx_j} \quad (8)$$

Differentiating equation (1) for dy_j/dx_j we get:

$$\frac{\partial E}{\partial x_j} = \frac{\partial E}{\partial y_j} \cdot y_j(1 - y_j) \quad (9)$$

The total input is a linear function of the states of the previous levels and also a linear function of the weights on the connections. Hence, it becomes easy to compute how the error is affected by a change in the state and the weights. Given a weight w_{ji}, from i to j the derivative is given as:

$$\frac{\partial E}{\partial w_{ji}} = \frac{\partial E}{\partial x_j} \cdot \frac{\partial x_j}{\partial w_{ji}} = \partial E/\partial x_j \cdot y_i \quad (10)$$

And the contribution of $\partial E/\partial y_i$ for the i^{th} output unit because of the effect of i on j is:

$$\frac{\partial E}{\partial x_j} \cdot \frac{\partial x_j}{\partial y_i} = \partial E/x_j \cdot w_{ji} \quad (11)$$

Considering all the synapses emanating from i, we get:

$$\frac{\partial E}{\partial y_i} = \sum_j \frac{\partial E}{x_j} \cdot w_{ji} \quad (12)$$

So now we have the $\partial E/\partial y$ for a unit in penultimate layer, given the $\partial E/\partial y$ for all the output neurons. To compute this term for previous layers, weuse the same principle successively while computing $\partial E/\partial w$ for the weights.

$\partial E/\partial w$ is used to change the weights in every epoch. The $\partial E/\partial w$ over the network are accumulated and then at the end of the epoch, we change the weights of each neuron by an amount proportional to the accumulated $\partial E/\partial w$:

$$\Delta w = -\varepsilon \partial E/\partial w \quad (13)$$

As stated by Rumelhart, the method has a low convergence rate as compared to methods that make use of second derivative but it is easy to implement on parallel hardware. The method is improvised by accelerating method where current gradient modifies

the velocity of the point in weight space instead of its position:

$$\Delta w(t) = -\frac{\varepsilon \partial E}{\partial w(t)} + \alpha \Delta w(t-1) \qquad (14)$$

where t denotes the time-step or epoch and α denotes an exponential decay factor between 0 and 1 that controls contribution of current and previous gradients to the change in weights. Thus, α is also called the learning index.

3. Power Efficiency and Accuracy

The dynamic power consumption of a single neuron is reduced by replacing sequential units like counters and MAC units by parallel multipliers and adders that perform the calculation in parallel. This also reduces the requirement of storage elements within each neuron.

The network improves accuracy of the output by learning by back-propagation of the error. As the final output of one epoch is generated, an FSM is designed that would generate a signal to start a back-propagation algorithm [12]. This algorithm measures the difference between the desired output and the actual output. The error in the final output is back propagated to all the neurons in the preceding layer while the weights of the current layer are updated. The control of the learning mechanism being synchronised using an FSM gives a time multiplexing to the learning mechanism so as to reduce switching power consumption of the complete network.

4. Results and Comparison

The algorithms have been coded in Verilog and implemented on ZynQ7000 FPGA using Xilinx Vivado. The results of the implementation are shown in Table 1.

Table 1. Comparison of two implementations of Activation Function in FPGA based design.

Implemen-tation	MUX	LUT	DSP	Power (FPGA) (Watts)	Power (ASIC) (Watts)
Padé approximation	15	3578	18	5.95	3.75×10^{-4}
Non-linear approximation	14	3144	12	5.3	2.47×10^{-4}

The power consumption of the FPGA implementation were very high. Thus, we synthesized the design using ASIC design methodology. The ASIC was synthesized using Cadence Encounter RTL Compiler tool with UMC 90 nm standard cell library. The power consumption of a neuron using Padé approximation dropped from **5.95 Watts on FPGA to 3.75×10^{-4} Watts in ASIC synthesis**. Similarly for the Non-linear approximation method the power consumption of a single neuron drops from **5.3 Watts on FPGA to 2.47×10^{-4} Watts for ASIC synthesis.**

Padé approximation method makes use of 25538 Cells covering 241897 nm^2 of the library as compared to 21571 cells covering 196997 nm^2 for nonlinear approximation method.

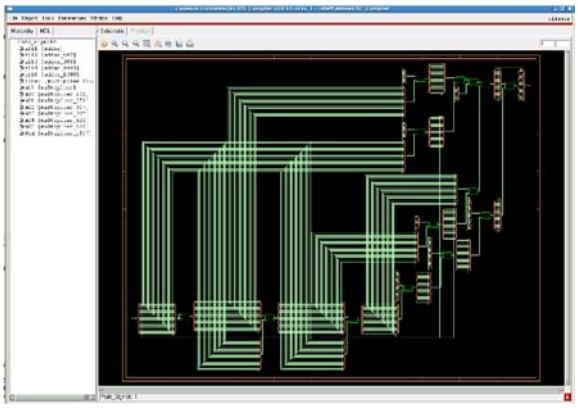


Fig. 5. ASIC implementation of Padé approximation.

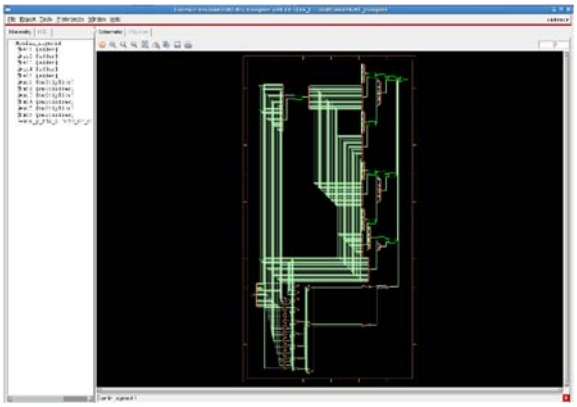


Fig. 6. ASIC Implementation of a Nonlinear Approximation of Sigmoid function.

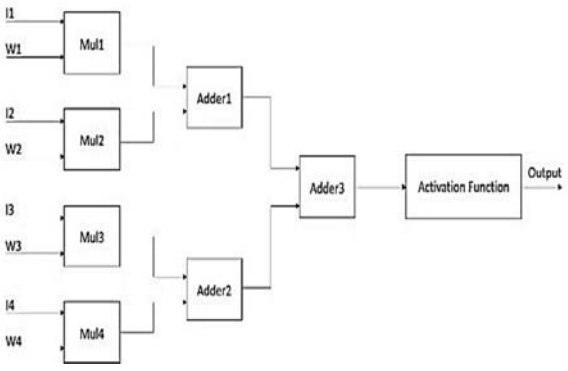


Fig. 7. Basic structure of a Neuron.

5. Conclusions

From the results shown in Table 1, non-linear approximation method is found to be more suited to proposed design for water quality application. It also is much more power efficient and utilises much less number of hardware resources. However, FPGA implementations are consuming much higher power. Thus we have changed to a compact ASIC implementation of the network designed. The ASIC implementation shows drastic drops in power consumption of the system as compared to FPGA implementation.

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Design and Evaluation of a Low-Cost and Flexible Data Acquisition System Using Sensor Network for Smart Homes

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Abstract: This research paper presents the design and performance evaluation of a low-cost and flexible data acquisition system using sensor network. This work, is an extension of our previous conference paper [24]. The study considers three important parameters for performance evaluation. Namely, temperature, humidity and light. Proteus and Arduino integrated design environment is used to build a complete sensor network. A real working prototype was designed and implemented. Experimental procedure includes building the hardware architecture of the transmitting nodes, modeling both the communication channels and the receiving master node. A low-cost digital-output relative humidity and temperature, and light dependent-resistor sensors were used for the data acquisition system. The values of the sensed parameters are stored on a secure digital card mounted on the Arduino board which served as the base station. Experimental (case study) results are obtained from the implemented prototype by taking the readings of the sensors stored on the secure digital card under various conditions and numerous results were collected to demonstrate the efficiency and flexibility of the proposed approach. The proposed approach, will assist the smart-home owners to be kept abreast of their environmental condition and equally know what changes would likely to happen. The implemented prototype can be deployed in smart-homes, remote monitoring and healthcare applications.

Keywords: Sensor network (SN), Data acquisition system (DAQ), Performance evaluation, Smart-homes, Light dependent resistor (LDR) sensor, Digital-output relative humidity and temperature (DHT22) sensor, Secure digital (SD) card.

1. Introduction

This study considers the design of a low-cost and flexible sensor network architecture for data acquisition system (DAQ), and provide a performance evaluation of the proposed system. The performance evaluation was based on three parameters, namely, Temperature, Humidity and Light. The readings of these parameters are stored as a text file in a media memory card (SD Card) and a real time clock will display date and time those parameters are sensed. The sensors with such capabilities are the light dependent resistor (LDR) and digital-output relative humidity and temperature (DHT22) sensors. DHT22 sensor senses both temperature and humidity, while the light dependent resistor-sensor, senses light (Lumina). These components are soldered on a Vero Board together with other digital components that made up the circuit. The fabricated device, is powered by battery to enable the sensors to work perfectly.

The data acquisition systems have emerged over some years from electromechanical recorders with few channels to electronic devices possessing the capabilities of measuring hundreds of parameters simultaneously. The most commonly used data acquisition systems make use of magnetic tape and recorders to record the signals. However, with the advent of new technology, the amount of data and the speed and time of collection increases dramatically. Therefore, there is the need to have a sophisticated device that can measure environmental parameters in real-time for making an informed decision. The computer-based data acquisition system, should possess the capabilities of recording extremely accurate, repeatable, and reliable and error free data, based on the design specifications and consideration [1].

In order to achieve these design specifications and considerations, the data acquisition system should include: selecting the correct sensors for the target application; the choice of proper wire and shielded cable; signal capturing in proper magnitude; signal and frequency ranging; proper grounding and shielding to avoid loops. In addition, the choice of correct impedance and double ended differential inputs is essential. The smart environment in which the device will be used should also be considered, especially for extremes of ambient temperature, humidity and light Lumina [2]. Therefore, the major goal of this research paper is to notify the smart-home users of the changes in the environmental parameters for informed decision making and the most needed recommended practices for smart cities.

The state-of-the-art sensor fusion technique in embedded mobile devices was provided by the authors in [3]. The approach is aimed to assist the mobile device users to identify their daily activities using mobile phones. The sensor fusion techniques are used to aggregate data collected from several sensors to enhance reliability in identifying different activities of the mobile phone users. In this regard, the mobile devices to monitor the user's activities have certain drawbacks, these include: low memory; low battery life and low processing capabilities. And this affects most sensor fusion techniques.

A static calibration and analysis of the Velodyne HDL-64E S2 scanning LiDAR system was demonstrated by the author's work in [4]. The work provided a mathematical model for measurements of the HDL-64E S2 scanner. In order to provide an optimal solution for the laser's internal calibration parameters, a planar feature based least squares adjustment method was demonstrated in a minimally constrained network. The proposed approach, provided a threefold enhancement in the planar misclosure residual over the standard factory calibration model.

The study of parameter selection for data sampling frequency and segmentation techniques and their effect on classification accuracy was studied. The study provided the empirical investigation of different data sampling rates, segmentation techniques and segmentation window sizes and how they affect the accuracy of activity of daily living event classification. In addition, the study presents the effect of computational load for two different accelerometer-sensor datasets [5].

Advances in heterogeneous communication technologies have enabled sensors to be used in smart cities, things or objects interact with each other while ensuring good network connectivity. However, the existing technologies cannot provide an efficient data acquisition mechanism for flawless and error prone connectivity in smart cities due to the presence of many sensing devices which generates several problems [6-8].

A low-cost microcontroller-based data acquisition device was provided by the authors in [9]. The design consists of a configurable microcontroller-based device with an embedded universal serial bus (USB) transceiver, and a 12-bit analogue-to-digital converter. The embedded DAQ device, is preloaded with a firmware program that allows easy data acquisition and generation of analogue and digital signals. The device, also has the capability of data transfer between the device and the application program running on a personal computer through the use of universal serial bus.

The monitoring of cultural heritage in the context of smart cities was provided by the authors in [10]. The idea is to perform future comparative studies and upload the gathered information into the cloud that will be useful for the conservation of other heritage sites.

The study of the side effect of heterogeneous DAQ hardware was carried out by the authors in [11]. The major challenge is the lack of an accurate synchronization between samples captured by each device. A low-cost hardware modular DAQ architecture consisting of a baseboard and a set of substitutable modules was presented. However, the system is not efficient enough to solve the presence DAQ requirement. Therefore, a design, implementation and performance evaluation of wireless sensor networks for data acquisition system is very essential.

The fundamental objectives of this study are: low-cost architecture, time saving; flexibility of sensor nodes; quick access to data; accuracy; reliability; data integrity, and ease of deployment.

This study will be of immense importance not just to those who use sensor networks for data acquisition (smart-home owners) but also to those who in one way or the other, the result will play a key role in their livelihood. The implemented prototype will go a long way in making a performance evaluation of data acquisition system through sensor networks for monitoring temperature, humidity and light in smart-homes much easier.

The rest of the paper is organized as follows: Section 2 presents the related literature; Section 3 discusses system architecture and design methodology; Section 4 discusses the system simulation methodology; Section 5 discusses

experimental results, case study and performance evaluation; Section 6 provides concluding remarks and plans for future enhancements.

2. Related Work

The work of the authors in [1] discusses the state-of-the-art sensor fusion technique in embedded mobile devices. This approach was aimed to assist the mobile device users to identify their daily activities using mobile phones. The sensor fusion techniques are used to aggregate data collected from several sensors to enhance reliability in identifying different activities of the mobile phone users. Though, the mobile devices to monitor the user's activities have certain drawbacks, these include: low memory, low battery life and low processing capabilities. And this affects most sensor fusion techniques. The author's objective is to present an overview of the state-of-the-art to identify instances of sensor data fusion techniques that are used in mobile devices to track the daily activities of mobile phone users.

In the research work by the authors in [2], a static calibration and analysis of the Velodyne HDL-64E S2 scanning LiDAR system was demonstrated. The work provided a mathematical model for measurements of the HDL-64E S2 scanner. In order to provide an optimal solution for the laser's internal calibration parameters, a planar feature based least squares adjustment method was provided in a minimally constrained network. The work provided the results of the adjustment along with a detailed evaluation of the adjustment residuals. The proposed approach, provided a threefold enhancement in the planar misclosure residual RMSE over the standard factory calibration model. Furthermore, the measurements from the scanner indicated that unmodelled distortions may still be existed in the range measurement. Nevertheless, despite the presence of measurement distortions in the measurements, the whole precision of the adjusted laser scanner data proved to be a practical choice for high accuracy mobile scanning applications.

The authors in [3] study the parameter selection for data sampling frequency and segmentation techniques and their effect on classification accuracy. The authors presented the empirical investigation of different data sampling rates, segmentation techniques and segmentation window sizes and how they affect the accuracy of the activity of daily living. In addition, how they affect the event classification and computational load for two different accelerometer sensor datasets. The authors presented results and recommendations for the choice of the best combination of parameters that are identified based on the equivalent Pareto curve.

The work of the authors in [4] provided a low-cost microcontroller-based data acquisition device. The major components of the device consist of a configurable microcontroller-based device with an embedded USB transceiver and a 12-bit analogue-to-digital converter. The embedded DAQ device, is preloaded with a firmware program that allows easy data acquisition and generation of analogue and digital signals. It also has the capabilities of data transfer between the device and the application program running on a personal computer through the use of universal serial bus. Furthermore, the authors presented the LabVIEW drivers for the fabricated device.

The authors in [5] propose monitoring of cultural heritage in the context of smart cities. The idea is to perform future comparative studies and upload the gathered information into the cloud that will be useful for the conservation of other heritage sites. The authors presented the development of an economical and appropriate data acquisition system which integrate wired and wireless communication, and third-party hardware tools for increased versatility of the designed system. The proposed device provided the capability of monitoring a complex network of points with high sampling frequency. The device used a wired sensor in a 1-wire bus and a wireless centralized data recording system and monitoring of physical parameters. Furthermore, it is envisaged that the device, will possess the future capability of attaching an alarm system or sending data over the Internet. The development of three board design and over five thousand algorithm lines of codes, demonstrated the efficiency of the proposed system.

The work of the authors in [6], study the side effect of heterogeneous DAQ hardware. The major problem is the lack of an accurate synchronization between samples captured by each device. In order to provide a solution to this problem, the authors proposed a low-cost hardware modular DAQ architecture consisting of a baseboard and a set of substitutable modules. The main objective is the ability to sample all data sources at predictable, fixed sampling frequencies, with a reduced synchronization mismatch of less than one second between heterogeneous signal sources. Experimental results were presented, demonstrating vibration spectrum analyses from piezoelectric accelerometers and a spectrum of quadrature encoder signals. Other approaches are given by the work of the respective authors in the literature [12-17].

3. System Architecture and Design

Fig. 1 illustrates the block diagram of a real-time device monitoring system. Once connection is established, the DHT22 and a light dependent resistor (LDR) sensors will verify the established connection and start reading the temperature, humidity and light Lumina, and the processed data or information is displayed by the LCD through the user interface window. Then, a real-time clock (RTC) module is accessed through I2C interface to obtain the current date and time. The SD card is accessed via SPI interface and a new data log file is created. If the file already exists, the new data will be written with its new date and time stamp beneath the existed data

inside the file. The two sensors will automatically start taking measurements of the indicated parameters, temperature, humidity and light [15-18].

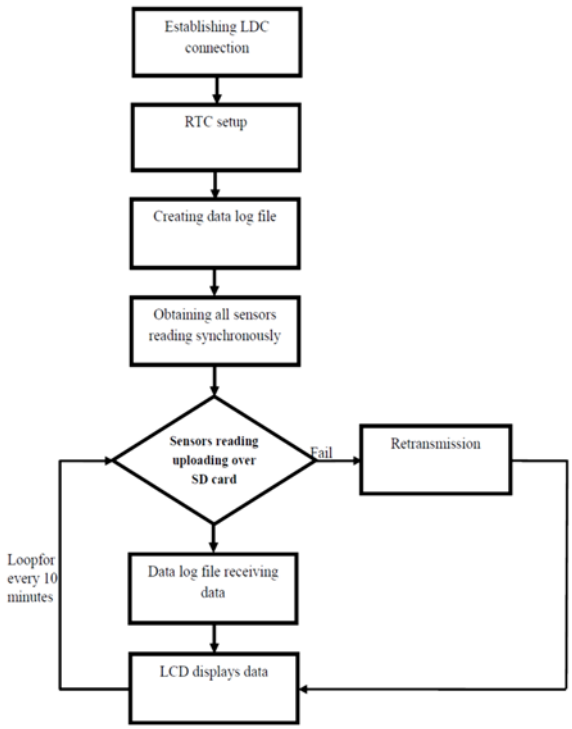


Fig. 1. Real time device monitoring system flow.

Fig. 2 shows the system architecture. The architecture consists of three input parameters, namely, temperature, humidity and light. The real-time clock module provides an input real-time clock signal to the ADC. The output of the ADC is transmitted to the microcontroller unit for processing. The microcontroller will then, process the sensor data and transmits the processed data to the LCD for display and to the secure data (SD) card for storage. The electrically erasable programmable read-only memory (EEPROM) serves as an on-chip memory for the microcontroller. All electronics operations are controlled by a single microcontroller unit, which is programmed based on how other peripherals components of the system will behave.

This device architecture, consists of two sensors; namely, temperature and humidity (integrated into a single module), and Light (LDR). The temperature and humidity sensors are responsible for detecting ambient environmental changes [19-21].

The LDR sensor is used to detect the Lumina (brightness) of light. The sensor's data readings are registered in the microcontroller unit along with date and time stamp synchronously. The data is then be uploaded over into the data log file monitoring database to provide the smart-home users with the real time data [22-23].

Fig. 3 illustrates the fabricated device prototype. The casing fabrication was done with plastic, and carefully engineered. The casing is portable like a small box which can be hand held and can be carried about easily.

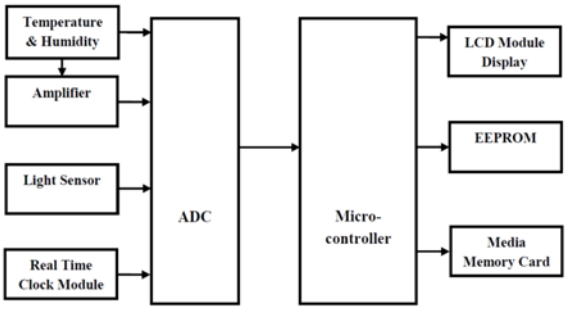


Fig. 2. System Architecture.



Fig. 3. The fabricated device's prototyp.

4. System Simulation

Herein, the procedure to simulate the sensor network for data acquisition system is provided. In order to demonstrate the concepts of the data acquisition using simulation methodology, a complete SN model was built as shown in Fig. 4 and Fig. 5. This network consists of three sensors serving as communication nodes (i.e. slave nodes) sending their measured data samples to a master node (SD card). Other components of the system are: real time clock; media memory card (MMC); liquid crystal display, virtual terminal and many other devices that are integrated to form the complete system. In addition, two power supply sources are provided [24].

The design of the sensor network for the data acquisition system is simulated using the Proteus 8.5 design suite, Arduino Uno integrated development environment (IDE), and embedded C programming language. Proteus 8.5 professional is an efficient tool and a high-performance design environment for simulating technical computing. The package integrates computation and virtual representation of the systematic operation of the system and shows how the prototype system components will operate. Arduino as the development board provides a user-friendly design environment IDE where embedded C source codes can be written, verified, and uploaded to the microcontroller unit [25].

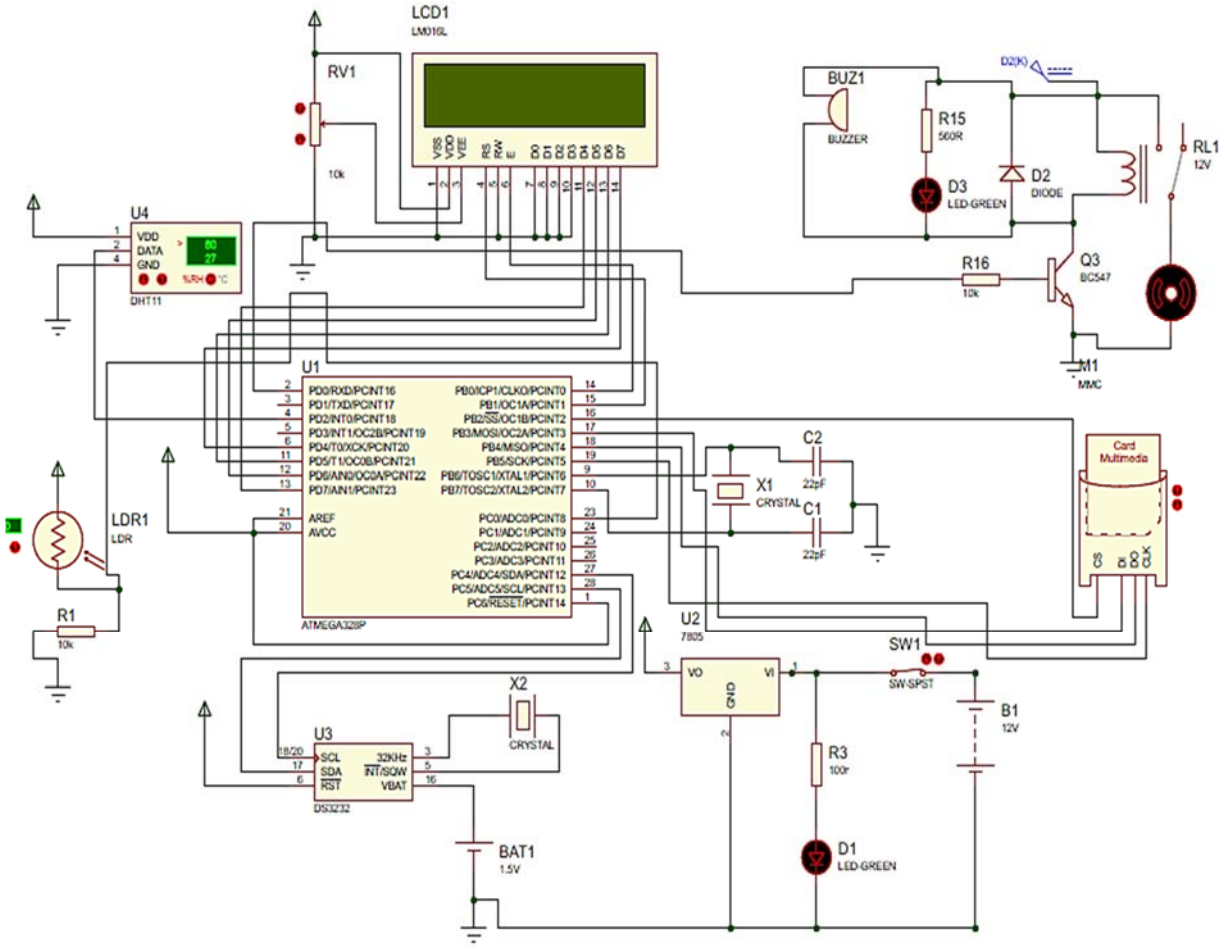


Fig. 4. The system simulation.

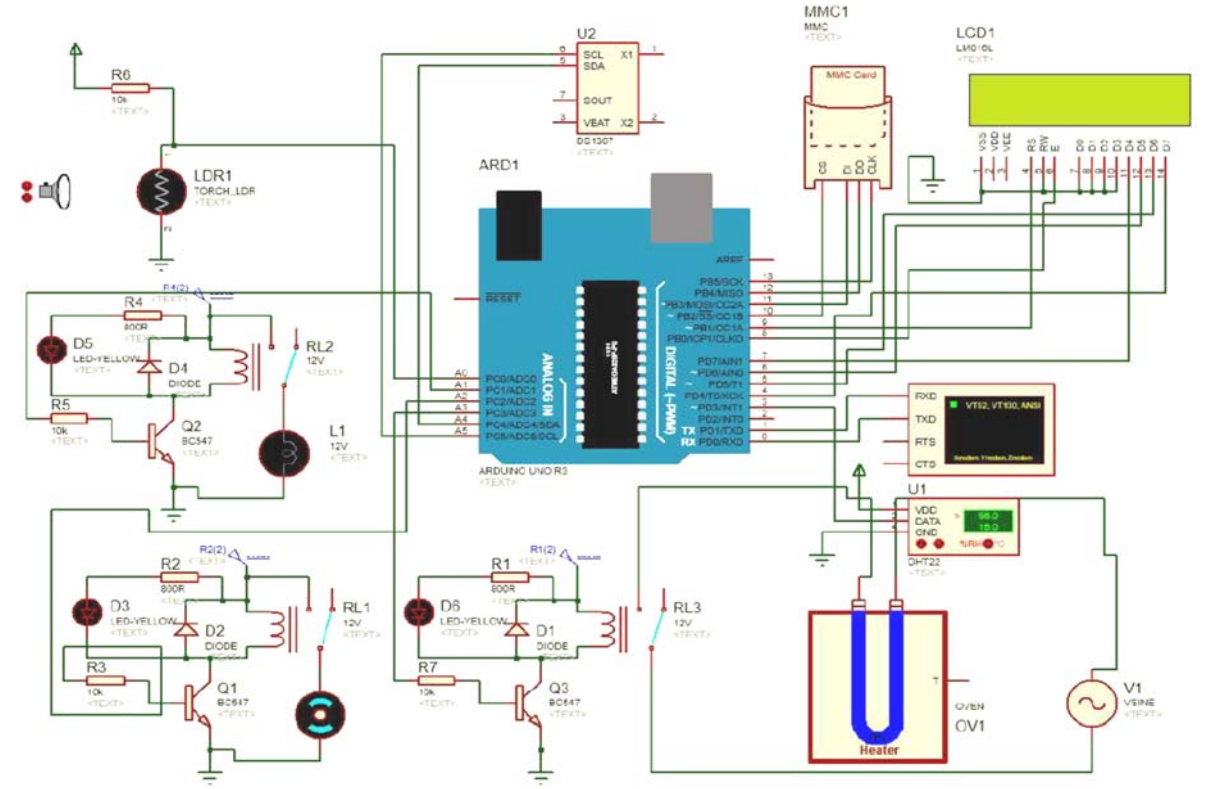


Fig. 5. The system simulation.

The design of the sensor network makes use of an Arduino board. Arduino is an open-source electronics platform that provides easy hardware / software co-design tools for designing embedded applications. Embedded C programming language is suitable for the design of embedded systems and sensor components. The codes written in embedded C language allow the circuit or devices to achieve their optimal performance. In addition, it has a failure rate less than one percent when developed to interact with the hardware components. These features of the embedded C language are employed and used to provide a low-cost, flexible and highly efficient DAQ system for measuring ambient environmental changes for smart-home owners [26].

5. Experimental Results (Case Study)

The experiment was conducted using the fabricated device prototype. A case study of a smart-home was chosen and the device was run for 52 hours and 30 minutes continuously. The three sensor measurements are captured, stored and processed.

5.1. Sensor Data Logging

Fig. 6 and Fig. 7, illustrates the data logged by the three sensors. Each sensor sends its captured data to the microcontroller. The microcontroller, processes the data and sends it to the receiver (SD card) base station and to the LCD display unit for user information. In addition, the processed sensor data is sent to a serial terminal emulator and logged to a data file. The saved data can be opened with any text editor for further analysis. Here data logging of temperature, light and humidity with their appending date and time is shown in a serial terminal emulator as shown in Fig. 6 and Fig. 7.

Data Acquisition System using Sensor Network for Smart-home Users

----------Sensors Data Logging----------

Date	Time	temp (C)	Light (Lum)	Humidity (%)
2017/9/19	8:8:5	27.50	5336.3	62.0
2017/9/19	8:8:13	27.60	5775.7	61.5
2017/9/19	8:8:22	27.90	5783.9	58.6
2017/9/19	8:8:30	28.50	5515.3	56.7
2017/9/19	8:8:38	28.40	5564.1	55.5
2017/9/19	8:8:47	28.20	5572.3	54.7
2017/9/19	8:8:55	28.10	5458.3	54.6
2017/9/19	8:10:0	29.30	5783.9	51.1
2017/9/19	8:10:8	29.40	5783.9	50.3
2017/9/19	8:10:17	29.60	5775.7	49.7
2017/9/19	8:10:25	29.80	5783.9	49.0
2017/9/19	8:10:33	29.90	5783.9	48.4
2017/9/19	8:10:42	30.10	5783.9	47.8
2017/9/19	8:10:50	30.20	5783.9	46.8
2017/9/19	8:10:58	30.40	5783.9	45.8

Fig. 6. Data logging of temperature, light and humidity sensors (scene 1).

Date	Time	temp (C)	Light (Lum)	Humidity (%)
2017/9/19	8:12:4	31.60	5783.9	41.9
2017/9/19	8:12:12	31.60	5783.9	41.4
2017/9/19	8:12:20	31.80	5783.9	40.9
2017/9/19	8:12:29	31.90	5783.9	40.4
2017/9/19	8:12:37	32.10	5783.9	40.6
2017/9/19	8:12:45	32.20	5783.9	40.0
2017/9/19	8:12:54	32.30	5783.9	39.7
2017/9/19	8:14:5	33.30	5783.9	37.6
2017/9/19	8:14:13	33.30	5783.9	37.3
2017/9/19	8:14:22	33.50	5783.9	36.9
2017/9/19	8:14:30	33.50	5783.9	36.4
2017/9/19	8:14:38	33.60	5783.9	36.1
2017/9/19	8:14:47	33.70	5783.9	35.7
2017/9/19	8:14:55	33.80	5783.9	35.6
2017/9/19	8:16:0	34.50	5783.9	34.1
2017/9/19	8:16:8	34.50	5783.9	34.0
2017/9/19	8:16:17	34.60	5783.9	33.8
2017/9/19	8:16:25	34.80	5783.9	33.5
2017/9/19	8:16:33	34.80	5783.9	33.1
2017/9/19	8:16:42	34.90	5783.9	32.9
2017/9/19	8:16:50	34.90	5783.9	32.7
2017/9/19	8:16:58	35.00	5783.9	32.8

Fig. 7. Data logging of temperature, light and humidity sensors (scene 2).

5.2. Performance Evaluation

The performance evaluation of the three sensor readings is illustrated in Fig. 8 to Fig. 10. Fig. 8 illustrates the temperature sensor readings against time of a smart- home as a case study. There are three scenarios namely, morning, afternoon and night as indicated in the figure. And each scenario is boarded with a vertical gold, black and thick red dotted lines for easy understanding.

The temperature reading samples were taken once for every 30 minutes. The measurements ran for over 104 samples, and the device had been running for 52 hours and 30 minutes continuously. The temperature reading shows 37 ˚C max and 25 ˚C min, while the temperature during the morning of the first day, obviously dropped by 12 ˚C, and constantly swings between 27 ˚C and 37 ˚C during the morning and drastically dropped during the night.

Fig. 9 shows the light sensing result, that is, the light Lumina. As can be observed, the light senor's reading is very high during the daylight (morning) and very low at night. During the daytime, the Lumina varies depending on the atmospheric weather condition either cloudy or sunny. This variation ranges between 3480 to 5710 Lumina, and we can also observe a significant drop in the light sensor's reading, especially, at sunsets (night) to be between 1609 to 1999 Lumina. However, we can observe that where the Lumina reading goes low during the daytime, it shows that the doors and the windows of the smart-home were closed / locked by the owners. Similarly, where the Lumina reading goes up during the night time, it is an indication that there was a light flashing either from electric bulb or nearby automobile cars.

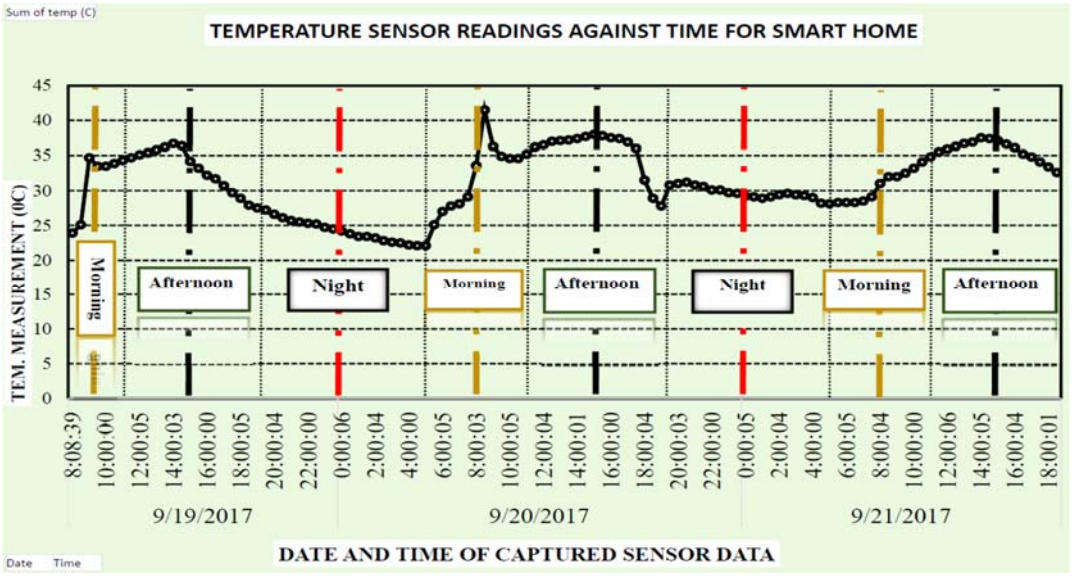


Fig. 8. Temperature sensor readings against time for smart-home.

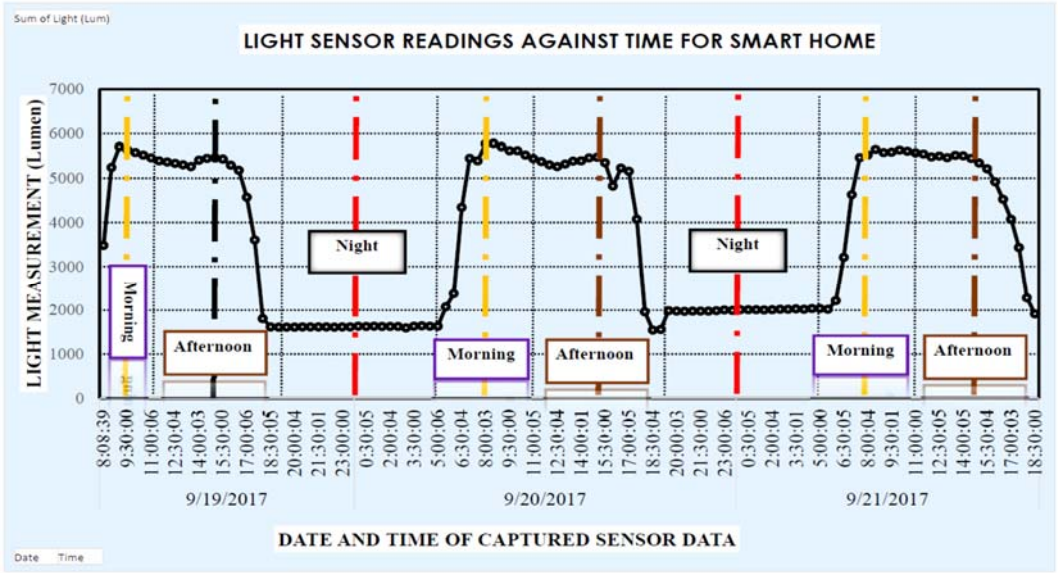


Fig. 9. Light sensor readings against time for smart-home.

Fig. 10 illustrates the humidity sensor readings for smart-homes. As can be observed, the humidity readings are higher during the night most especially the day that it rained and lower during a normal day. It can also be observed that during the night, the humidity sensor measurements varies in the ranges of 44 to 85. However, humidity measurements dropped to 22 and varies in the ranges of 22 to 85.

These results demonstrate the efficiency and reliability of the fabricated device prototype and its application to smart-homes. The device will be of immense importance to the smart-home owners to be kept abreast of their environmental condition and equally know what changes are likely to happen and when. The performance of the proposed system is reliable in terms of captured data, speed, accuracy, integrity and capacity in its storage as demonstrated in the experimental results. The fabricated device prototype can be deployed in smart-homes, remote monitoring and healthcare application.

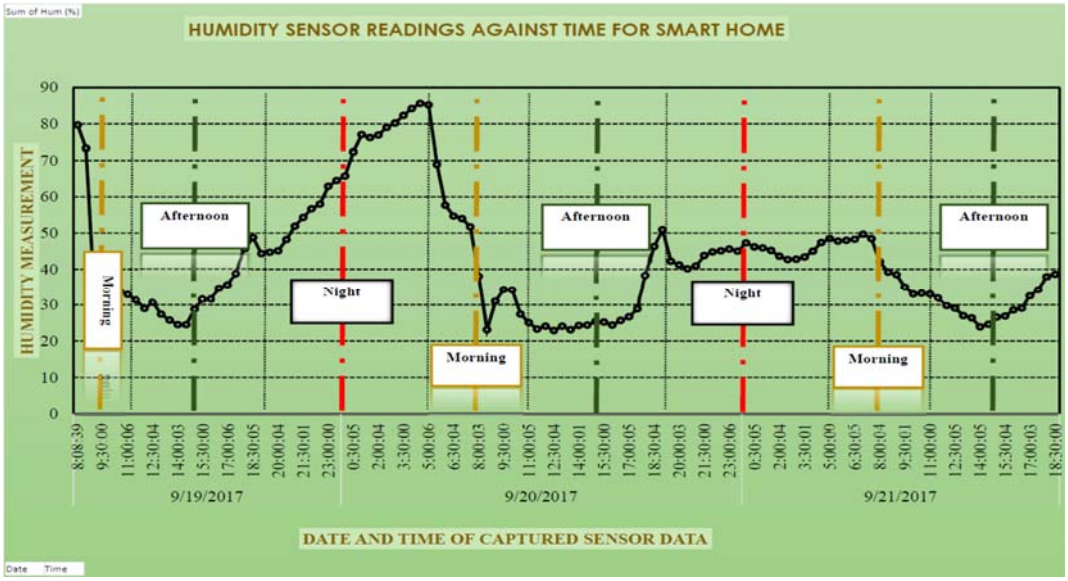


Fig. 10. Humidity sensor readings against time for smart-home.

6. Conclusion and Future Work

This research paper used the capabilities of two sensors with three parameters for the data acquisition system. The sensors include: DHT22 used for measuring temperature and humidity, and a light dependent resistor (LDR) used for measuring light Lumina. The real time clock (RTC) module was used for capturing date and time stamp of the sensed parameters to record their actual readings. The media memory card (MMC) was used as the main base station for the storage of the sensor data. The methodology used in this paper is the rigorous performance analysis of the data stored on SD Card (base station). The recording of the sensor's measurement into the SD card was done in the interval of 30 minutes. The sensor's reading stored on the SD card with date and time stamped for the three parameters are used to plot the graphs of the three parameters versus time. This approach will help the smart-home owners to be kept abreast of their environmental condition and equally know what changes are likely to happen and when. The performance of the system is reliable in terms of captured data, speed, accuracy, integrity and capacity in its storage. Experimental results from the fabricated (device) prototype, demonstrates the efficiency and reliability of the proposed approach. Overall, the system can be deployed in smart homes, remote monitoring and healthcare applications.

The future work will consider the integration of a WiFi module to enable transmission, visualization and storage of sensor data over the internet. The use of the field programmable gate array (FPGA) and system-on-chip (SoC) will be considered to provide flexible, programmable and high-performance capabilities. Smart-home users can access the information regarding their environment from remote locations.

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High Temperature Fluorescence Sensor for Oilfield Applications

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Abstract: Optical fluorescence spectra of crude oils depends on the concentrations of certain chemical components, such as asphaltenes, saturates and aromatics present in these oil samples. In this work, we report a high temperature optical fluorescence spectrometer tool for in situ measurements. This instrument uses a miniaturized spectrometer with a small semiconductor laser source and an optical reflection probe. The miniature sensor was controlled with an Arduino Nano device. We have tested our spectrometer to elevated temperatures present in borehole conditions (100 °C). The results indicate that our logging tool will be able to measure ~95 % of our liquid wells. The fluorescence measurements were compared to standard Saturates-Aromatic-Resins-Asphaltenes (SARA) and Gas Chromatograph (GC) data. The results indicate that the fluorescence spectra could be potentially used to estimate the chemical components of the crude oils. Saturates-Aromatic-Resins-Asphaltenes and Gas Chromatograph measurements are not available downhole, but fluorescence spectroscopy could be used to measure density stratification inside an oil reservoir, which can guide production strategies. It can alert production engineers to heavier crudes, which are less valuable and can be problematic to produce. It can also identify condensate-rich zones in wet gas reservoirs, so that these more valuable zones can be targeted for production.

Keywords: Optical sensors, CMOS sensors, Arduino, Fluorescence, Downhole tool, Oil density.

1. Introduction

The targeting of hydrocarbon reservoirs with favorable fluid properties is essential for increasing profitability for oil companies. As a result, the American Petroleum Institute (API) gravity (a measure of density) [1] is one important property that is measured to ensure that the fluids produced have economic value. Fluorescence measurements of oils can be used to estimate fluid properties, such as API gravity [2-4]. We have recently reported a miniaturized fluorescence measurement for small diameter logging tools [5]. In this work we discuss the dependence of the fluorescence spectra of crude oils on their chemical composition. Crude oil samples have to be carefully prepared in order to be representative of the reservoir fluids; therefore we propose a method of sample preparation to ensure sample uniformity. Further, we discuss how this fluorescence sensing platform can be used to target potential producing zones, both in conventional and unconventional reservoirs. In oil exploration and production a tool is typically deployed inside a well at the end of a conveying cable and chemical/physical properties of oils are measured by moving the tool from the bottom of the well. This is known in the oil industry as wireline logging [3].

2. Motivation

Accurately predicting the API gravity of oils in reservoirs is of great economic importance for oil production, both for conventional and unconventional prospects. Lighter oils and condensates (higher API gravity), for example, are frequently targeted by oil production companies. The cost of refining these hydrocarbon types is minimal compared to other heavier crudes. Condensates also provide valuable sources, such as ethane, for synthesizing plastics and other polymers. Thus, the profit per barrel realized makes producing lighter hydrocarbons more economically attractive and feasible. The economic value of lighter hydrocarbon fluids is also strongly related to the costs to produce them. This is especially true for unconventional reservoirs, where the small nanometer pore structures support relatively low permeabilities measured in nanodarcys [6]. In unconventional reservoirs, horizontal wells are drilled and then several hydraulic fracturing stages are used to increase the flow of the hydrocarbon fluids. Targeting optimal producing zones in parallel horizontal wells can be achieved by measuring properties of a producing well and using that information for the adjacent wells. This step has a critical economic impact, as it can reduce the length drilled and the number of hydraulic fracturing stages required for optimal hydrocarbon production. Unconventional oil reservoirs with nanometer pore sizes will have an increased production when lighter hydrocarbons are targeted. Fluorescence can be used to find such lighter fluids inside the borehole. Tracking the API gravity can be useful in determining if the oil produced matches the source maturity [7]. Anomalous API gravity trends are indications that the pressure inside the reservoir is decreasing too fast and only the lighter oils are being produced, leaving significant amounts of heavier oils behind. Targeting the optimum API gravity is also important in unconventional prospects. Lighter, more mature oil flows more easily in low permeability rocks than heavier oils, and these lower API gravity, more viscous oils are more challenging to produce economically. Measuring and predicting the API gravity for such reservoirs therefore helps to determine production costs and with facility planning. It has been shown that the fluid properties of produced oils can be measured and estimated using fluorescence spectroscopy. The API gravity is one property that shows a strong relationship to fluorescence [2]. Differences in fluorescence occur as the concentrations and types of polycyclic aromatic molecules change with maturity, which correlate to changing API gravity [3]. Therefore, developing a method using fluorescence to predict the API gravity and other fluid properties is essential to estimate the costs of producing different hydrocarbon types.

3. Geochemical Analysis Results

In this work, the 5 oil samples chosen for fluorescence measurements ranged from medium to condensate grades (API 28 to 46), and originated from conventional carbonate reservoirs. Biomarker analysis [7] of the oils correlate both with the API gravity and saturates, aromatics, resins and asphaltenes (SARA) fractions measured [8] (Table 1, Fig. 1) (Saturates-Sat, Aromatics-Aro, Resins, Asphaltenes-Asph). Fig. 1 plots typical Gas Chromatograph (GC) data in the C20 to C27 typical terpanes [7] biomarkers present in crude oils. These biomarkers are important in reservoir design for understanding the source of the oil and in refining processes where the type of output product (such as kerosene) needs to be maximized. Gas Chromatograph analysis is not available in situ and it requires injecting the oil sample into very long glass columns. Fluorescence spectra could be used to correlate the biomarker quantity to the biomarker content of the crude oils.

Table 1. API gravity and SARA percentage compositions of crude oils.

Oil	API	Sat	Aro	Resins	Asph
C-28	28.2	29.27	26.03	17.31	8.84
L-28	28.3	35.26	27.33	17.63	7.68
K-29	29.2	33.13	26.43	16.01	8.56
B-39	39.0	43.73	18.67	9.02	3.63
N-46	45.8	65.92	10.83	5.02	0.13

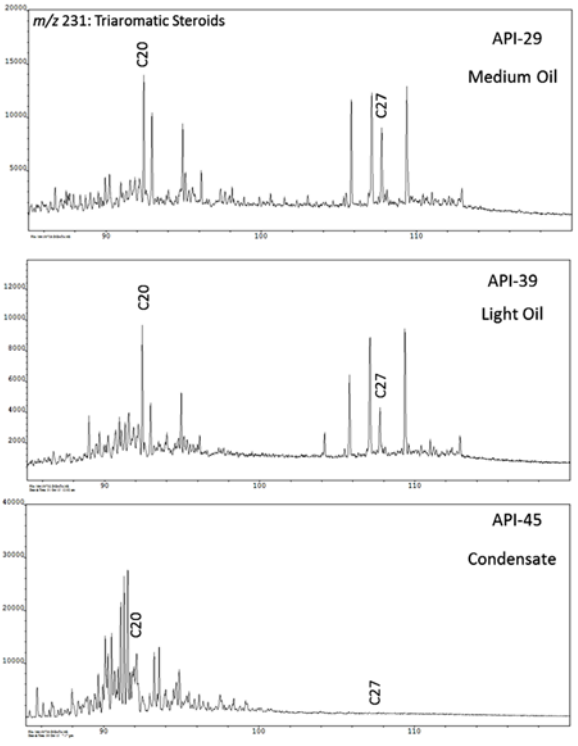


Fig. 1. Biomarker analysis showing changes in triaromatic steroids (C20 vs C27) for oils K-29, B-39 and N-46.

Maturity from biomarker measurements ranged from near peak oil to late oil to well into the condensate stage and were consistent with the increasing API's and the saturate/aromatic ratio (Fig. 1) [6]. API gravities measured are mainly related to the maturity of the oil source. We have to ensure that during the measurement the crude oil sample is not changing and it is representative of the oil samples encountered inside the borehole.

4. Benchtop Spectrometer Results

Fluorescence measurements were performed using a small optical spectrometer, model USB2000+, manufactured by Ocean Optics (Dunedin, FL) [9], a small 5 mW 405 nm laser, and a reflection probe. Before the oil samples were measured, they were thoroughly mixed using a vortex mixer. The homogeneity of the sample was checked with a small refractive index sensor manufactured by FISO Inc. (Ville de Québec, QC) and results are shown in Fig. 2. We used two sensors simultaneously, one near the top of the sample and one near the bottom. The RI values shown are the averages of the values given by the two sensors.

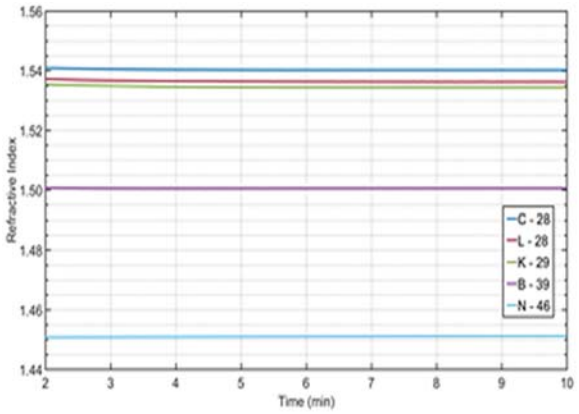


Fig. 2. Refractive index vs time for our oil samples.

As seen from Fig. 2 each sample has a stable refractive index over time, indicating that the heavier components in the oil are not segregating during our measurements. The refractive index correlates with the API gravity, with the heavier oils having larger refractive indices. This property can be used to distinguish oil from diesel-based drilling mud, since this type of drilling mud also exhibits fluorescence. Fluorescence measurements were performed on 10mL samples of each of the 5 oils, the results are shown in Fig. 3. Five milliliters of each sample were removed, had their fluoresence measured, and were then sent for a non-topping SARA analysis (Weatherford Laboratories method), in which traditional SARA is combined with GC to account for evaporation losses [8]. The SARA results are shown in Table 1. The remaining 5 mL of each oil sample had their fluorescence measured as well. For each of the oils there were three fluorescence measurements taken: the original 10 mL sample and the each of the two 5 mL samples after the original was split in half. All three measurements for three of the oil samples are shown in Fig. 4.

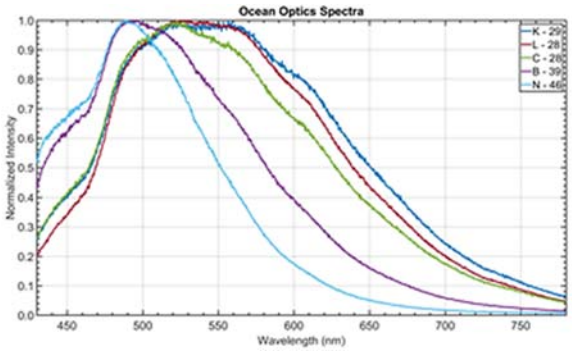


Fig. 3. Normalized fluorescence spectra of five oils using a 405 nm laser.

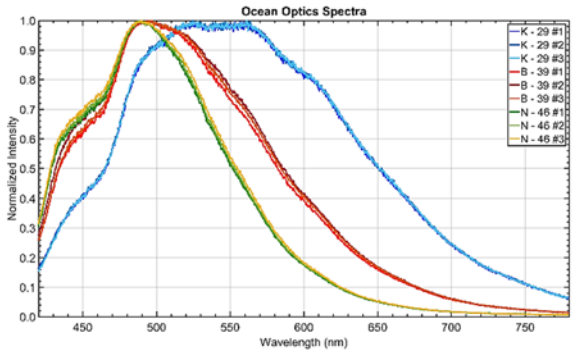


Fig. 4. Variability of optical fluorescence for three oil samples.

The results show that measurements were uniform and the variability between the three containers is small. The largest variability we see is with oil B-39. As the API gravity of the oil decreases, the fluorescence emission redshifts and broadens [2-3], which is consistent with the Urbach absorption. The redshift can be explained by considering that the lower API crudes have fused aromatic rings larger in size compared with those of the higher API gravity crudes [3]. The delocalized π electrons have a lower energy level when the fused rings are larger, resulting in emission at longer wavelengths.

5. Mini Spectrometer Optical Results

Our goal is to implement the fluorescence sensor in a small (43 mm diameter) wireline tool. The environmental requirements are 350 bar hydrostatic pressure and 100 °C operating temperature. For this

purpose, we have used a small form Hamamatsu mini spectrometer model C12880MA-10 [10] (Bridgewater, NJ). The spectrometer has a 256 pixel CMOS sensor and a glass based diffraction grating. The spectrometer was integrated with an Arduino Nano microprocessor using a V3.0 Elegoo Nano board type CH340/Atmega328P. We performed a calibration measurement of both spectrometers using two known fluorescent dyes, Fluoro-Max Green and Red by Thermo Fisher Scientific. The response of both spectrometers was calibrated using a black body radiation source, Ocean Optics HL-2000-FHSA (Dunedin, FL). The results are shown in Fig. 5.

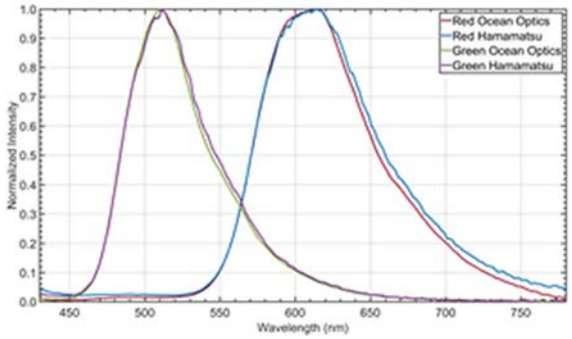


Fig. 5. Fluorescent dye spectra comparison.

The red/green fluorescence spectra match well after the instruments were calibrated. The calibration was done by taking into account the dark counts and the response of each instrument to a known black body radiation source. This calibration methodology needs to be used in any instance where two spectrometers are compared, as variability in responses can affect the results in some cases by as much as 25 %. Fig. 5 also indicates that although the CMOS sensor in the mini spectrometer has a factor of 10 fewer pixels than the Ocean Optics spectrometer, its spectral resolution is still sufficient for our measurement.

Fig. 6 presents an optical image of the mini spectrometer and the microcontroller.

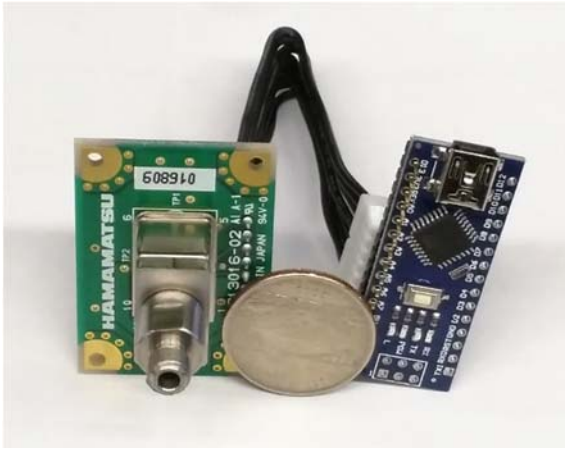


Fig. 6. Optical image of mini spectrometer and Arduino microcontroller. USA Quarter for scale.

The small Hamamatsu board was used for ease of wiring. A diagram of the sensor circuit board is presented in Fig. 7. The actual Arduino code does not require the Hamamatsu board and the spectrometer is connected directly to the microcontroller which, in turn, is connected to a wireline main controller.

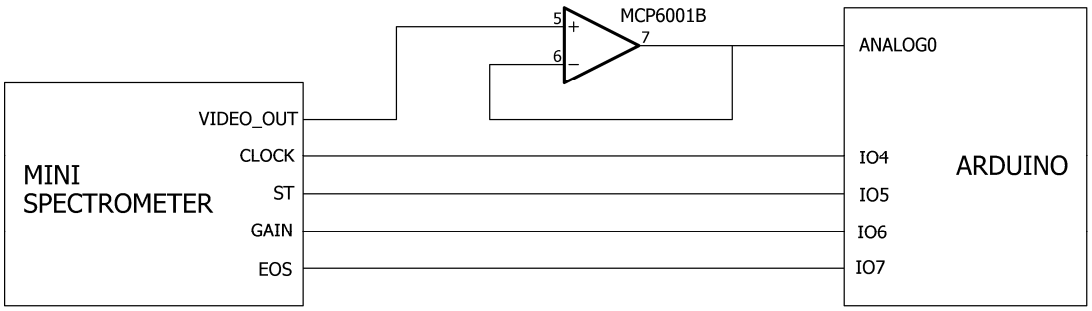


Fig. 7. Mini spectrometer electronic control diagram.

6. High Temperature Tool Implementation

The packages of the active optical components in our system are hermetically sealed to prevent damage due to moisture, i.e. the laser chip, the CMOS detector and the optical grating in the spectrometer. The hermetically sealed packages cannot be pressure compensated for the 350 bar required for our wireline logging tool. The TO56 laser and the C12880MA-10 mini spectrometer need to be housed inside the wireline tool at atmospheric pressure. Due to these requirements, we have opted for a fluorescence reflection probe which protrudes from the pressure housing of the tool. The pressure tolerant optical probe was manufactured by Custom Sensors Inc. (Fenton, MO). A picture of the wireline tool with two sensor ports is shown in Fig. 8. The housing for the

electronics is shown on the left side of the top image. The tool can be connected to another logging module, via the connectors on the right side of the top image.



Fig. 8. Optical images of the fluorescence probe.

The bottom image of Fig. 8 shows the fluorescence probe inserted into the tool connector (left port). The optical probe has one 600 µm core fiber in the middle for the source and eighty-one 100 µm core fibers around the outside for the spectrometer arm. This geometry ensures a good signal for our samples. The tip of the probe is protected with a sapphire window suitable for harsh downhole conditions. The fluorescence probe uses one port, while the other port can be used for another type of fluid property sensor such as refractive index, density, viscosity, or temperature. A temperature probe is shown in the right port of the bottom image in Fig. 8.

Two models of miniature spectrometers were tested for dark voltage counts at elevated temperatures. The model C12666MA spectrometer has lower noise due to a lower gain, while the model C12880MA-10 spectrometer has higher sensitivity due to a higher gain. The results are plotted in Fig. 9 for the C12666MA spectrometer (top) and C12880MA-10 spectrometer (bottom). The dark counts increased with temperature due to increased leakage of the CMOS sensor and also due to high leakage in the amplifiers used after the CMOS sensor. The dynamic range of our CMOS sensor is ~5000 at 25 °C. The low limit is set by the dark counts in the pixel and the high limit is set by the 'depth' of the capacitor. As the temperature rises, the dark counts go up exponentially as seen in Fig. 9. At some temperature the dark counts will fill up the pixel completely and the CMOS sensor will be saturated. We can also consider the 5000 dynamic range of the sensor as a temperature dynamic range. With this temperature range (25-100 °C) we can measure more than 95 % of our targeted liquids wells. The C12880MA-10 spectrometer has ~150X more gain when compared with the C12666MA model. This sensitivity can be useful when measuring samples with lower fluorescence level such as heavier crude oils.

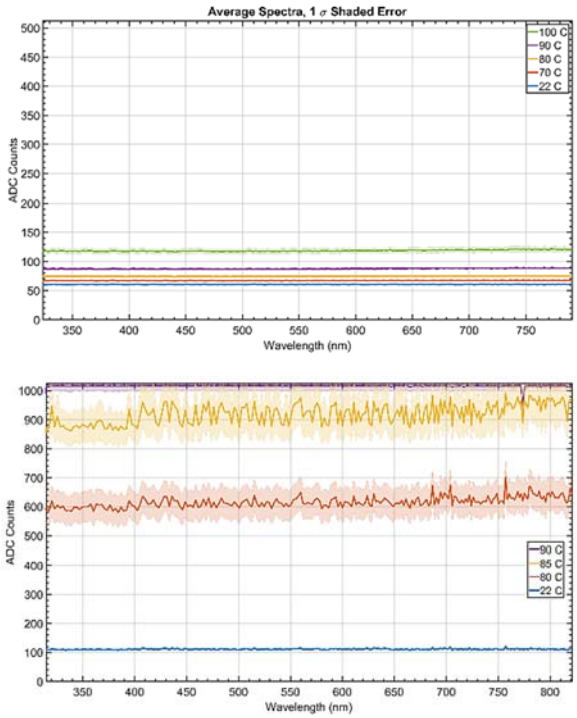


Fig. 9. Dark counts of the mini spectrometer at different temperatures for two models C12666MA (top) and C12880MA-10 (bottom).

7. Conclusions

In this paper we have investigated the relationship between chemical composition of hydrocarbon fluids (SARA) and optical fluorescence. We have shown that the density of an oil changes the shape of its fluorescence spectrum, with more mature sources (higher API gravity) having a blue shift compared to less mature oil sources (lower API gravity). We have also presented the integration of a mini spectrometer into a small diameter (43 mm) logging tool. The performance of the logging tool is similar to a benchtop, laboratory grade spectrometer. The optical measurement was integrated into the wireline tool using a high pressure (350 bar) fluorescence reflection probe. The probe itself is rated to a temperature of 150 °C. The miniature spectrometer was tested for high temperature operation. The results indicate that our logging tool could be used in most of the wells encountered in our application.

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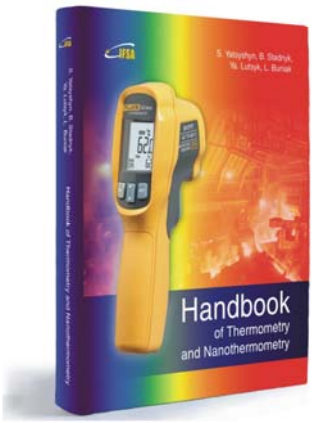
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Handbook
of Thermometry and Nanothermometry

IFSA

S. Yatsyshyn, B. Stadnyk, Ya. Lutsyk, L. Buniak



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Time-based Acoustic Displacement Transducer

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Abstract: The purpose of this research is to design and test an acoustic linear displacement transducer operated in a time-based measurement. A standard computer system supported with a sound card has been used in order to realize the measurement, process, and store data. The operation principle of the proposed transducer is summarized as follows. The acoustic transmitter (speaker) which is fixed at one end of a resonance tube generates a pulse signal with specific parameters and then the pulse travels within a glass tube (filled with air) and is reflected from the other end of the resonance tube, which is a part of a movable spindle. The time of the reflected signal will be measured using an acoustic receiver (MEMS or electrolyte microphone) which is located at a specific distance from the speaker. A mathematical representation and experimental tables describing the relationship between displacement and the time of the reflected signal will be illustrated.

Keywords: Displacement Measurement, Standing wave, Phase Shift, Time Delay, IOT.

1. Introduction

Measurement of dimensions, displacements and deformations are widely used in modern industrial automation. Displacement measurement plays a great role in various industrial applications [1]. The role of displacement transducers in industrial measurements is also great because when measuring many mechanical quantities such as force, pressure, and torque, they are first converted to displacement and then transferred to an electrical quantity.

Devices for measuring displacement are widely used in various systems of automatic regulation and control. The use of such devices is a typical example of how to determine the dimensional changes and deviations of part shapes during the process of sorting and processing to regulate the position and movement of various objects. Measuring devices used in engineering and instrument manufacturing, used in the processing of parts, is mainly intended for measuring small displacements (less than 1 mm); measuring devices for measuring large displacements is used to measure the positions of different objects, liquid levels and in other similar cases [2].

Displacement transducers are used in industry to measure distance of objects and related parameters such as displacement, velocity and vibration [3]. For this purpose, measuring displacement transducers are classified by the range of their inputs. The first class of small displacement transducers (up to 2-3 mm for linear and 2-3 ° angular displacements) is utilized. The second class contains large displacement transducers (up to several meters for linear displacement and 25-40 revolutions for angular displacements). Various types of measuring transducers are used for measuring displacement such as rheostat, strain gauge, inductive sensors, capacitive sensors, radiation transducers and acoustic transducers [4].

Inductive sensors are widely used in the industry for measuring movements in the range of tenths of a micrometer to units of decimeters, as well as for

measuring other physical quantities that are converted into movement. This is due to the significant advantages of inductive sensors such as the simplicity of design, reliability, high sensitivity, significant output power, protection from external electric and magnetic fields [5]. An example of a well-known inductive sensor is Linear Variable Differential Transformer (LVDT) [6], a transformer with a mechanically controlled core. A sinusoidal voltage of constant amplitude is applied to its primary winding. On the secondary windings, an alternating voltage is induced. A core of ferromagnetic material is inserted into the cylindrical hole between the coils. In this case, the core does not touch the windings. Two secondary windings are included in the anti-phase. When the core is located in the center of the transformer, the output signals of the secondary coils mutually cancel each other, so there is no voltage at the transformer output. Moving the core away from the central position leads to a change in the magnetic fluxes in the secondary windings. As a result of the resulting unbalance, the output voltage appears. The change in magnetic fluxes occurs due to a change in the magnetic resistance of the space between the coils. On the basis of what has just been mentioned, it follows that the magnitude of the flux linkage is determined by the axial position of the core. In the linear working region, the amplitude of the induced signal is proportional to the displacement of the core. Therefore, the output voltage contributes to the measurement of movement. The output of the LVDT not only shows the amount of movement, but it also displays its direction. The direction of movement is determined by the phase angle between the reference and output voltages. The reference voltage is produced by a stabilized generator.

Capacitive displacement transducers operate on the principle of a capacitor, which is formed by two plates separated by a dielectric. The change in the size of the plates, the distance between them or between them and the dielectric causes a change in capacitance.

With respect to the capacitance change, several types of capacitive sensors are found in industry such as capacitive proximity sensor and the capacitive proximity switch. These sensors are capable of detecting the target at some distance from the instrument.

Capacitive transducers are used to measure angular and linear displacements, linear dimensions, level, forces, humidity, concentration, etc. They can be structurally made with plane-parallel, cylindrical, pin electrodes, with or without dielectric between the plates.

High accuracy of displacement measurements can be obtained using optoelectronic transducers. The operation principle of these transducers is based on the use of optoelectronic transmitters and receivers of optical radiation, including but not limited to raster and moire methods. In the raster method, two flat plates with parallel strokes are used. The distance between the strokes on each plate is constant, but for the two plates is slightly different. When the plates (rasters) are superimposed on one another and their transmission is observed, the zones of condensation and discharge of striations. Moving one raster relative to the other in a direction perpendicular to the strokes causes the indicated densification zones to move in the same direction.

In the Moire method, the rasters on the two plates have the same pitch, but they are located at a small angle α. to each other. When overlaying rasters and their translucence, there are light and dark bands running across the strokes and called combinational or moiré strips. Moving one of the rasters causes a much larger displacement of the Moire bands in a direction perpendicular to the direction of the raster's movement, i.e., optical reduction also occurs. The presence of optical reduction in the methods of raster and moiré makes it possible to achieve a high sensitivity to the measured movement.

The choice of the type of transducer is determined by several factors: the range of measured displacements, the static and dynamic characteristics of the transducers, the practical design, and reliability, and the output signal [7].

Most of the displacement transducers used in practice are analogue types. However, there are also digital transducers which have a built-in analog to digital converter, which provides a simple interfacing with most popular data acquisition and computer systems.

Computer technology makes the way of development of measurement and control systems more effective and less costly [7]. Nowadays, several computer systems and platforms such as Arduino, Raspberry PI and minicomputers [8] invest in measurement and control to build measurement and control systems which could be used in industrial, domestic and medical applications. Furthermore, these computer systems are considered the base of IoT (Internet of Things) and cloud computing.

The present trend in computer development could be applied to several transducers, which are capable of working in industrial environments [6, 9, 10].

In works [6, 9], the authors utilize the acoustic standing wave phenomenon to build a displacement transducer operating in both forced and resonance modes to measure displacement. The transducer is used to measure linear displacement in different ambient temperatures. The measurement setup consists of a resonance tube filled with air, a speaker attached at one end of the tube and a microphone located at the other end of the tube (which forms the movable spindle). In work [6], the authors generate an acoustic signal traveling within a resonance tube and received by microphone, and then the amplitude of received signal is measured by a computer software such as LabVIEW. In work [9], the authors apply free resonance mode of operation of a resonance tube, in which the resonance frequency generated within a tube depends on the distance between the transmitter (speaker) and receiver

(microphone) of an acoustic signal. The LabVIEW software is used to measure the frequency of the signal received by the microphone.

2. Literature Review and Theoretical Background

The general name "acoustic sensors" or acoustic transducers refers to a class of very diverse devices based on acoustic measurement. The commercial use of acoustic sensors and transducers began more than 60 years ago. The most important application of these devices is the telecommunication industry, which annually uses about 3 billion of acoustic wave filters, mainly in mobile phones and base stations. Basically, these are devices that work with surface acoustic waves and serve in the transmitters as band-pass filters for both intermediate frequencies and frequencies of radio waves [11].

In addition, acoustic sensors and transducers are used in the automotive industry (torque and tire pressure sensors), medicine (chemical sensors), oil industry (gas chromatography) and many other fields (as moisture sensors, temperature sensors, etc.).

The reasons for such widespread use of this technology in industry are low cost, reliability, sensitivity and endurance of devices. In addition, some of them do not need power sources.

As a detection mechanism, a mechanical, or acoustic, wave is used. When a wave propagates within a material or on its surface, any changes in the characteristics of the wave propagation path affect the velocity and / or wave amplitudes. The frequency and phase characteristics show the change in the speed of the wave.

Sensors and transducers based on acoustic waves are extremely versatile devices whose commercial potential is only beginning to be realized. They are competitive in price, durable, very sensitive, and reliable, and even some of them are wireless and / or do not require batteries. Acoustic sensors are very convenient for use on moving objects, for example, for measuring the pressure of tires on machines or the shaft torque. In addition, acoustic sensors are desirable for remote observation of chemical evaporation, humidity and temperature. Other applications include the measurement of force, acceleration, shock wave, angular velocity, viscosity, displacement and flow, as an addition to the film characteristics. The sensors also have electroacoustic sensitivity, which allows them to determine the level of pH, ionic impurities and electric fields.

Furthermore, acoustic transducers based on standing wave measurement are also used in many industrial applications for measuring displacement, temperature, density and speed of rotating shaft [13-14]. The operation principle of these devices is based on the creation of a standing wave within a resonance tube. Then the measurement of the desired parameter is obtained by measuring the change of the condition of creating a standing wave. Although the author in works [6] and [9] develops displacement transducers for measuring the displacement of a spindle within a resonance tube, these works are operated by the resonance existed in the tube. This work also utilizes the resonance tube for measuring displacement. Instead of creating a standing wave within a tube, a pulse with a short duration is generated, and then the time of the phase of the reflected signal is measured.

3. Operation Principle

The operation principle of acoustic sensors is based on the radiation, reception and analysis of a direct or reflected acoustic wave. The speaker generates an acoustic signal, which is received by a receiver that converts the acoustic signal into an electrical one. A computer system is widely used to acquire and analyze the information received by the receiver.

Acoustic sensors are widely used as proximity sensors, for remote detection of various objects, for measuring distances. Currently, the market offers a wide selection of acoustic sensors in various designs, operating in different acoustic frequencies. The behavior of different acoustic frequencies in similar environmental conditions is not the same. In most cases, it will not be difficult, guided by the specifications given by the manufacturer, to select the appropriate sensor for its task. But in cases where there are malfunctions or significant errors in measurements in the operation of devices, it is necessary to make a more thorough assessment of the influence factors, such as:

- Changes in sound velocity depending on temperature and environmental properties (mainly air), - how these changes affect the accuracy of measurements and the resolution of the sensors;
- Changes in the length of the sound wave depending on the speed and frequency of sound, - how these changes affect the accuracy of measurements, resolution, minimum object size, minimum and maximum distance to the object;
- Changes in attenuation depending on the frequency of sound and humidity, - how these changes affect the maximum sensitivity distance of the sensors in the air;
- Changes in the level of external noise as a function of frequency, - how these changes affect the maximum sensitivity distance and the size of the detection object;
- Changes in the reflected echo amplitude depending on the distance to the object, the size and geometry of the surface, - how these changes affect the sensitivity distance.

In this work an acoustic sensor based on measurement of the time of reflected echo pulse is presented. The wave surface can be drawn through any point in the space covered by the wave process. Consequently, there are an infinite set of wave surfaces, while there is only one wave front at each

moment of time. The wave surfaces remain stationary. The wave front moves all the time. Wave surfaces can be of any shape. In the simplest cases, they have the form of a plane or sphere.

Accordingly, the wave in these cases is called flat or spherical. In a plane wave, the wave surfaces are a set of planes parallel to one another, in a spherical wave there are a number of concentric spheres.

If a particle of an elastic medium at point 0 (Fig. 1) oscillates in accordance with the formula

$$S(t) = A_0 \cos(\omega t), \tag{1}$$

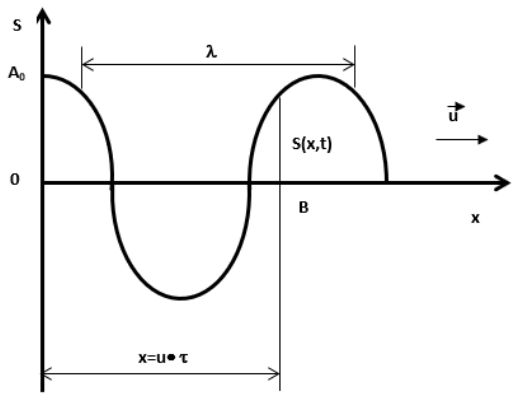


Fig. 1. The of oscillation of particles in a planar waveform

where S (t) is the displacement of the particle of the medium from the equilibrium position; $A0$ is the amplitude (the largest displacement of the particle of the medium from the equilibrium position); t - time; T - period (time of one complete fluctuation); ω = 2πT - cyclic or circular frequency; then an arbitrary point B of the medium will come with an oscillatory motion with some time lag.

$$\tau = \frac{x}{u}, \tag{2}$$

where x is the distance over which the oscillation from point 0 to B has propagated, u is the propagation velocity of the wave (phase velocity of the wave).

The equation of the dependence of the displacement of a particle of the medium on time at point B will be written

$$\begin{aligned} S(x,t) &= A_0 \cdot cos\omega(t-\tau) \\ &= A_0 \cdot cos\left(\omega t - \frac{\omega x}{u}\right), \end{aligned} \tag{3}$$

where ω/u = 2π/T·v = 2π/λ = k is the projection of the wave vector onto the OX axis; λ = T·v is the wavelength.

Thus, a wave propagating in the direction OX in an infinite elastic rod or an extended column of gas (air) is described by the equation of a plane monochromatic traveling wave:

$$S(x,t) = A_0 \cdot cos(\omega t - kx + \varphi_0), \tag{4}$$

where φ = (ωt-kx + φ0) is the phase of the wave, and φ0 is the initial phase.

The wave Equation (3), as well as waves of a more complex type, are a solution of the one-dimensional wave equation:

$$\frac{\partial^2 S}{\partial t^2} = \frac{1}{u^2} \cdot \frac{\partial^2 S}{\partial x^2}, \tag{5}$$

where u is the phase velocity associated with ω and k by the relation: u = ω/k = λ/T = λ·ν, where, in turn, ν is the linear frequency of the oscillations.

The phase velocity is the velocity of a certain phase value, which unambiguously characterizes the fixed state of the vibrational motion of the particles of
the medium.

The distance λ traversed by the wave (determined by the oscillation phase) during one oscillation period is called the wavelength, i.e. the wavelength is the shortest distance between adjacent particles of the medium, which oscillate in the same phase.

The oscillation frequencies ν of the particles of the medium have the same frequency as the oscillation frequency of the wave source. Waves, the frequency of oscillation of particles in which lie in the range from 16 to 20,000 Hz, are called sound waves.

Sound waves in gases and liquids are longitudinal and can propagate only in an elastic medium.

Sound waves, like electromagnetic waves, have a number of properties: interference, diffraction, reflection, etc.

The speed of sound in gases close to ideal is equal to

$$u = \sqrt{\frac{\gamma RT}{M}}, \tag{6}$$

where γ = Cp/Cv is the ratio of the specific heats of the gas at constant pressure Cp and constant volume Cv; M is the molar mass; R is the universal gas constant.

Standing waves are usually created when the incident and reflected from the obstacle are added, for example, reflected from the end of the tube containing the gas.

Suppose that two plane waves with the same amplitudes and frequencies propagate along the OX axis in opposite directions. If the origin is taken at a point at which the opposing waves have the same phase and the time is selected so that the initial phases are equal to zero, then the equation of both plane waves can be written in the following form.

For a wave traveling in the direction of the positive OX axis

$$S_1 = A_0 \cdot cos(\omega t - kx) \quad (7)$$

and for a wave traveling in the direction of the negative axis OX

$$S_2 = A_0 \cdot cos(\omega t + kx) \quad (8)$$

A standing wave is described by the expression:

$$S = S_1 + S_2 = 2A_0 \cdot cos(kx) \cdot \cos(\omega t) \quad (9)$$

The factor $A = 2A0 \cdot |\cos(kx)|$, which does not depend on the time t, expresses the amplitude of the standing wave. However, the position x could also be determined using the phase shift between the two signals S1 and S1. The phase shift expresses the time delay between the two shifted signals, as will be shown in the next section.

The phase difference of the simultaneously applied electric oscillations is measured by a microphone and it has the form: $\delta = \varphi 1 - \varphi 2 = 2\pi x/\lambda$.

The phase shift is converted into time shift using the following formula

$$t = -\frac{\delta}{\omega} = \frac{\varphi 1 - \varphi 2}{2\pi f} \quad (10)$$

The Formula (10) is used to measure the distance.

4. Design of An Experimental Setup and Testing Procedure

In this report, the length of a sound wave in air is measured by time delay which depends on the phase shift method between oscillations of the source of oscillations and oscillations in different parts of the traveling wave propagating in the air.

The experimental setup consists of the following parts: Speaker (1), Microphone (2) to measure the time shift fixed at near the speaker and parallel to it, a glass tube closed on both sides (3), Microphone (4) fixed on the spindle (5) which is freely moving along the waveguide, a measuring ruler (6).The schematic design of the transducer is shown in Fig. 2.

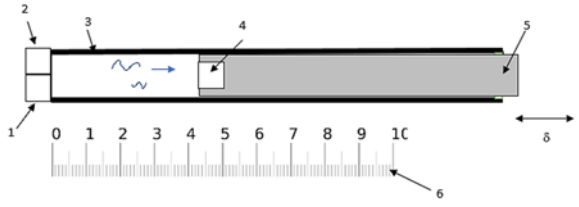


Fig. 2. The schematic design of acoustic transducer for displacement measurement.

The speaker 1 is powered by the output of a sound card which is a part of standard PC. The parameters (i.e, phase shift) of the sound wave is measured by microphone placed parallel to the speaker (Microphone 1).

The operation principle is follow. A pulse of signal is transmitted via a media and reflected by the spindle surface. The phase of reflected signal and the time shift is measured by acquiring the sound using Microphone 1.

At time t_0, the phase value φ_1 of transmitted (original signal) sound wave is ωt si measured by microphone 4, where $\omega = 2\pi\nu$ is the cyclic frequency of the oscillations.

The sound signal received by the microphone 1 placed has a phase value φ_2 equal to $\omega t - 2\pi x/\lambda$, where x is the distance between the speaker and the microphone, and λ is the length of the sound wave. The coordinate x is between the speaker and microphone.

5. Software Development

Modern programming languages and programming environments designed for developing measurement and control application software provide a wide range of tools, both for experienced programmers and for those who are not experienced programmers.

These tools allow the researchers and the students interested to create custom programs directly in standard programming languages, for example C / C++, Basic, as well as using special scientific programming languages such as MATLAB and Mathematica and LabVIEW [15].

According to the method of programming, these programming languages are divided into the following:

- Text or text-graphical programming languages of environment (Pascal, Delphi, LabWindows / CVI, Measurement Studio, Visual Basic, Visual C / C ++) that use elements of visual text programming to create user interface applications and focus first turn on experienced programmers;
- Graphical object-oriented (InTouch, "Trace Mood"), based on the use of graphic images of the automated process control system in as elements of programming;
- Graphical functionally-oriented (LabVIEW, LabVIEW / DSC, Agilent VEE), using the functional-logical principle design (drawing) and graphical representation of algorithms programs.

Graphic programming environments are easily mastered not only by professional programmers, but also by non-experienced programmers. On the one hand, modern graphical systems allow you to create programs that are almost as effective as programs written in text packages. With other parties, in most cases, graphical programs are more visible, easier to modify and debug, and faster to develop.

The main advantage of graphic programming systems is that the developer of the application, whether the engineer or technologist, can be the director himself.

LabVIEW (Laboratory Virtual Instrument Engineering Workbench) is one of the data flow programming environments that allows you to develop application software for organization of interaction with measuring and control equipment, collection, processing and display of information and calculation results, and modeling of both individual objects and automated systems in whole. The developer of LabVIEW is the American company National Instruments [16].

In this work, the author will use LabVIEW for developing the required software for data acquisition and signal processing. The flowchart of the developed software is shown in Fig. 3.

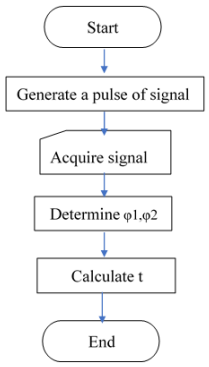


Fig. 3. Flowchart for developing software.

The flowchart illustrated in Fig. 3 can be easily converted into LabVIEW program, which is also called VI (Virtual Instrument). The program in this case consists of small programs, called subVIs or VI. These VI can be found in any version of LabView. The developed LabView Vi for receiving and processing the acquired signal is shown in Fig. 4.

The description of the main VIs is explained in Table 1.

Table 1. Description of the main VI's.

LabView VI	Description
	Acquire a sound signal by a microphone
	Generate a sound signal with specific parameters
	Measuring sound parameters: Amplitude, Phase, Frequency
	Stop program

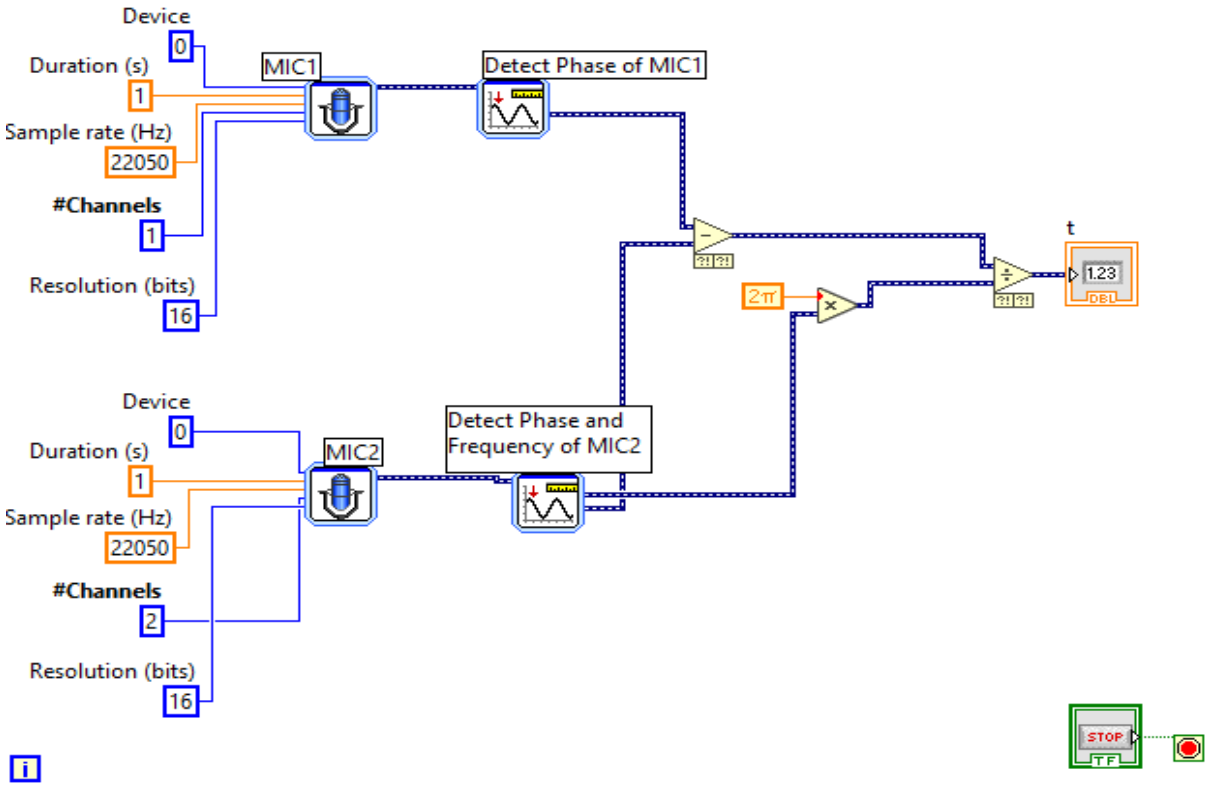


Fig. 4. The developed LabView Vi.

6. Experimental Results

The experimental results present the relationship between the measured distance and the time shift, as illustrated Fig. 5. The point 0.05 is chosen as a reference value to avoid non-linear effects that may appear in the zone near the speaker [16].

The plot of experimental results is shown in Fig. 5.

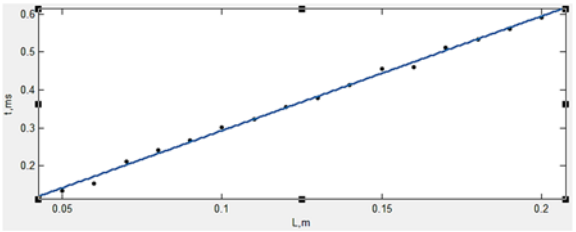


Fig. 5. The plot of experimental results.

7. Conclusion

It has been shown that a computerized transducer for displacement measurement is designed and experimented. The designed transducer is efficient, inexpensive, and multipurpose. It could be integrated with other primary non-electrical sensors and orders to get an electrical read out and to realize computer data logging and automatic positional control.

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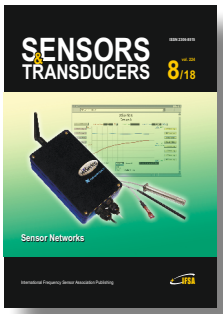
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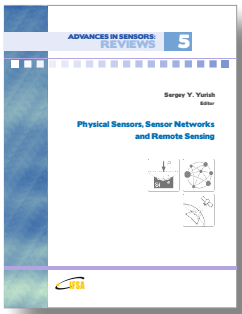
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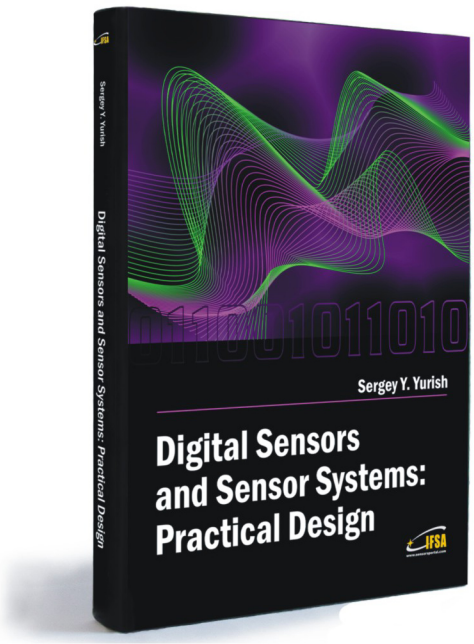
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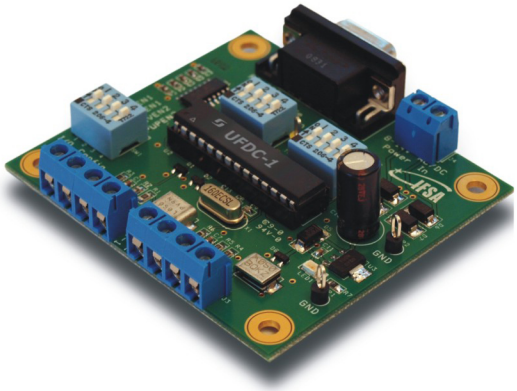
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