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130 nm CMOS SAR-ADC with Low Complexity Digital Control Logic

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Abstract: This paper reports on an original approach to design the digital control logic of a Successive Approximation Register Analog to Digital Converter, where no sequencers or code registers are used. It turns out a low complexity digital circuitry, which is applied to the design of a 130 nm CMOS 8-bit SAR ADC. The simulations demonstrate that the proposed digital control logic correctly works leading to an Analog to Digital Converter exhibiting performances well aligned with the literature in terms of linearity, dissipated power, and energy spent per bit generation.

Keywords: SAR-ADC, Control circuitry, CMOS, Shift register, Counter.

1. Introduction

The Successive Approximation Register Analog-to-Digital Converter (SAR-ADC), when compared with other ADC solutions (e.g. sigma-delta ADC, pipeline ADC), has its strengths in the low power consumption, medium-to-high resolution, and small form factor. Its weakness is in a high latency, as the conversion process requires operation cycles as many as the resolution. This mix of strengths and weakness makes the SAR-ADC very well suited for applications targeting low frequency signals and suffering from a limited energy availability. In medicine, the battery powering the integrated electronics front-end cannot be frequently replaced, because it is often implanted (e.g. pace-makers, heart defibrillators, epileptic seizure detector). In smart agriculture, the nodes of the sensor network distributed on a cultivation (e.g. vineyard) should work with a limited amount of available energy, because this energy should be harvested from the environment. Same consideration holds for the mobile sensors embedded in the collars for the smart monitoring of livestock (e.g. cow).

A SAR-ADC converts the value of the input analog signal, sampled at the given time, into a digital word generated after a given latency time elapsed from the sampling instant. The conversion process is based on a binary search algorithm, which explores a binary tree to find the best digital approximation, for a given resolution, of the input analog value. During the latency time the SAR-ADC explores this binary tree. The binary search algorithm is implemented in a digital control circuitry, which is usually constituted by sequencers and code registers [1-5], that makes complex the design flow. Aim of the present paper is to report on a low complexity approach to the design of the digital control circuitry [6]. The paper is organized as follows. Section 2 explains how the binary search algorithm can be implemented, in order to simplify the design of the digital control circuitry.

Section 3 focuses on the architecture and schematic of the proposed digital control circuitry. Section 4 applies the proposed digital control circuitry to the design of an 8-bit SAR-ADC in a bulk CMOS 130 nm CMOS technology. Section 5 reports on the performances obtained for the designed SAR-ADC. Eventually, the paper ends with Section 6, where some conclusions are drawn.

2. Binary Algorithm Implementation

Fig. 1 depicts the general architecture of a SAR-ADC. It is constituted by three main building blocks: the comparator, the Digital-to-Analog Converter (DAC), and the digital control circuitry, which is called hereinafter Digital Control Logic (DCL).

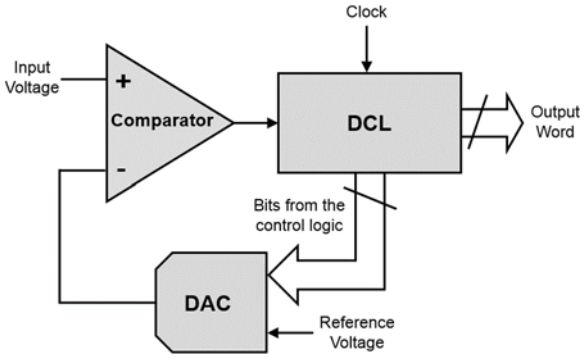


Fig. 1. General architecture of a SAR-ADC.

The present section addresses the implementation of the search binary algorithm run by the DCL. Generally speaking, the chosen implementation can make the design of the DCL more or less complex. In particular, in the present work the implementation was simplification orientated. For sake of clarity, a 4-bit resolution SAR-ADC is addressed.

The proposed approach moves from thinking of the DCL as a finite state machine, a point of view not adopted in the literature, even when the design sounds very close to a state transition diagram [2]. Fig. 2 depicts the state transition diagram for the DCL, described as a finite state machine. It is worth noticing that the state diagram reproduces the structure of a binary tree. The diagram is distributed on four layers. The first layer is the initial state. In the fourth layer are the final states obtained at the end of the digitization process. The DCL goes through the states following the outcome of the comparator around which the SAR-ADC is designed (see Fig. 1). Fig. 2 shows that in the approach proposed in the present paper, for a 4-bit resolution SAR-ADC, each state is encoded into six bits. The two right-most bits (in grey) count the layer (e.g. they are "00" for the first layer and "10" for the second layer). The remaining four bits (in black) track the sequence of the comparator outputs. In the initial state, these bits are all set to "1". After each comparison, these bits are right-shifted and the left-most one is replaced by the comparator outcome.

In the general case of an R-bit resolution ADC, the right-most bits in grey are in the number of the next higher integer of $\log_2 R$ and the remaining bits in black are in the number of R.

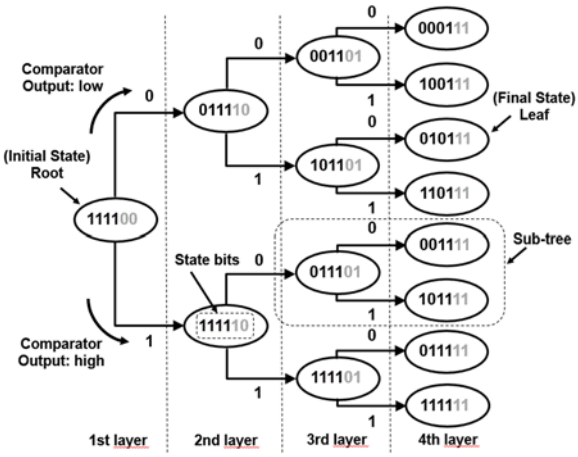


Fig. 2. State transition diagram for the DCL.

3. DCL Architecture and Schematics

The state encoding described in the previous section does not minimize the number of bits for the design of the finite state machine. In fact, four bits would be indeed enough to encode the fifteen states in Fig. 2. The advantage offered by the proposed state encoding is that the next state of the binary algorithm can be generated from the actual one by using a shift register for the bits in black and a counter for the bits in grey, making straightforward, in this way, the design of the DCL. The resulting architecture of the DCL is depicted in Fig. 3.

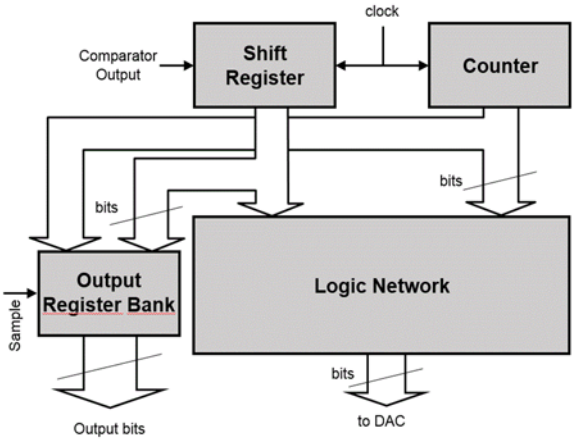


Fig. 3. Building block diagram of the DCL.

It is constituted by four main building blocks: a shift register, a counter, a logic network, and an output

register bank. Note that no sequencers and code registers are used. The shift register can be obtained by cascading four D-type registers as depicted in the following Fig. 4(a). The counter can be implemented as a binary counter obtained by arranging two D-type registers as in Fig. 4(b). Eventually, the output register bank is an array of four D-type registers as sketched in Fig. 4(c). In the case of a 4-bit resolution SAR-ADC, the design of the DCL requires therefore a total of ten D-type registers. The D-type register is therefore the basic cell to build up the DCL. In the present work, this register was designed by arranging in a master-slave configuration two transmission gates based latches, as depicted in the following Fig. 5.

Fig. 4 shows the ten D-type registers used in the case of a 4-bit resolution SAR-ADC. For a higher resolution R, the DCL can be quickly re-designed by just extending the register chains in Fig. 4. This consideration highlights the simplification in the design of the DCL allowed by the sub-optimal state encoding described in Fig. 2. The shift register and the output register bank, each needs a chain of R D-type registers and the binary counter needs a chain with a number of D-type registers equal to the next higher integer of $\log_2 R$. In the case of an R-resolution SAR-ADC the design of the DCL requires therefore a total of $2R+ \log_2 R$ registers.

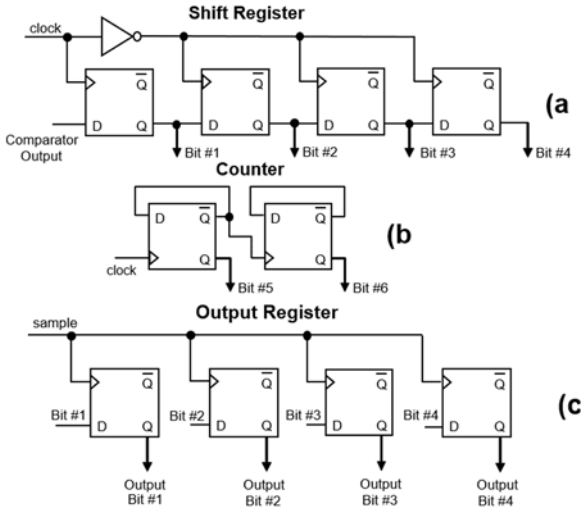


Fig. 4. Schematics of the shift register, the counter, and the output register bank in the case of a 4-bit SAR-ADC.

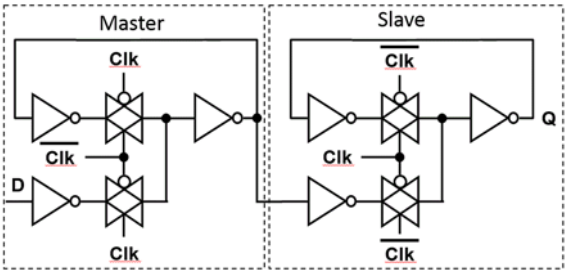


Fig. 5. Schematic of the D-type register.

The state encoding bits, as generated by the shift register and the binary counter, cannot be used directly to control the DAC. The logic network in Fig. 3 is in charge of translating the state encoding bits into signals useful to control the DAC. The design of this logic network depends therefore on both the implementation of the DAC and the specific architecture of the SAR-ADC.

4. 8-bit Resolution SAR-ADC

The previously described idea of DCL was applied to the design of an 8-bit resolution 130 nm CMOS SAR-ADC, whose architecture is depicted in the following Fig. 6. As in the case of the general architecture in Fig. 1, it uses one comparator and one DCL but, as a difference, it uses two DACs instead of only one. With the DAC implemented in the form of a switching capacitor network, as depicted in the following Fig. 7, this architecture allows for the minimization of the dissipated energy [2]. The use of two DAC's leads to a different way of using the comparator. In the general architecture the comparator receives the sampled value of the analog input signal V_{IN} to be digitized (see Fig. 1) while in the architecture in Fig. 6 V_{IN} is sampled by the DAC2 when the signal Sample is active. The comparator compares the voltages at the node Y and Z generated by the two DACs.

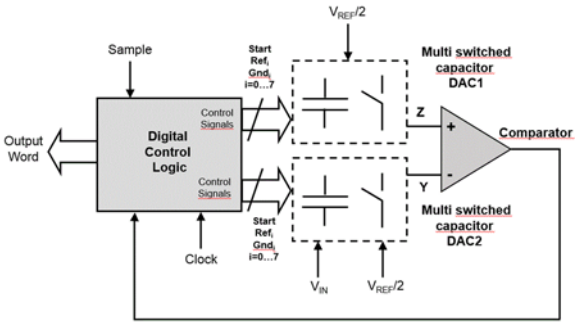


Fig. 6. Architecture of the designed 8-bit SAR-ADC.

For the architecture in Fig. 6, the logic network, has been designed to implement the following switching strategy. During the sample phase, the capacitors in the DAC1 are discharged with both plates at the potential $V_{REF}/2$, where V_{REF} is the reference voltage used for the conversion process, while the capacitors in DAC2 are charged at V_{IN}-$V_{REF}/2$. In the following phase, all Ref_i signals are forced to 1 and Gnd_i signals to 0. This phase generates the Most Significant Bit (MSB). The comparator outcome is used by the DCL to generate the future control signals for the two DACs. In particular, at the n^{th} comparison phase, the signal Ref_n is forced equal to the comparator outcome and the signal Gnd_n equal to inverse of the comparator outcome. At the same time, the signal Ref_{n-1} is forced to zero and the signal

Gnd_{n-1} to one. In this way, comparison by comparison the DCL explores the binary tree of Fig. 2 until the Least Significant Bit (LSB) is generated. For an 8-bit resolution SAR-ADC the logic network receives therefore eleven ($8+\log_2 8$) bits from the shift register and the binary counter and generates sixteen control signals Ref_i and Gnd_i (i=0…7). The logic network was synthesized through Karnaugh's maps and designed by using static NOR and NAND CMOS logic gates.

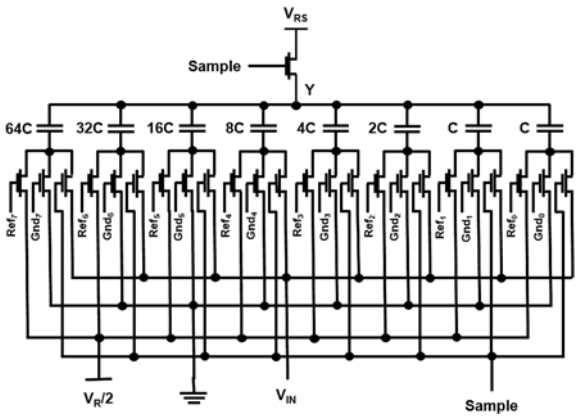


Fig. 7. Schematic of the DAC for the designed 8-bit SAR-ADC.

The comparator was designed as a dynamic latch, because of its higher sensitivity and lower dissipated power with respect to an operational amplifier based solution. Fig. 8 depicts the schematic of the designed dynamic latch comparator. Since the circuit is very sensible to capacitive mismatches at the output nodes, a dummy inverter was added at the output node of the comparator not connected to the DCL.

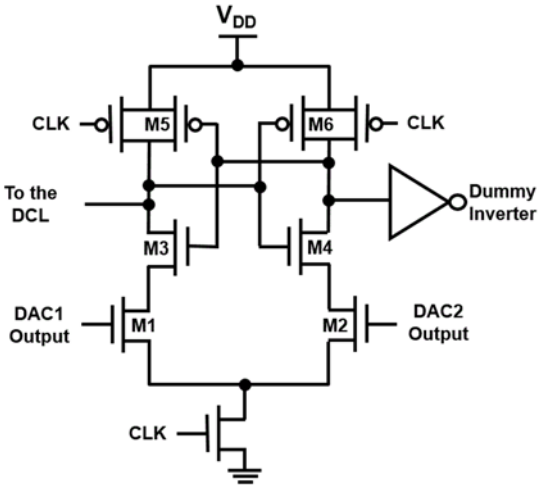


Fig. 8. Schematic of the dynamic latch comparator.

5. Simulations

As a first simulation, a sinusoidal tone with an amplitude of 800 mVpp and an oscillation frequency of 70 Hz was applied at the input of the designed SAR-ADC. The sampling frequency was set equal to 1.4 kS/s, the clock signal to 12.5 kHz, and V_{REF} to 800 mV. The following Fig. 9 shows a 12 ms time interval of the input signal. The figure highlights on the input waveform six samples (samples #2, #6, #9, #11, #13 and #16), whose values are reported in Table 1. Fig. 10 shows how the output bits are generated during the time for each of the previous six samples.

For example, the input sample #2, sampled in correspondence of the sampling pulse #2, is digitized during the time interval between this sampling pulse and the following sampling pulse #3. The output bits are made available in correspondence of the rising edge of the sampling pulse #3. It is therefore visible a latency time, spent by the DCL for exploring the binary tree (see Fig. 2) during the digitization process.

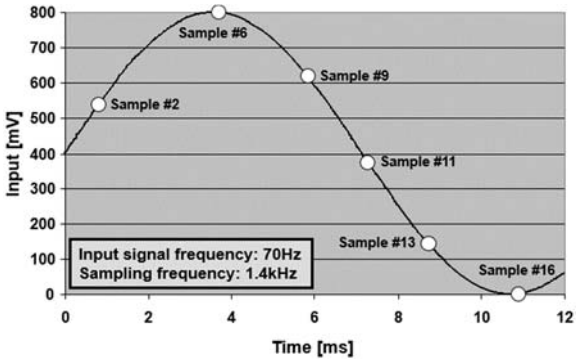


Fig. 9. Sampled values on the input sinusoidal waveform.

Table 1. Output words and quantization error.

Sample	V_{IN}, (mV)	Output Word	V_A, (mV)	ΔV, (mV)
#2	537.790	10101100	537.50	0.29
#6	799.560	11111111	796.88	2.69
#9	617.310	11000101	615.63	1.69
#11	374.780	01111000	375.00	0.22
#13	143.500	00101110	143.75	0.25
#16	1.120	00000000	0.000	1.12

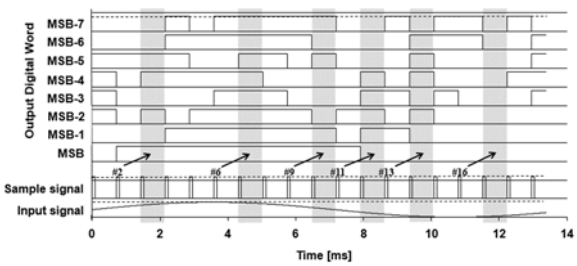


Fig. 10. Generation of the output digital word.

Table 1 reports also the voltage V_A computed from the output digital word using the usual formula:

$$V_A = V_{REF} \sum_{i=0}^{7} \frac{MSB - i}{2^{i+1}}, \qquad (1)$$

where MSB-i is the i[th] output bit, being MSB-0 the MSB and MSB-7 the LSB. The most-right column in Table 1 shows the quantization error ΔV between V_{IN} and V_A. It is possible to observe that ΔV is always lower than one LSB (3.13 mV). Table 1 provides therefore a first rough indication that the designed SAR-ADC is correctly working.

The performances of the designed SAR-ADC were more in depth tested by investigating the static parameters Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), and the dynamic parameters Equivalent Number of Bit (ENOB), Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), and Signal-to-Noise And Distortion ratio (SINAD), as well. The simulation set-up employed for these parameters are shortly sketched in the following Fig. 11. The ideal DAC was described in Verilog-A code. For INL and DNL (upper part of the figure) a slow linear voltage ramp covering the whole input dynamic range was applied at the input of the SAR-ADC under test. The stair-case ramp generated by the Verilog-A code DAC was analyzed in the time domain by investigating the distribution of the thresholds. The following Fig. 12 and Fig. 13 show the obtained DNL and INL, respectively.

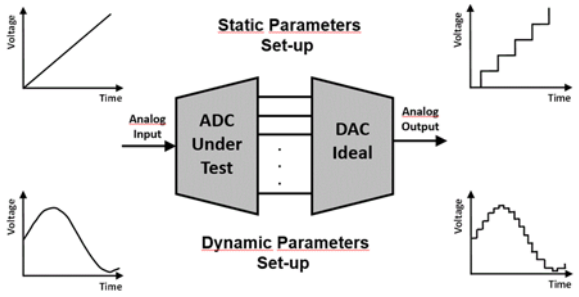


Fig. 11. Simulation set-ups for static and dynamic parameters of the SAR-ADC.

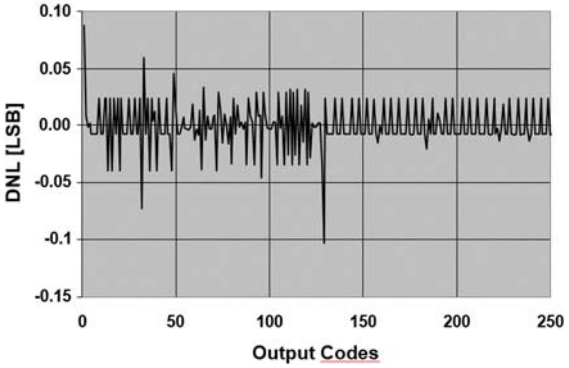


Fig. 12. Differential Non-Linearity of the designed SAR-ADC.

The DNL oscillates in the +/-0.05LSB range with exception for the code #128, where it exhibits a peak at around -0.1LSB. The worst DNL can be indeed expected when the MSB changes [7]. The INL is in the -0.15LSB/+0.10LSB range with a step in correspondence of the worst DNL.

For ENOB and SNR (lower part of Fig. 11) a 70 Hz sinusoidal tone was applied at the input and the stair-case waveform generated by the ideal DAC was analyzed in the frequency domain with a Discrete Fourier Transform. The following Fig. 14 shows the spectrum. The summation of the first eleven harmonics leads to a THD of 45.9 dB. By accounting for the process gain from the noise floor it is possible to compute a SNR of about 42.9 dB.

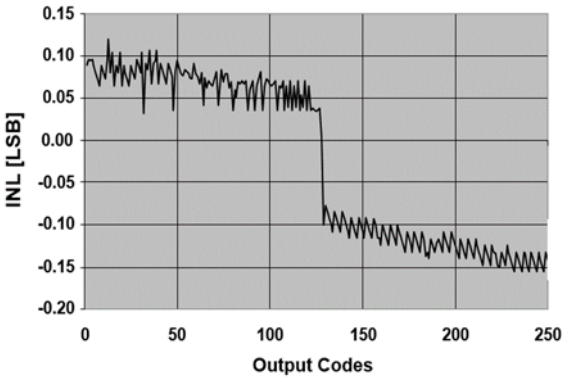


Fig. 13. Integral Non-Linearity of the designed SAR-ADC.

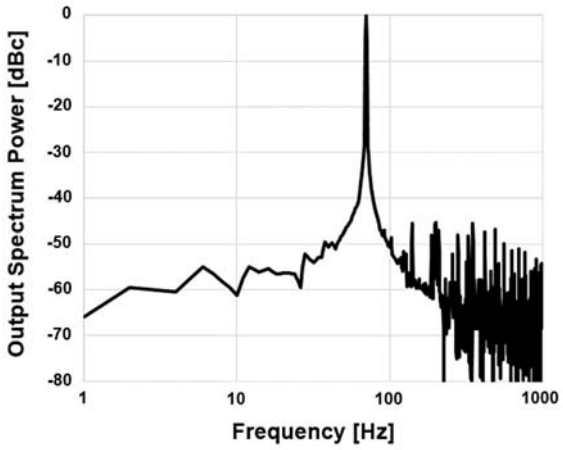


Fig. 14. Spectrum of the stair-case sinusoidal tone generated by the ideal DAC in the simulation set-up for dynamic parameters.

The following Equation (2) allows for computing the SINAD:

$$SINAD = -10log\left(10^{-\frac{THD}{10}} + 10^{-\frac{SNR}{10}}\right), \qquad (2)$$

which results to be 41.2 dB. Finally, through the following Equation (3) it is possible to compute the ENOB:

$$ENOB = \frac{SINAD - 1.76}{6.02}, \quad (3)$$

which results to be 6.5 bits.

THD can be also estimated from the INL through the following Equation (4) [8]:

$$THD = 20log \frac{INL_{MAX}}{2^{N-1}}, \quad (4)$$

where INL_{MAX} is the maximum observed module of INL and N is the number of bits. Since INL_{MAX}=0.15LSB from Fig. 13 and N=8 for the designed SAR-ADC, the equations from (2) to (4) provide therefore an ENOB of 6.8 bits. It is therefore possible to estimate an ENOB of 6.65 bits for the SAR-ADC proposed in the present work.

Table 2 compares the obtained DNL, INL and ENOB with those reported of other 130 nm CMOS SAR-ADCs in the literature. The present SAR-ADC well compares with the literature even if it suffers from a somewhat low ENOB.

Table 2. Output words and quantization error.

	[9]	[10]	[11]	This work
Resolution [bits]	8	10	8	8
DNL [LSB]	+/- 0.61	-0.61 / +0.54	-0.15 / +0.15	-0.05 / +0.05
INL [LSB]	+/- 0.63	-0.46 / +0.45	-0.35 / +0.23	-0.15 / +0.10
ENOB [bits]	7.6	9.1	7.8	6.7

The following Fig. 15 plots the dissipated power versus the sampling rate for several SAR-ADC collected in the literature regardless of the employed technology. The two dashed lines in the figure suggest that the power dissipated (P_D) by the SAR-ADC increases of 10 dB when the sampling frequency increases of one decade. Fig. 15 shows that the SAR-ADC proposed in the present work (open symbol in the figure) well compares with the literature.

A more homogeneous comparison with the state-of-the-art in the literature can be carried out through the following Figure-of-Merit (FoM) [11], [14]:

$$FoM = \frac{P_D}{f_s 2^{ENOB}} \quad (5)$$

It quantifies the energy dissipated to complete a conversion step. The following Fig. 16 plots this FoM versus the sampling rate for the SAR-ADCs already addressed in the previous Fig. 15. Even if with a FoM somewhat higher than the average value, the SAR-ADC described in the present work still remains comparable with other SAR-ADCs reported in the literature.

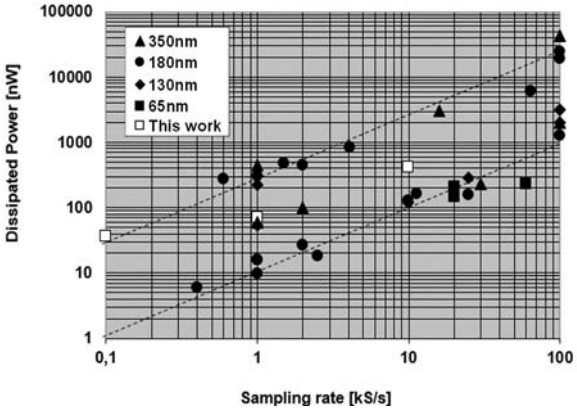


Fig. 15. Dissipated power versus sampling rate. References for 350 nm: [2], [12-16]. References for 180 nm: [2], [17-27]. References for 130 nm [10], [11], [28-31]. References for 65 nm: [32]

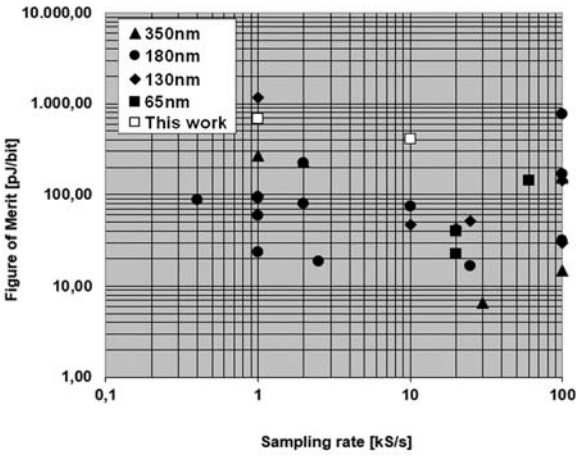


Fig. 16. FoM versus sampling rate. References for 350 nm: [2], [12-16] References for 180nm: [2], [17-27]. References for 130 nm [10], [11], [28-31]. References for 65 nm: [32].

6. Conclusions

The present paper proposes the design of a low complexity digital control circuitry for SAR-ADC. The elementary cell for the design of this control circuitry is a D-type register. The obtained control circuitry results to be of low complexity. It is indeed constituted by two chains of registers, whose lengths can be easily accommodated to the desired resolution.

The proposed digital control circuitry was applied to the design of an 8-bit resolution SAR-ADC in a 130 nm CMOS bulk technology. The simulations demonstrated that the designed SAR-ADC correctly works exhibiting performances well comparable with the literature in terms of DNL, INL, and dissipated power. The only weakness was the ENOB, which results to be less performant without nevertheless severely affecting the energy spent per bit generation that remains comparable with the literature.

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