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Fully Differential Operation Amplifier Using Self Cascode MOSFET Structure for High Slew Rate Applications

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Abstract: In this paper, an adaptive fully differential OPAMP using Self Cascode MOSFET Transistors giving a maximum differential gain 75.31 dB with slew rate of 14.58 V/µS has been presented. In comparison to conventional 2 stage operational amplifier design, proposed design with adaptive bias has slew rate increased by 7× for a capacitive load of 3 pF. An adaptive bias circuit with current reference circuit is also designed using Self Cascode MOSFET Transistors to get reference current varying by only 20 nA when temperature varies from 25ºC to 100ºC. A Common Mode Feedback circuit designed using Self Cascode MOSFET Transistors shows only 0.01 % variation in Vocm as Vicm varies by 1 V. The proposed OPAMP has been developed in a standard TSMC 0.18 µm CMOS technology and the simulations are done using Cadence software.

Keywords: Self cascode, Slew Rate, High DC Gain, Adaptive bias, Common Mode Feedback, Operational Amplifier, Current reference.

1. Introduction

The decrement of supply makes difficult to implement useful analog circuits, so novel circuit architectures have to be introduced. The values of the current sources inside the amplifiers are the main responsible of quiescent power dissipation. Adaptive bias boosts the bias current of the input differential pair when large signals are applied, thus increasing circuit dynamic characteristics without affecting stand-by dissipation. In this paper we propose a novel rail-to-rail fully differential self cascode (SC) operational amplifier (OPAMP), showing enhanced gain characteristics, where DC gain has been enhanced by a technique which increases the output impedance of the OTA input stage through a regenerative feedback [1-2].

Fig. 1 shows the variation of Rout with length of M1 in SC, where "Ls" and Ld are transistor lengths for M1 and M2 respectively in SC already published in [2] but reproduced here. Using this a highly optimized SC can be obtained by just varying the length of M1 resulting in maximum gain of OP AMP. SC is also used in the design of current mirrors in this paper.

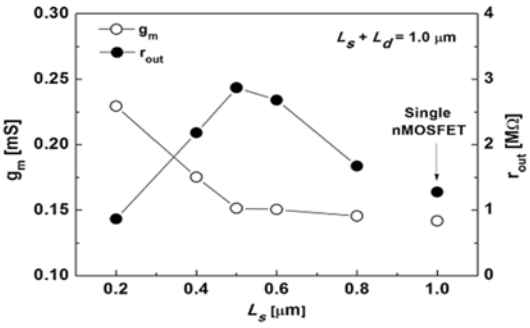


Fig. 1. Variation in Gm, and Rout of SC with variation in Ls and Ld [2].

2. Design Methodology

2.1. Self CascodeTransistor

Fig. 2 shows an NMOS SC configuration with gates shorted together and width of upper transistor is **m** times the lower transistor where **m**>>1. Length can be adjusted between the two so as to get the optimized trans-conductance gm_{eff} and output résistance R_{out}. For this design, Ln=400 nm (for M1) and Ln=600 nm (for M2) transistor.

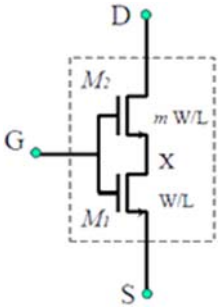


Fig. 2. Self Cascode Transistor.

Fig. 3 shows that gm_{eff} of SC increases with decrease in length but its R_{out} increases. Hence, an optimum value for gm_{eff} and r_o needs to be found out which will provide highest gain as compared to non SC transistor. Similar but complementary setup is made and used for pMOS transistors.

For a V_{DS} varying from 0 to 3.3 V, 'gm_{eff}' graphs are plotted in Fig. 3. As observed in simulations, gm_{eff} and R_{out} are functions of length of M1 transistor.

Fig. 4 shows circuit for computing equivalent resistance R_{out} of SC. Equivalent trans-conductance 'gm_{eff}' and R_{out} of SC are as computed below in Eq. (1) and (2).

$$R_{out} = (g_{m2}r_{o2}r_{o1} - r_{o2} - r_{o1}) \approx (g_{m2}r_{o1} - 1)r_{o2} = (mg_{m1}r_{o1} - 1)r_{o2} = (m-1)r_{o2} \quad (1)$$

$$g_{meff} = \frac{g_{m2}}{m} = g_{m1} \quad (2)$$

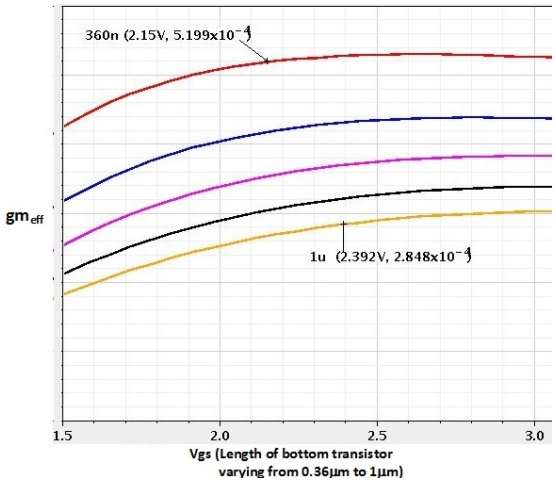


Fig. 3. Variation of gm_{eff} versus Vgs.

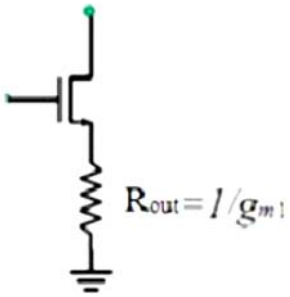


Fig. 4. Circuit for equivalent impedance of SC.

2.2. Operational Amplifier Schematic

Here, a positive feedback has been provided at the PMOS stage which gives us a gain increment of about 35 dB as compared to classical two stage cascode OPAMP at 1 MHz operating frequency.

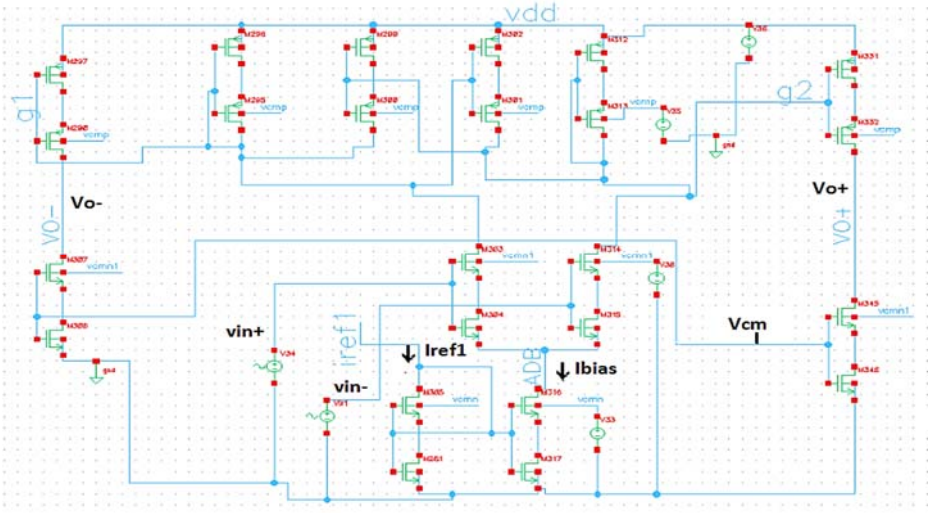


Fig. 5. Schematic design of proposed OPAMP [4].

Fig. 6, Fig. 7 and Fig. 8 shows frequency response of proposed OPAMP for differential mode gain (Adm), Adm with frequency compensation and common mode gain (Acm) respectively.

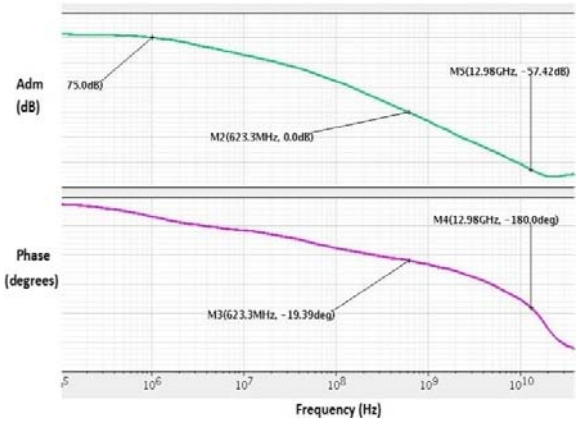


Fig. 6. Differential mode gain (Adm) of proposed design versus frequency.

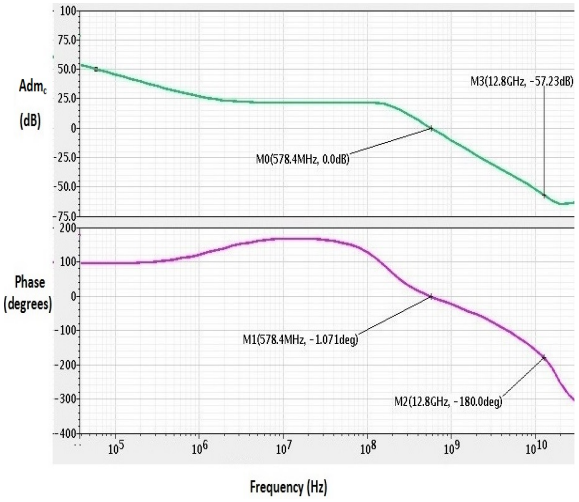


Fig. 7. Adm of proposed OPAMP with R-C miller compensation at second stage Vs. frequency.

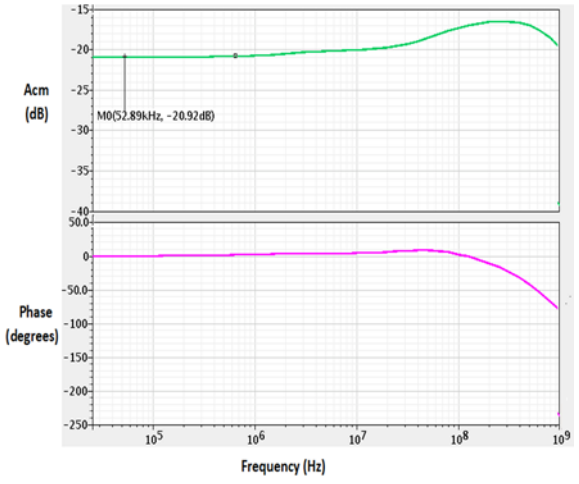


Fig. 8. Common mode gain (Acm) of proposed design versus frequency.

Table 1 shows the tabulated values of characterizing parameters of proposed and conventional OPAMP.

Table 1. Simulated values of characterizing parameters of proposed OPAMP.

No.	Parameter	Proposed Self cascode OPAMP Design	Conventional 2-stage CMOS OPAMP
1.	DC Differential Mode Gain, Adm, (dB)	75.31	40
2.	DC Common mode Gain, Acm, (dB)	-20.92	–
3.	CMRR (dB)	99.23	–
4.	Bandwidth (UGB) (MHz)	623.12	0.75
5.	Phase Margin (deg)	82	–
6.	PSRR (dB)	53.86	–
7.	ICMR (mV)	700	–
8.	OCMR (mV)	800	1000
9.	Slew Rate (58 V/μS)	14.58	2.3

2.3. Novel Current Reference Circuit Using SC

Typically CMOS reference current, Fig. 9 is designed using a CMOS Widlar source mirror and a passive resistor.

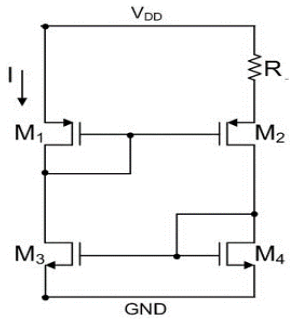


Fig. 9. Wildar reference current Generation [5].

The precision of the reference current depends on the complete value of the resistor. A slight variation in the resistor value can degrade the performance over temperature and process corners as current I is proportional to inverse of mobility and square of resistance. Since μp (mobility of pMOS) is a temperature dependent variable that reduces with temperature, the reference current 'I' *will increase with temperature.* Also, the mobility will change with carrier concentration, which makes the reference current sensitive to process variations too.

Thus in proposed OPAMP, a current reference is designed with only MOS transistors using SC as shown in Fig. 10 generating a 10 µA in each arms.

Here, instead of using resistor, a SC is replaced in linear region. PMOS Transistor pairs e.g. (M11, M12) in Fig. 10 is biased in deep triode region so that even if temperature increases, (M11, M12) remains in linear region. Thus a better stability with respect to temperature can be obtained by varying the W/L of Transistor pair (M11, M12).

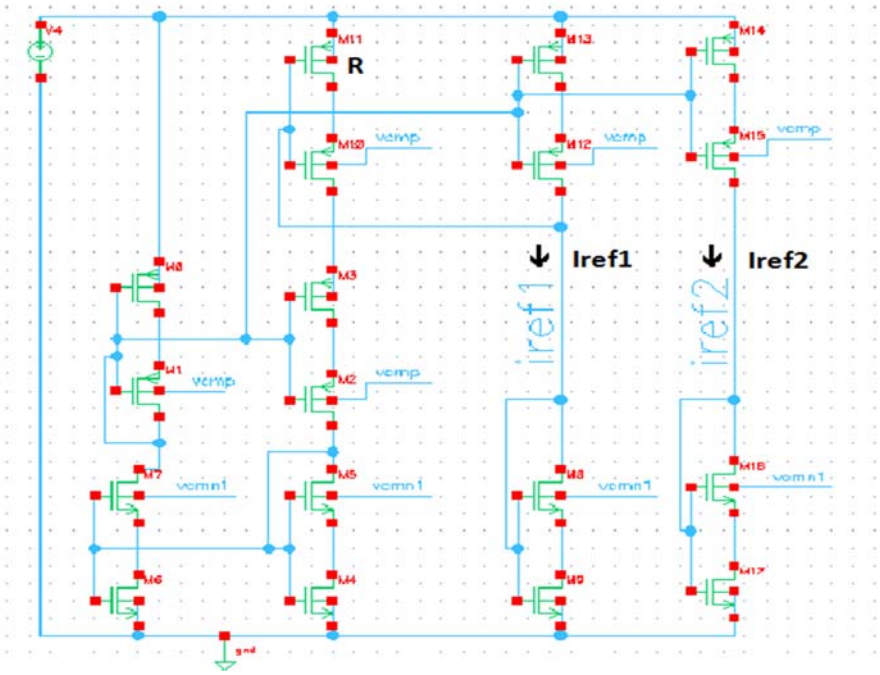


Fig. 10. Proposed current reference design using SC.

Fig. 11 shows the variation of only 0.02 uA in reference current I_{ref} with 50° change in temperature.

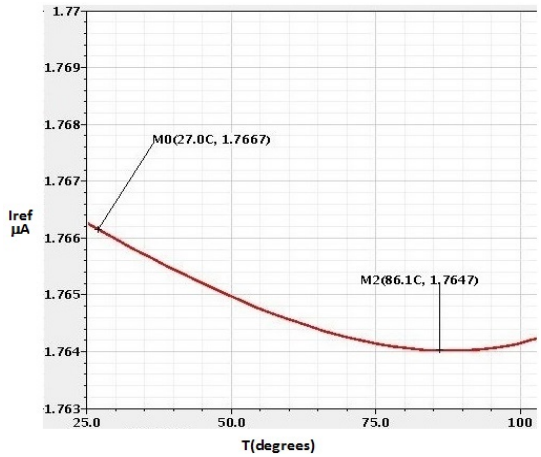


Fig. 11. Variation of reference current Iref w.r.t temperature.

2.4. Adaptive Bias Circuit

An adaptive bias circuit is designed for slew rate improvement. The circuit is shown in Fig. 12.

Basic current subtractor is realized in differential arms to provide extra current as seen from Eq. (4),

$$I_{total} = I_{bias} + A * \mathrm{mod}(I_2 - I_1) \quad (4)$$

I_1 and I_2 are current in branches close to main I_{bias} current mirror branch in differential tail branch.

$$I_{total} = I_{bias}(1 + A + A^2 + ...) \quad (5)$$

To ensure transistors to remain in saturation it is necessary to have value of parameter A<1 but not too less than 0.5 as it will reduce slew rate. I_{total} forms a geometric progression because of the positive feedback for A<1 as in Eq. (5).

For A= 0.9, current I shows 10 times improvement in slew rate as observed in Fig. 13 and Fig. 14.

2.5. Common Mode Feedback Circuit

Common mode feedback circuit is designed to maintain stable DC value at output, which will stabilize from process variations. CMFB senses voltage Vout should remain constant with V_{CM} variations. This is achieved by adjusting the current of Ibias, i.e. supplying it whenever needed to maintain constant Vocm. Instead of using resistive sensing, we have used all SC in implementation of CMFB [6] as shown in Fig. 15.

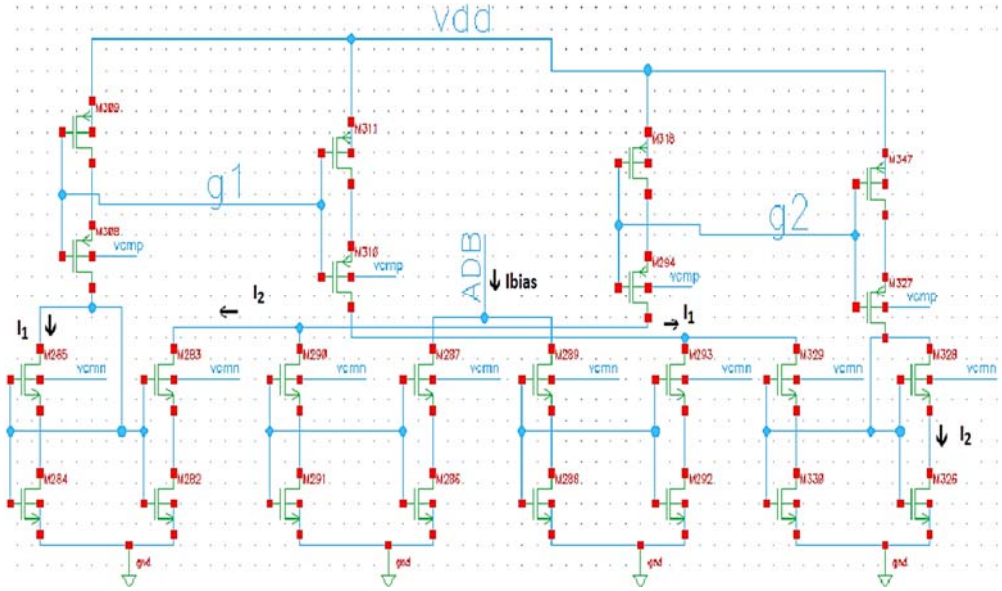


Fig. 12. Adaptive bias circuit [4].

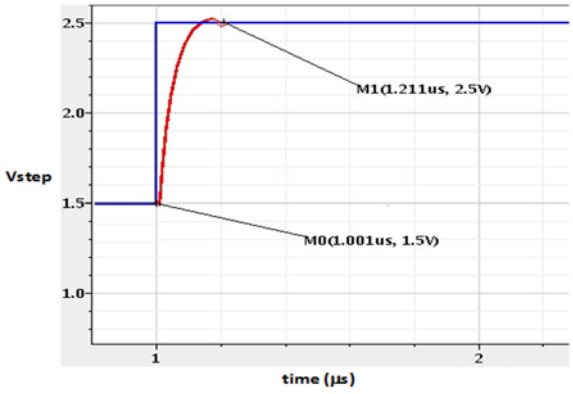


Fig. 13. Step voltage response of proposed OPAMP with time without adaptive bias, Slew Rate =2.3 V/µS.

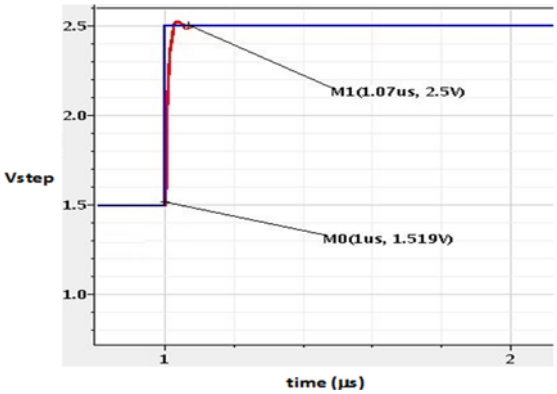


Fig. 14. Step voltage response of proposed OPAMP with time with adaptive bias, Slew Rate =14.58V/µS.

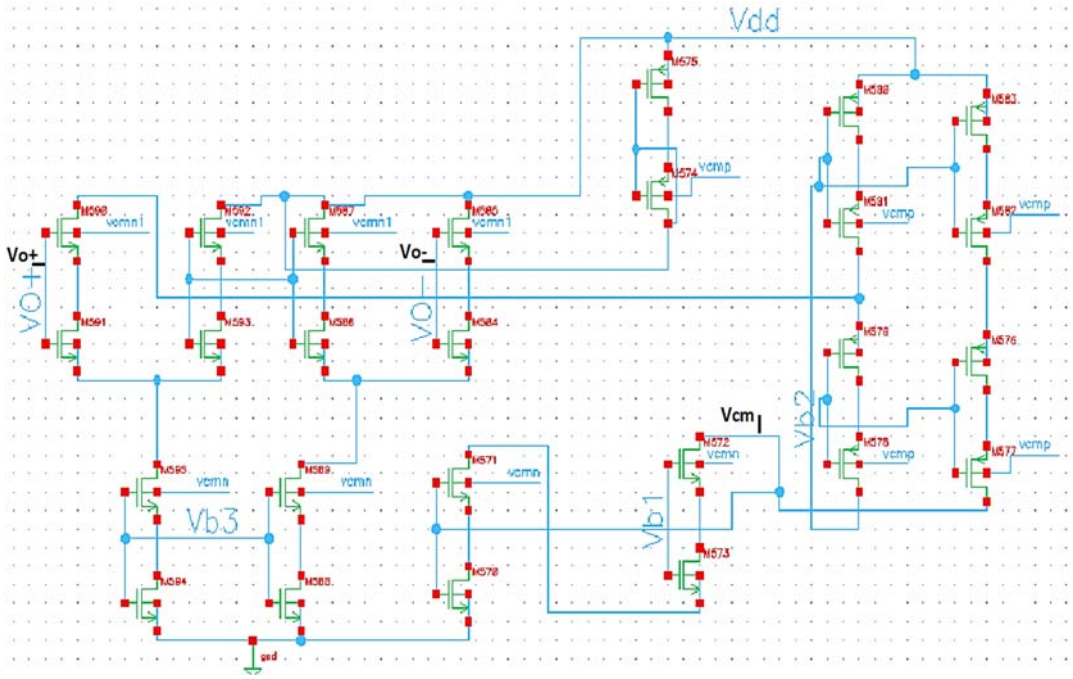


Fig. 15. Common Mode Feedback Circuit (CMFB) circuit.

As observed in Fig. 16, CMFB circuit tries to level the output to a constant value, within 0.01 % for Vicm varies from 1.5 to 2.5 V in differential mode operation.

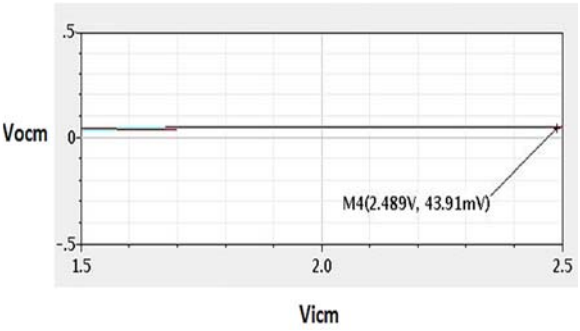


Fig. 16. Variation of Voutcommon mode (Vocm) w.r.t input common mode voltage Vicm varying from 1.5 to 2.5 V.

3. Conclusion

This paper presents a high performance 2 stage OPAMP design using SC based on the concept of dual-work function gate devices. Both the trans-conductance gm_{eff} and output resistance 'R_{out}' are optimized by channel length ratio of the SC MOSFETs. SC MOSFETs optimized for trans-conductance and output resistance are utilized in both input differential and output stages of the OPAMP. The DC gain improvement has been achieved by using partial positive feedback technique. This technique improves gain and bandwidth of the circuit. The measured DC gain of the proposed OPAMP is 35 dB higher, and slew rate is 7 times higher than that of the conventional 2 stage cascode OPAMP.

The proposed OPAMP has a power efficient high DC gain adaptive bias circuit which utilizes current subtractor based on CCM for providing extra tail current sources in addition to fixed bias current sources. The current subtractor provides the variable bias i.e. adaptive biasing, in the presence of input signal by providing additional bias current when the large signal is applied. The proposed circuits can be widely used in various signal processing applications such as filters, data convertors, resistors, inductors, integrators etc.

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