Sensors & Transducers, Vol. 227, Issue 11, November 2018, pp. 15-20

www.sensorsportal.com

Sensors & Transducers

Published by IFSA Publishing, S. L., 2018
http://www.sensorsportal.com

Behavior Analysis of a Simultaneous Read/Write Nanoelectronic SRAM

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Received: 31 July 2018 /Accepted: 28 September 2018 /Published: 30 November 2018

Abstract: This work presents and analyzes a fully working single-electron transistor (SET) based SRAM with individual read and write addressing for simultaneous operation. The SET-based SRAM presents smaller area, lower power consumption and lower latency time, making it ideal for devices with small area and low power consumption demands such as Systems-on-Chip (SoCs).

Keywords: SRAM, SET, Nanoelectronics.

1. Introduction

The capability of storing and retrieving large amounts of information is essential for most modern digital systems. The structured storage of bits, usually as a two-dimensional array, is defined as a memory [1]. One of the types of memories used in modern systems is the Random-Access Memory (RAM). The RAM is a volatile read/write memory in which the access time for read and write operations is independent of the data location in the memory array. The Static RAM (SRAM) is a type of RAM in which the written data remains stored while there is power applied to the system.

Area and dissipated power are limiting factors in improving the performance of mobile and Systems-on-Chip (SoCs) devices [2]. About 70 % of the area of a SoC chip is occupied by the SRAM memory [3]. Using a nanoelectronic device instead of CMOS transistors within the SRAM could be the solution to these limitations.

Particularly the single-electron transistor (SET) present attractive features like reduced dimensions, extremely low power consumption and low noise behavior. Single-electronic devices are able to control the movement of individual electrons through the tunneling phenomenon, i.e., the nonzero probability that the electron will be transmitted through a potential energy barrier [4].

This work presents and further analyze a fully working nanoelectronic SRAM based on the SET transistor with individual read and write addressing [5].

2. Single-Electron Transistor

The SET consists of two tunnel junctions connected together, forming an island between them (Fig. 1) [6]. Its operation is based on the flow control of single electrons (or small groups of electrons) by tunneling. That leads to very low power consumption, noise and device dimensions. The gate voltage

manipulates the Fermi level, i.e., the highest energy level occupied on the island, thus controlling the electrons conduction through the transistor [7].

The disadvantages of the SET include low gain, high susceptibility to offset charges, and high temperature operation issues. However, the operation of SETs up to 350 K has already been reported [8]. In this work, a SPICE model for the SET, which operates at room temperature, proposed by and available at Lientsching, *et al.* [9] was employed.

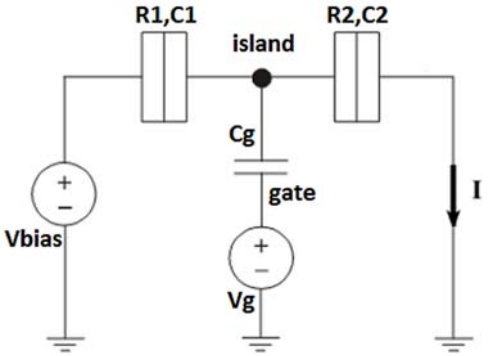


Fig. 1. Single-electron transistor.

3. SRAM Architecture

A generic SRAM architecture (Fig. 2) is composed of storing cells, read and write control, and address logic. The cells store 1 bit in a latch or flip-flop device and are usually arranged in a $m \times n$ matrix, where m corresponds to the number of arrays (words) that can be stored in the memory, and n represents the number of bits each array contains. They also contain the read/write logic that selects the operation to be executed, and a select control that enables the operation of each cell.

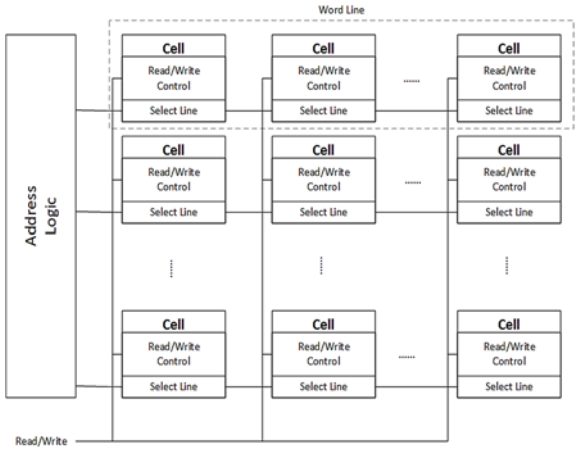


Fig. 2. Generic SRAM architecture.

The address logic allows each array of the memory matrix to be selected individually. As both read and write operations are controlled by one control, only one operation can be executed at a time, which generates a latency during the SRAM operation.

The developed SRAM module can store 8 words of 8 bits and presents separate controls for read and write addressing, allowing an individual and simultaneous execution of these operations (Fig. 3). The module is completely digital, and it can be combined with more modules to further expand the SRAM storage capacity.

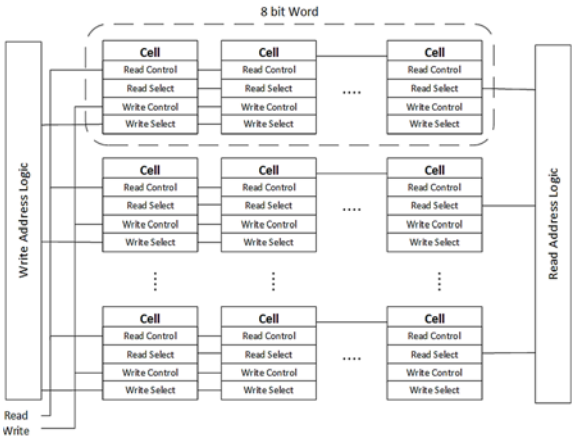


Fig. 3. Proposed SRAM architecture.

All the components of this digital architecture were designed with a nanoelectronic gate (nanoNAND) as base element (Fig. 4), which in turn is composed of SET transistors. All simulations were made using the LTSpice software [10]. Its building blocks are presented in the next subsections.

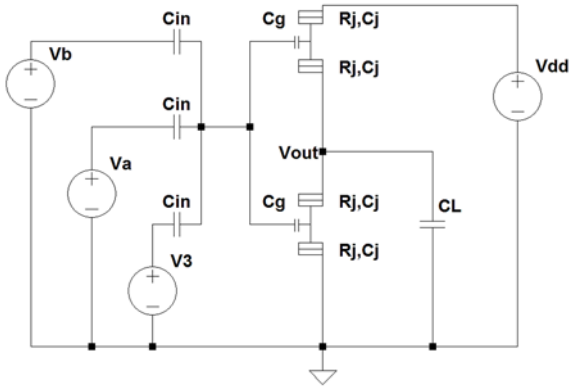


Fig. 4. Nanoelectronic NAND gate architecture.

3.1. Nanoelectronic NAND Gate

The NAND gate can be used to implement any Boolean function due to its functional completeness property. All the components of this digital architecture were designed with a nanoNAND as base element, including the NOT gate.

Various nanoNAND based on SET devices have been previously proposed in the literature [11-12]. The nanoNAND used in this work is the one redesigned at Silva, *et al.* [13] (Fig. 4). This choice was made because this specific nanoNAND configurations allows its simulation at ambient temperature. This nanoNAND is a programmable gate and its parameters are presented in Table 1.

In Fig. 4 voltages V_a and V_b are the inputs A and B of the digital signals. Voltage V3 is a select input that enables a NOR function on the output of the gate when its value is high (0.5 V) or a NAND function when its value is low (0 V). The nanoNAND is composed of two SET transistors.

Table 1. NanoNAND gate parameters.

Parameters	Value
R_j	1 MΩ
C_j	0.001 aF
C_{in}	2 aF
C_g	0.15 aF
C_L	0.25 aF
V_{dd}	0.5 V
V_3	0 V

3.2. SRAM Cell and Array

The SRAM cell consists of a flip-flop D, which can store 1 bit. The cells are arranged in an array of 8 bits, constituting a word. Each array consists of the 8 bits entries, a clock and an asynchronous clear, read and write signals to indicate the current operation and independent select signals for each operation, which are used by the addressing logic (Fig. 5).

In order for the read/write operation to occur in the m^{th} word, both the corresponding operation signal and operation address should be selected in the m^{th} array. Because it is possible to realize a simultaneous read and write operation in the same array, an unstable situation could be reached in the output. To avoid this problem both operations are also regulated by the system's clock. The write operation is executed only during the rising of the clock signal, while the read operation is executed when the clock signal is low.

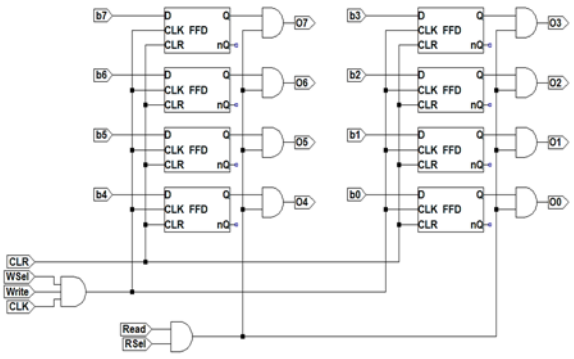


Fig. 5. SRAM array.

3.3. Read and Write Addresses

Because the proposed SRAM contains 8 memory arrays (words), read and write addressing are done through separated 3 to 8 decoders. An array address is then a 3-bit number that should be input in the corresponding operation decoder.

4. Simulation

The simulations were done through the software LTSpice. In this phase a test was presented to evaluate the correct functioning of the SRAM. The test consisted of writing two different 8-bit words on address 3 and 7 (Table 2), respectively, and retrieving them later.

The simultaneous read/write feature was also assessed during the test. Table 3 presents a timetable for when the write and read actions occurred and what addresses they accessed.

Table 2. Words for SRAM testing.

Add.	b7	b6	b5	b4	b3	b2	b1	b0
3	1	0	0	1	0	1	1	1
7	1	1	0	1	1	0	0	1

Table 3. Read/Write actions timetable.

Time (ms)	Write Action	Write Address	Read Action	Read Address
0 – 0.5	1	3	0	-
0.5 – 1	0	-	1	3
1 – 1.5	1	7	1	7
1.5 – 2	0	-	1	7

5. Results

The results of the test presented during simulation shows that the nanoelectronic SRAM works correctly. The write, read, addressing and simultaneous read/write functions perform as expected, as shown on Fig. 6.

The complete nanoelectronic SRAM has a total of 1890 nanoNANDs. The area of 1 nanoNAND is 172 nm² and 3.5 pW [13] and its dissipated power can be calculated by using equations 1 to 3. The total dissipated power is given by the sum of the static and dynamic powers. Table 4 presents the values for area and dissipated power for 1 nanoNAND, 1 array (word), 1 decoder, and the complete SRAM.

$$P_{dissipated} = P_{static} + P_{dynamic}, \quad (1)$$

$$P_{static} = V_{dd} \times I_{max}, \quad (2)$$

$$P_{dynamic} = f \times {V_{dd}}^2 \times C_L \quad (3)$$

The complete SRAM has an area of 0.325 μm² and dissipates 6.6 nW, which highlights the advantages of a nanoelectronic SRAM.

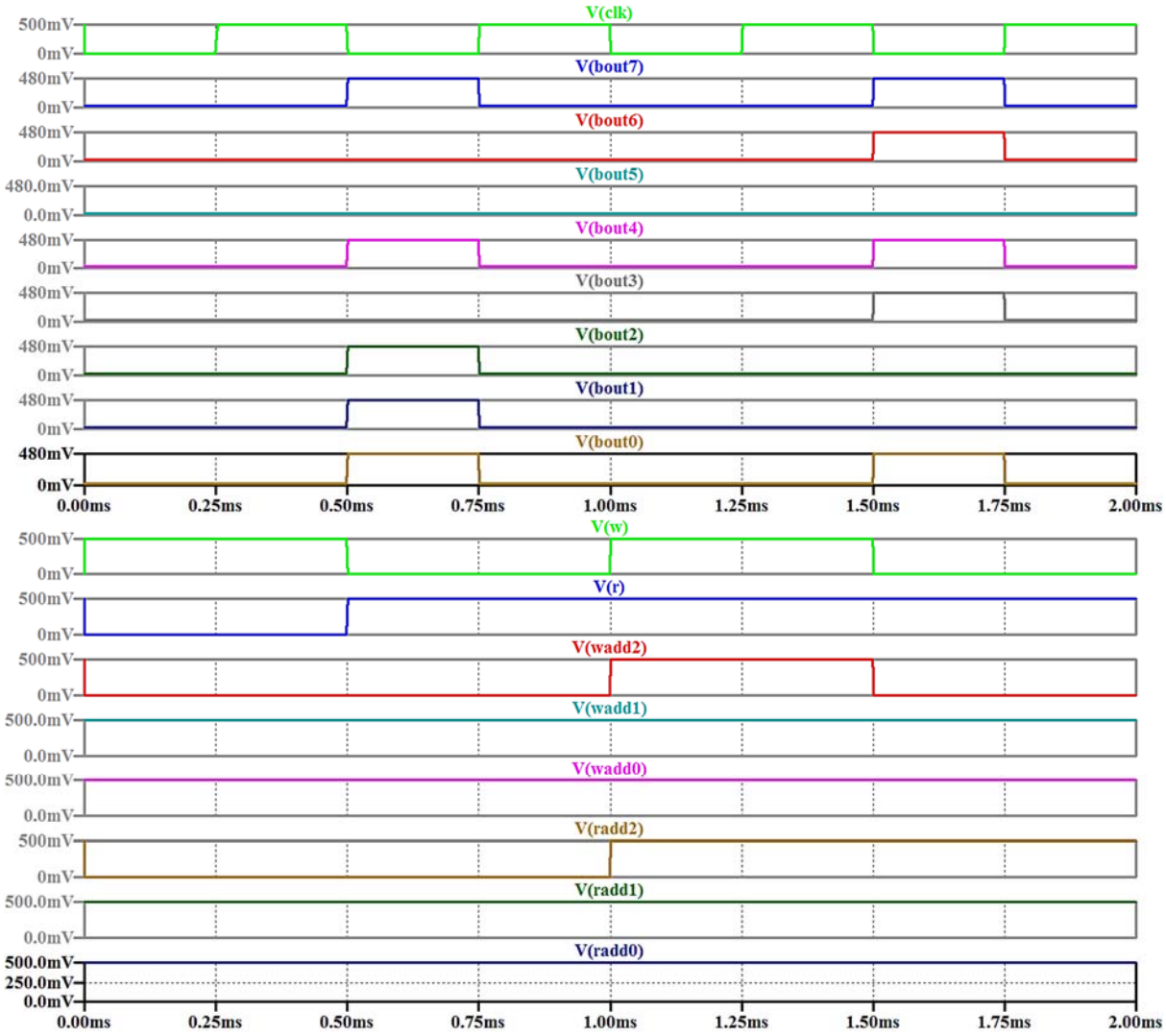


Fig. 6. SRAM Simulation.

Table 4. SRAM area and dissipated power.

	#SET NAND	Area	Power
nanoNAND	1	172 nm²	3.5 pW
Array	206	35432 nm²	721 pW
Decoder	37	6364 nm²	129.5 pW
SRAM	1890	0.325 µm²	6.6 nW

A preliminary noise margin analysis for the nanoelectronic SRAM includes temperature and background charges influences. The temperature noise analysis was achieved by varying the operation temperature between 270 K and 330 K and observing both the input (V_i) and output (V_o) voltage levels. The V_o x V_i characteristic plot for varying temperatures is shown on Fig. 7. Fig. 8 shows the upper part of the plot with zoom in.

It is visible that higher temperatures do influence somewhat the device behavior. However, this influence is not great given that for 30 K temperature variation, alters the output voltage at 0.5 %. This analysis does not include any background charge.

The background charges analysis was obtained by the inclusion of random background charges in the SET's islands during the simulation. The amount of charges was varied between 0 % and 20 % of the elementary electron charge. During this analysis the device temperature was kept constant at 300 K. The results are shown on Fig. 9.

The insertion of random background charges shifts the high/low level transition of the device to the right. As shown in the graph, up to 10 % of random charges is not only tolerable, but also beneficial for the device, since it brings the noise margin closer to ideal values. The graph also shows that the nanoNAND employed in this work is more robust against random background charges, which happens because its architecture is original, i.e., it is not a copy of the CMOS-based NAND gate architecture [14].

6. Conclusions

This work presented, validated and analyzed the proper working of a completely nanoelectronic

SRAM. This approach solves the area and power consumption limitations that current applications face. Also, the architecture provides the possibility of a separate read and write addressing, allowing for more versatile applications with lower latency time for the memory.

Acknowledgements

The authors would like to thank CAPES, PQ/CNPq and INCT-NAMITEC for support.

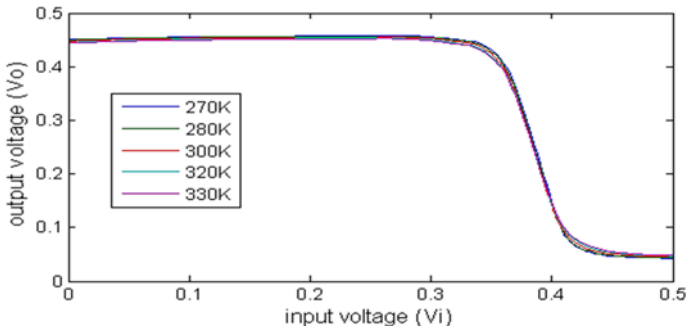


Fig. 7. Characteristic VoxVi transfer curve for varying temperature.

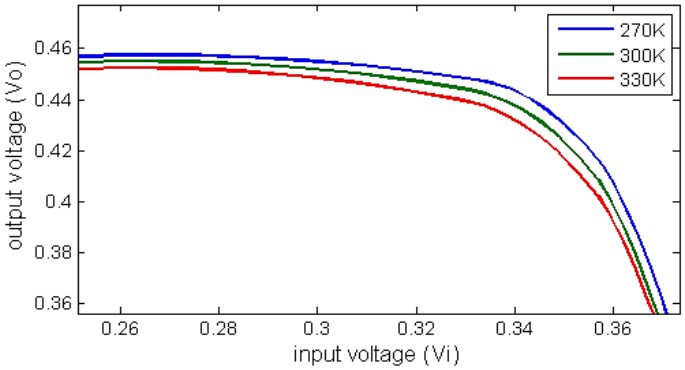


Fig. 8. Zoom of the characteristic curve.

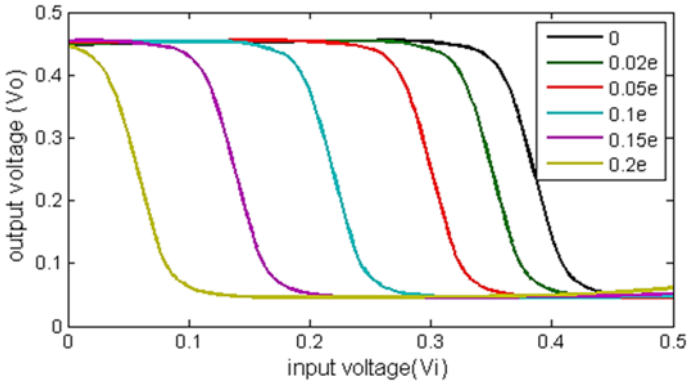


Fig. 9. Characteristic curve plot for varying random background charges percentage.

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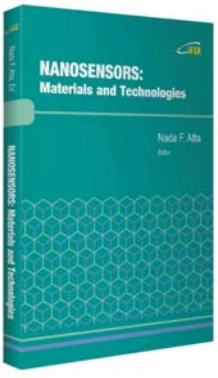
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Published by International Frequency Sensor Association (IFSA) Publishing, S. L., 2018 (http://www.sensorsportal.com).

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Hardcover: ISBN 978-84-616-5378-2
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