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MIS Transistor with Integrated Waveguide for Electrophotonics and the Effect of Channel Length in Light Detection

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Abstract: In this work, we study the optical response of MOS-like transistors with a Si_3N_4 integrated waveguide which serves also as the dielectric of the gate, and P-type substrate with 1×10^{12} cm^{-3} acceptor concentration and different channel length. Simulation results show the possibility to integrate this kind of MIS transistor as detectors in an electrophotonic circuit compatible with CMOS fabrication process and obtaining electrical gain for low power light signals (below 400 nW).

Keywords: Electrophotonics, Integrated photonics, Planar waveguide, Si photonics.

1. Introduction

Silicon photonics studies the generation, transmission, modulation, processing and detection of light using silicon-based materials as optical media. The application of photonics in silicon shows great potential to overcome the limitations of metallic interconnections such as transmission speed, heating losses, noise, crosstalk, which have impacted the performance of integrated circuits as the integration scale increases. In addition, silicon photonics has been widely used in optical sensors of chemical or biological type where it has had an increasing impact, due to the lower manufacturing costs of planar silicon technology given the abundance of the base material and the maturity of fabrication processes and infrastructure for this technology [1-4].

Although it has already been possible to perform optical operations on silicon chips, one of the important limitations for the widespread of the technology is the lack of light sources made of silicon. As it is well known, silicon is an indirect band semiconductor and therefore a poor emitter of light. Because of this, the technology is usually forced to couple external light sources to the silicon photonic chips, as such sources are incompatible with the fabrication processes of the rest of the photonics. However, from the observation of light emission from materials such as Silicon Rich Oxide (SRO) and implanted oxides, light emitters compatible with silicon technology and can be integrated into these chips have been developed [5-9], resulting in the arise of a new research area called electrophotonics.

Electrophotonics seeks to integrate operations that involve both electrons and photons simultaneously in monolithic silicon chips. In its simplest form, an electrophotonic circuit consists of three main elements: a light source, a waveguide that transmits the light and a photodetector. The procurement methods employ process techniques that include complementary metal-oxide-semiconductor (CMOS)

circuit technology and technologies such as silicon on insulator (SOI).

Applications in chemical or biological sensors called lab-on-a-chip could use the advantages of developing fully integrated silicon electrophonic chips. Although the development of optically pumped silicon lasers with silicon nano crystals has recently been reported, they are still far from being integrable in these circuits [10], and the silicon compatible light sources available have low optical powers compared to non-compatible ones.

To improve the efficiency of these systems, light detectors with high sensitivities must be used. In the past, light sensors made with SOI and MOS-based heterostructures have been proposed, but the application and detection schemes are not suitable for electrophotonic chips with integrated light sources and have mostly been designed for applications with high intensity luminous (laser), which are not fully integrable in CMOS technology [2, 11-13]. Nevertheless, considering the restrictions imposed by the light source power, one way of dealing with them is to integrate multiple light sources distributed within the chips, as opposed to having only a single light source. This is actually enabled by the possibility of fabricating the light emitter in the same process. Electrophotonic systems have already used light sources with relatively low light output (below 500 nW) and have demonstrated their operation [14-16]. Exploiting the advantages of direct light emitter and waveguide integration, new approaches using the direct coupling of these two elements and the detector (a unique feature of electrophotonics) have been then introduced, including devices with MOS and bipolar technology that merge waveguides and detectors to obtain electrophotonic photosensing devices [17-18]. Nevertheless, the close interrelation of all the components, and the restrictions imposed by CMOS processes call for very good knowledge of the influence of fabrication parameters for a proper design of the new photodetectors.

In this paper, a MOS-like transistor with an integrated waveguide is proposed as a highly sensitive photodetector for electrophotonic applications. The device is studied through computer simulation. The dielectric material in the transistor is replaced by silicon nitride, which is simultaneously used as the waveguide conducting the light directly to the channel region below the metallic gate, having effectively an electrophotonic metal-insulator-semiconductor (MIS) structure. The goal is to identify the channel length effects on the electrical gain of optical signals with power below 400 nW injected directly from the gate area in order to move forward in.

2. Device Description and Simulation Conditions

The proposed structure consists of a channel n Metal-Insulator-Semiconductor (MIS) transistor in which the insulator is made with silicon nitride. This is at the same time the core of the waveguide which will transmit the light produced by the light emitter in an electrophotonic emitter-waveguide-detector scheme [14]. Fig. 1 shows a transversal cut along the transistor structure, which was simulated using the Athena – Silvaco TCAD platform [19-20]. The selected substrate was crystalline silicon with [100] orientation. The boron substrate doping concentration was 1×10^{12} cm^{-3}. Drain and source regions were obtained using phosphor ion implantation and a thermal annealing at 1100 °C for 180 min. The waveguide/insulator silicon nitride film was obtained using chemical deposition, and its thickness 140 nm. The metal for the contacts is aluminum with a thickness of 1 µm. The substrate contact is achieved through the back of the substrate. The proposed lengths of the channel (L) for this study were 40 µm, 20 µm and 10 µm. The transistor width (W) was normalized at 1 µm.

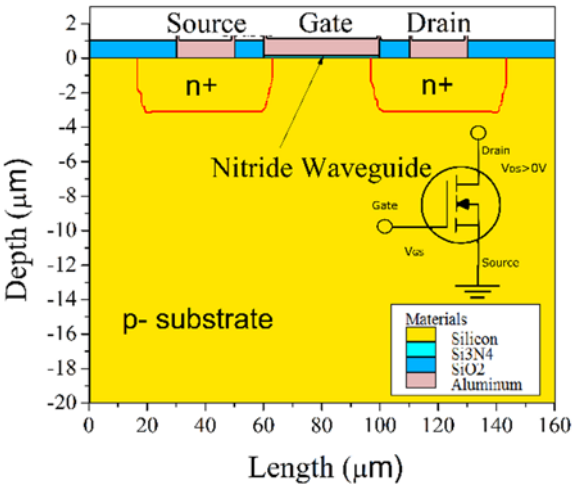

Fig. 1. MIS Transistor Structure Proposed.

Electric and optical simulations were performed using Atlas-Silvaco [20]. The drain voltage was fixed to 5 V, source and substrate was fixed to 0 V and different gate voltage (VGS) values were studied. A uniform monochromatic light beam was applied from the gate dielectric in normal direction towards the substrate, with 600 nm wavelength (λ) and optical powers (Pin) varying from 0 nW (dark) to 400 nW, simulating light transmitted by the nitride waveguide directly to the channel region.

3. Simulation Results

3.1. Electrical Simulations

Fig. 2 shows the drain current at dark condition (I_{Ddark}) as a function of V_{GS} for three transistors with different channel lengths for the fixed drain voltage value (5 V).

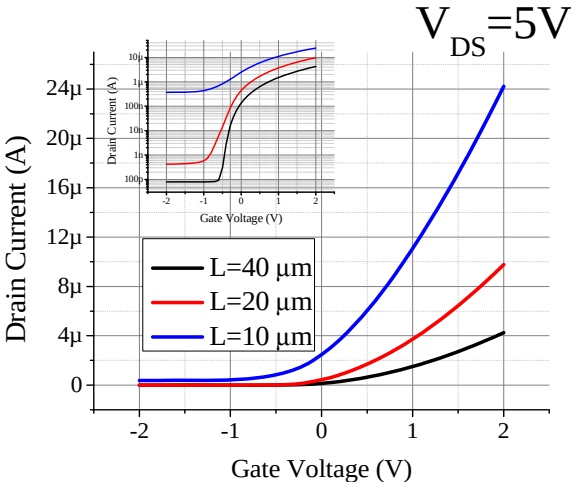

Fig. 2. Drain Current of MIS transistor at dark condition. Threshold voltage is negative below V_{gs}=-0.36 V. I_{Ddark} tends to increase when the channel length is reduced.

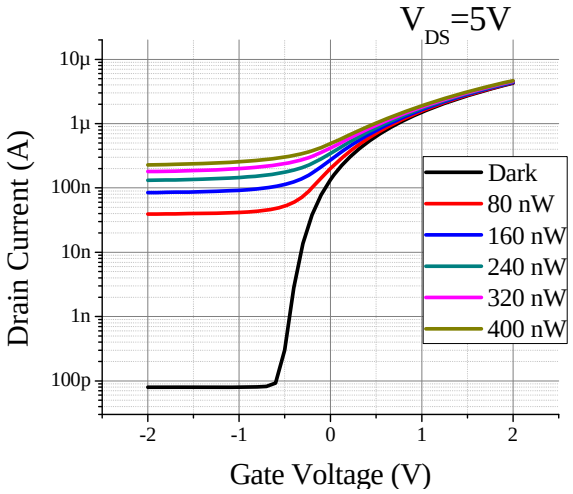

Fig. 3. Drain current under illumination. L is 40 µm. λ is 600 nm and drain voltage is 5 V. The presence of light increases the drain current values.

The curves have the characteristic quadratic behavior. The threshold voltages for these transistors has negative values. This means that they operate in depletion mode, for 0 V in the gate, the transistor is turned on (a channel is formed). Threshold voltages are around to -0.36 V.

It is observed that the dark drain current (leakage current) increases when the channel length is decreased for the applied drain voltage. There is a difference of three orders of magnitude between the longest transistor and the shortest one. This means that the transistor with 10 µm channel length requires a higher gate voltage to be turned off. This leakage current could be decreased using lower drain voltages.

3.2. Optical Simulations

Fig. 3 shows the drain current under different illumination conditions for the transistor with 40 µm channel length. The value of λ= 600 nm was selected according to the emission spectra of previously reported SRO-based light sources embedded into nitride waveguides [14].

The presence of light increases the drain current values in whole gate voltage range. This means that the drain photo detection is independent of the gate bias condition, but the amount of photocurrent could depend on the gate bias value. The current value difference between dark condition and 80 nW illumination is approximately 400 times when the transistor is turned off.

In order to show only the drain current contribution due to the optical power, the dark current was subtracted from the total drain current I_D. The optical drain current is:

$$I_{Dopt} = I_D - I_{Ddark}, \quad (1)$$

where I_D is the total drain current and I_{Ddark} the drain current in dark condition.

Fig. 4 shows I_{Dopt} for different gate voltages and different light power stimulations (from 80 nW to 400 nW) for the MIS transistor with 40 µm channel length.

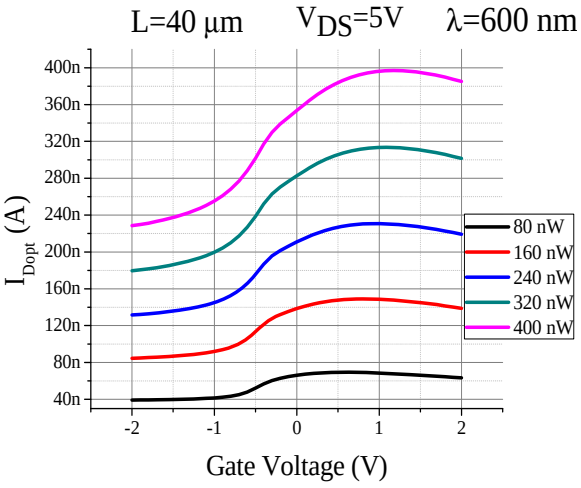

Fig. 4. Optical drain current as a function of gate voltage. L is 40 µm. λ is 600 nm and drain voltage is 5 V. Optical drain current is generated in whole gate voltage range.

It is observed that the optical drain current has a modulation effect dependant on the gate voltage. The optical drain current is increased when the gate voltage is biased towards higher voltages for the same light power value, until reaching a maximum value and then decresing again, although always to higher values as compared to V_{gs}<-0.5 V biasing of the gate.

Fig. 5 shows the optical drain current for different gate voltages and different light power for the MIS transistor with 20 µm channel length.

In this case, the optical drain current varies between 200 nA and 900 nA for the range of applied optical powers, which is lower than the variation

registered for L=40 µm, in which the change was of one order of magnitude. The optical drain current has its maximum photo detection values around V_{gs}=-0.5 V and is decreased when the gate voltage moves away from this voltage to larger values.

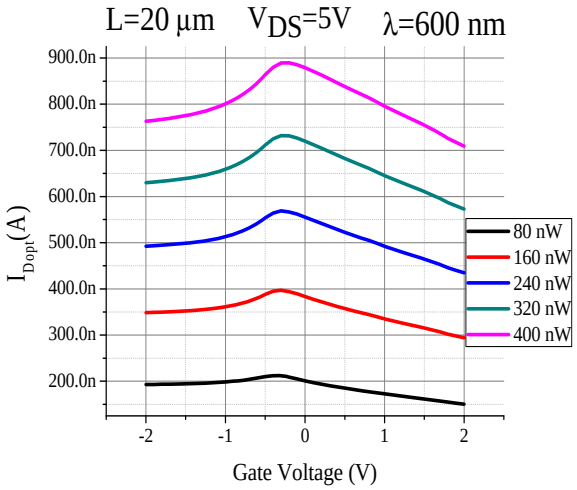

Fig. 5. Optical drain current as a gate voltage function. L is 20 µm. λ is 600 nm and drain voltage is 5 V.

Finally, Fig. 6 shows the optical drain current for different gate voltages and different light power for the transistor with L=10 µm.

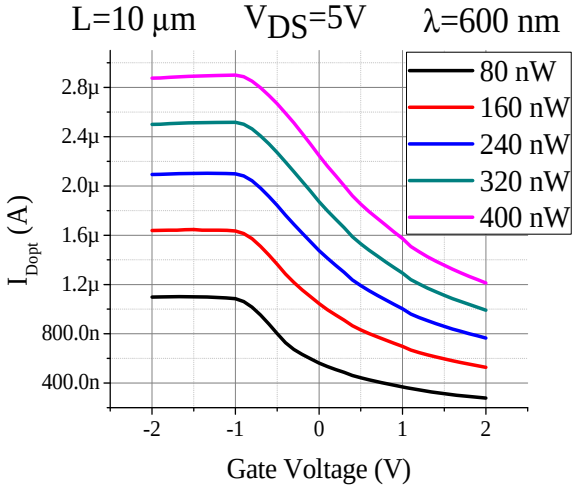

Fig. 6. Optical drain current as a gate voltage function. L is 10 µm. λ is 600 nm and drain voltage is 5 V.

Here, it can also be observer an optical drain current increment for higher light power values, with larger changes in I_{Dopt} for values of V_{gs} < -1 V, value after which a saturation behavior is observed. For V_{gs}=-2 V, the optical drain current varied from 1.1 µA to 2.8 µA when the light power is varied from 80 nW to 400 nW. This particular case could be the better if the lowest posible dark current and major photodetection is desired.

4. Analysis and Discussion

When the light is absorbed in the silicon substrate, each absorbed photon could produce an electron-hole pair which under proper conditions can contribute to the generation of an excess current, called photocurrent. This current is maximum when each photon incident produces an electron-hole pair that contribute to the photocurrent, i.e., they do not recombine. The maximum available photocurrent provided by the light emitter I_{ph} is a measure of the incident photons expressed as a current and is defined as [20]:

$$I_{ph} = q\frac{P_{in}\lambda}{hc}, \qquad (2)$$

where q is the electron charge, h is the Planck Constant and c is the speed of light. For P_{in} = 80 nW and λ = 600 nm, I_{ph} is 38.68 nA. This is the value of photogenerated current in ideal conditions (solely due to the incidence of photons and further generation of electron-hole pairs). If we compare this value with the simulated I_{Dopt}, it is possible to have an idea of the proportion of incident photons contributing to the generation of a detectable current. Fig. 7 shows the optical drain current for the different transistors and the ideal photocurrent I_{ph} for 80 nW light power.

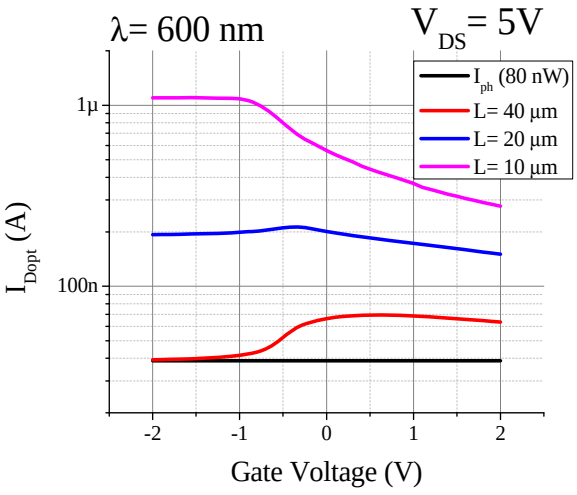

Fig. 7. Optical drain current as a gate voltage function. P_{in} is 80 nW, L is 40 µm. λ is 600 nm and drain voltage is 5 V. I_{Dopt} is above I_{ph}.

The photo generated drain current is greater than the I_{ph} value and is increased when the channel length is decreased. This means the detection of a current whose value is higher than the maximum available from photo-generated electron-hole pairs, i. e., the existence of an optical photocurrent gain. To better analyze this, a photocurrent ratio between optical drain current I_{Dopt} and the ideal photocurrent I_{ph} can be calculated and expressed as:

$$G_{opt} = \frac{I_{Dopt}}{I_{ph}} \quad (3)$$

Fig. 8 shows this photocurrent ratio G_{opt} for the different transistors with different length channel under light illumination with 80 nW.

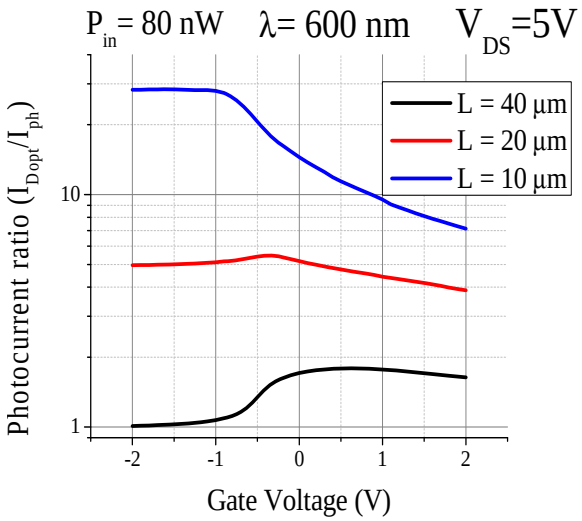

Fig. 8. Photocurrent ratio for the different MIS transistor with integrated waveguide. λ is 600 nm and drain voltage is 5 V. Light power is 80 nW.

The photocurrent ratio is greater than one and increases as the channel length is decreased. Note that transistors with channel lengths L = 20 µm and L=10 µm have lower dark current values and their photocurrent ratio is several times larger than one on the sub threshold or depletion regimes, meaning these are better behaved in such regimes.

Fig. 9 shows the photocurrent ratio as a channel length function and the gate voltage as a parameter.

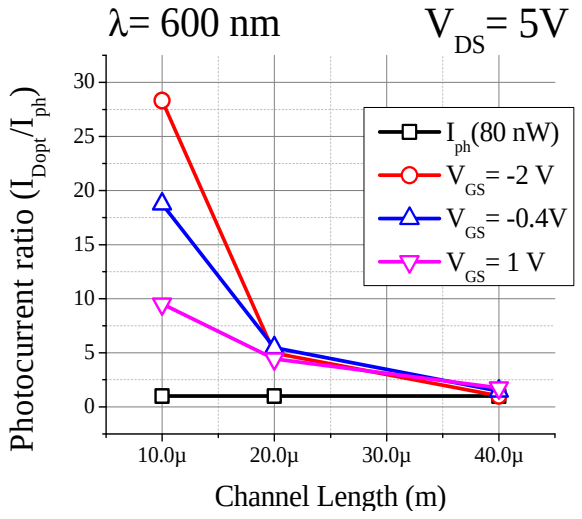

Fig. 9. Photocurrent ratio vs channel length. Gate voltage as a parameter. λ is 600 nm and drain voltage is 5 V.

The photocurrent ratio clearly depends on the gate voltage value. The ratio G_{opt} increases from 2 to 5 when the channel length is decreased from 40 µm to 20 µm and increases from 5 to 20 approximately when channel is decreased from 20 µm to 10 µm. In this study, the photocurrent ratio presents its higher value for 10 µm channel length and -2 V gate voltage.

Fig. 10 shows the electric field profile for the MIS transistor for L = 10 µm. The gate voltage is -2 V and drain voltage is 5 V.

The surface channel is not built it due to hole accumulation for the negative gate bias. However, the drain and source depletion regions are overlapped under the channel region due to the drain voltage. This condition reduces the physical distance between drain and source regions.

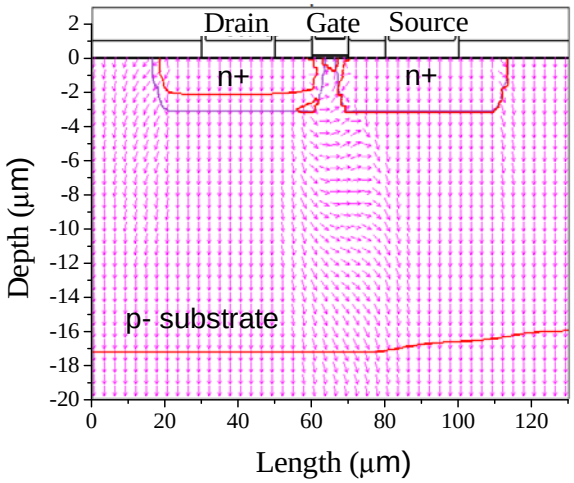

Fig. 10. Electric field directions in the MIS transistor. L is 10 µm. λ is 600 nm, drain voltage is 5 V and gate voltage is -2 V.

The depletion width is 17 µm due to low substrate concentration (1×10^{12} cm^{-3}), which is suitable for light detection in visible spectrum [21–24]. The drain-substrate contact region can be regarded as a pn junction reversely biased. If a photo generation process is carried out in the substrate depletion region, the electron-hole pairs are separated by the electric field. Electrons drift to drain and holes towards substrate. In addition, the hole excess in the absorption region decreases the potential or barrier height between drain and source. This allows for electrons to diffuse from source to drain through the substrate and an excess drain current is established. A decrease in the channel could be reducing the recombination and the number of electrons that reach the drain could be increase. This could explain the larger photocurrent ratio or amplification.

Fig. 11 shows the current density for the MIS transistor under illumination.

For λ = 600 nm the penetration depth is approximately 2.4 µm [22]. The current trajectory coincides with this depth value. This shows that an

important part of the current excess due the light photo generation can be produced in the substrate.

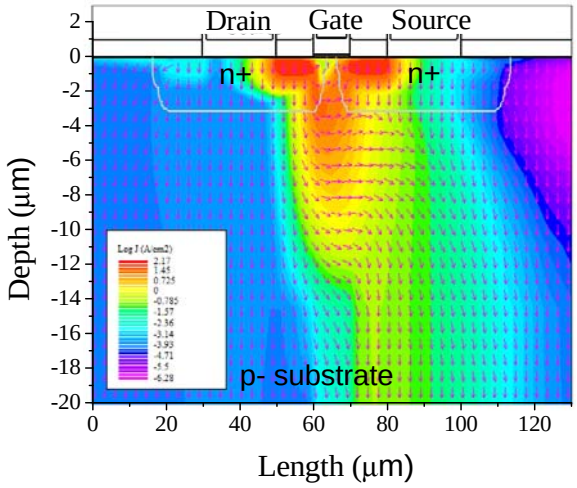

Fig. 11. Current density for the MIS transistor with 10 μm channel length. λ is 600 nm, gate voltage is -2 V and drain voltage is 5 V.

The total current in the transistor could be expressed as:

$$I_{Dtotal} = I_{Ddark} + G_{opt} I_{ph} \quad (4)$$

The I_{Ddark} is controlled by gate bias and the I_{Dopt} is a substrate contribution due the optical generation. The simplest model relates the I_{Dopt} to the photon current I_{ph} I_{Dopt} is composed by a photocurrent generated in the drain-substrate junction plus a drain-source diffusion current that is composed by photo generated excess carriers on the substrate region.

5. Conclusions

A MIS transistor with an integrated nitride waveguide was studied through computer simulation. The structure was obtained by fabrication process simulation using materials and process steps compatible with the standard CMOS fabrication technology. The transistor was biased with different gate voltages and was illuminated directly from the gate considering a uniform visible light beam with 600 nm wavelength and power varying from 0 nW to 400 nW. The results show that the drain current increases as the light intensity increases. Drain currents under dark condition have the typical MOS like behavior. However, the threshold voltages have negative values and the transistors operate in depletion mode. The dark current is increased when the channel length is decreased. Light detection is observed in all the range of gate voltages studied. A photocurrent ratio of optical drain current to ideal photon current larger than one was found, meaning that an optical detection gain is observed. This is dependent on the gate length, showing larger gains for shorter lengths. The best results were observed for a transistor with 1×10^{12} cm^{-3} substrate concentration and 10 μm channel length, in which a gain photocurrent ratio up to 30 was observed. Such gain was explained by the substrate current that exists when the incident photons produce a carrier excess within depletion region in which an electric field exists due to the reverse bias of the substrate to drain junction. This allows for the electrons to diffused from the source to the drain and an additional drain current component can be built. This means that the device can be used to improve the detection of light intensities in the nW range for visible wavelengths in electrophotonic systems fabricated in silicon technologies using CMOS compatible process

Acknowledgements

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