Implementation and Design of Digital System for High Frequency RFID Tag Chip

Wenwen Zhang, * Weiping Jing, Bin Jiang

Nantong University, No. 9 Seyuan Road, Nantong City, Jiang Su Province, 226019, China
* Tel.: +86-513-85012701, fax: +86-513-85012701
* E-mail: jing.wp@ntu.edu.cn

Abstract: Passive RFID tag system requires low-power consumption. In this paper, the clock shutdown technology was been used to reduce power consumption and the module re-used was been used to reduce chip area. The design was been described for the digital part of RFID tag chip based on ISO/IEC15693 standard, that was including decoder, encoder, CRC generation and verification, EEPROM interface block ,the master state machine and clock management block. The detailed design scheme about the master control block, Conflict part and coding block was been given. The unique coding was been used and state machine design scheme was been used in all blocks, which would not only simplify the design, but make the design more flexible. And EEPROM RTL model was been built-in for test validation. Finally, the results were verified correctly in the specified clock frequency in device in DE2-115FPGA Altera kit using Verilog in RTL level. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: RFID, ISO/IEC15693, RTL, Low-power design, FPGA, Tag.

1. Introduction

Radio frequency identification (RFID) uses radio waves to exchange data between a reader and electronic tags attached on objects [1]. There are two kinds of RFID tag: active tag and passive tag. RFID tag chip based on ISO/IEC15693 [2] standard is passive tag. Passive RFID tag system requires low-power consumption in order to increase recognition distance. There were ISO/IEC14443 [3] and ISO/IEC15693 standards, that main frequency is 13. 56 MHz. ISO/IEC 14443 is a standard operating in proximity, with communicating distance of less than 10 cm. ISO/IEC 15693 is a standard for vicinity cards, with operating range of up to 1.5 m. ISO/IEC 18000-3 is a new standard for item management. The physical layer of the air interface for ISO/IEC 18000-3 [4] Mode 1 is compatible with ISO/IEC 15693 [5]. RFID tag chip applications of ISO/IEC 14443 standard was limited to members of management,

staff attendance, shopping card, card and other label cards. RFID tag chip applications of ISO/IEC 15693 standard was been widely used, can be used to open access, open meeting attendance, valuables management, digital library book management, medical management, asset management, product security, logistics and supply chain fields, etc. It is waterproof get from [6], which can be applied to the special environment such as aquatic management.

There are many publications about the design of an RFID tag chip. In [7], the design of a novel circuit is presented, which was been design for a UHF-RFID tag in compliance with the ISO 18000-6B protocol. In [8], the design of the RF transceiver and digital control of the tag IC is based on the International Organization for Standardization-14443 type-B protocol. In [9], the frequency of operation for different RFID applications changes depending on the constraints associated with the application, some of the blocks of the RFID tag can be designed, which

works for multi-standard RFID frequencies such as 13.56 MHz, 915 MHz and 2.45 GHz. But there are almost no technical papers regarding the design of ISO/IEC 15693-compatible RFID tag chip.

Communications between the interrogator and the transponder IC takes place using the modulation principle of ASK in the ISO/IEC 15693. Two modulation indexes are used: 10 % and 100 %. Data coding is possible using 1 out of 4 or 1 out of 256 data coding mode which leads to a downlink rate up to 26.48 kbps. The transponder uses load modulation to send its response. Depending on the mode, uplink rates of up to 26.69 kbps are achievable. The configuration is done via the application protocol.

The rest of the paper is organized as follows. Digital part of VICC is covered in the immediate section. The detailed design scheme about decoder, encoder and the master state machine was described in section 3, the system function simulation and FPGA verification are discussed in section 4. Finally the paper is concluded.

2. Digital Part of Vicinity Integrated Circuit Card

The main task of digital part is to deal with the vicinity coupling device (VCD) request and give the appropriate response, which is a core part of VICC, controlling the work of the entire chip. In addition, it connected to the analog front end and EEPROM memory, which is the most important part of the chip. The block diagram of Digital part is given in Fig. 1. That is including decoder, encoder, CRC generation and verification, EEPROM interface block, the master state machine and clock management block.

The management process of digital part which is as follows.

1) Clock management block would do clock frequency division to provide the clock for other piece when the VICC power on.

2) Decoder would decode the data which analog front end received the VCD request and then give to the CRC check block and main control block.

3) When CRC check was completed, it would feedback the results to the master control block.

4) Master control block was corresponding to requests such as conflict prevention, read and write EEPROM block, which would return data to CRC generation block and encoder after processing had completed.

5) CRC generation block would get the CRC codes to the encoder. And the encoder would response to output analog front end for VCD.

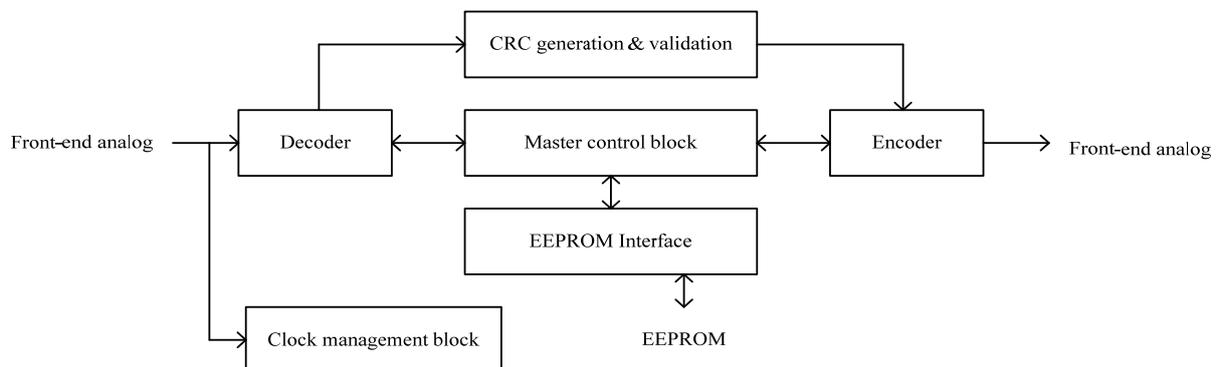The idea on implementation of each block is as follows.

Fig. 1. Block diagram of Digital part.

2.1. Decoder

The demodulated signal from the front-end analog is decoded according to ISO15693 standard. Communications between the VCD and the VICC takes place using the modulation principle of ASK. Two modulation indexes are used, 10 % and 100 %. The VICC shall decode both. The VCD determines which index is used. The two cases unified data format protocol mentioned can be met, and ultimately ensure completely accurate decoding. And two data coding modes shall be supported by the VICC, these are 1 out of 256 and 1 out of 4 pulse position modulation. Frames shall be delimited by a start of frame (SOF) and an end of frame (EOF) and are implemented using code violation. By counting the width between adjacent pulses to get the decoding data.

2.2. Master Control Block

Its main task is coordinating the work of each module, processing the request from VCD including collision block operation, state transitions, read, write or lock EEPROM, etc. When decoding block received SOF, suggests a data request from VCD, after the CRC check correctly, the main state machine begin to work. The first thing is to check each flags and the request of command, and then to manage the operation. Finally, return data to VCD from coding block.

2.3. CRC Generation and Validation

CRC block has two tasks under the scheduling of main control block. One is processing CRC check, another is generating CRC codes for return data. The initial register content shall be all ones: 'FFFF'. The residue is 'F0B8'. Upon reception of a response from the VICC, it is recommended that the VCD verify that the CRC value is valid. If it is valid, actions to be performed are left to the responsibility of the VCD designer. If it is invalid, it shall discard the frame and shall not answer. CRC check work is to verify VICC receives the request is correct or incorrect. At the same time, CRC generation block the response returned with 16 bits of CRC. So we can put the two pieces up for reuse, reduce the area.

2.4. EEPROM Interface Block

EEPROM interface block is the connection bridge of the EEPROM memory and Digital part. Digital part read, write or lock EEPROM memory through it control operation and transport address or data. The State diagram of EEPROM interface block is given in Fig. 2.
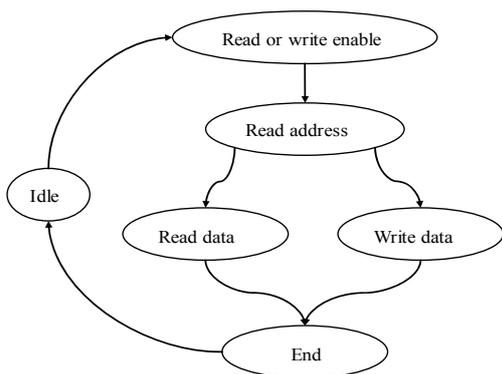

Fig. 2. State diagram of EEPROM interface block.

2.5. Encoder

Return data encode according to Manchester code. Data rate of return data decide by the request data format. Its lowest level would decide a single carrier or double carrier format, low decide the high rate transmission or low rate. The whole data start with SOF, after combined with 16 bits of CRC and EOF. Encoding must be complete to ensure the VCD can be accurately identified.

2.6. Clock Management Block

The gating clock has the strongest inhibitory effect to turn on the power consumption and internal power dissipation in low power technology. In order to get the lowest power consumption, the design adopts the gating clock to manage the clock of each block with the clock management block.

The clock of each block is opening in need, and every time you feel you don't need to turn off, that can reduce power consumption. For example, decoding block is working, the clock of encoding block can be turned off.

3. The Management Processing of VICC

By ISO/IEC15693 of part 3, the VICC belong to passive chip, after receive the request from VCD, through the digital part of the process to make the appropriate response. The whole working process of VICC can be divided into three steps: receiving, processing, responding. Of all the blocks used low power consumption state machine design method. Using 2 always style writing program, which would not produce burr noise, improving the design [6].

3.1. The Processing of Main State Machine

State diagram of main control block was been shown in Fig. 3.

1) VICC was in the state of Power on once in Field. Its state is idle in fact. When it found a pulse, it starts to work. The processing turn to (2).

2) Receives the front end of the decoding module of bytes, the front end of 8 bits of data stored in a temporary register, according to the ISO/IEC 15693, the first byte is Flag. It determines the following several aspects of information, and decides the operation later. These messages are respectively: back in the data model and rate, the way of addressing, the format of the command.

3) Parameters of the receiving, storage into the Buffer as a Buffer, waiting to read, whenever they are needed.

4) If it is a way of addressing, block by EEPROM control module read the UID and instructions given comparing the UID.

5) According to different commands to choose different way of jump, the second byte is the request. According to the command code into the next state, a total of four kinds of circumstances are respectively the Inventory (conflict prevention operation) to (6); Change VICC state to (10); Read to (8); Write to (9).

6) If it is using 1 slot collision algorithm, according to MASK the LENTH and MASK the UID VALUE controls the tag itself, and comparison operations.

7) If it is using 16 slots collision algorithm, the specific algorithm as shown in the description of the agreement. For collision operation, the selected label will turn to step (10), otherwise go to step (6).

8) Perform a Read operation, Read the UID, Read block, Read security status. Read operation is completed to (10).

9) Write operation, Check the lock bit, Write block, Write security status. Write operation is completed to (10).

10) Return data to the reader a sign of the data content and related code. Returns the relevant

parameters according to the requirements of agreement: the error code, UID, DSFID and so on. Return to (1) end.

3.2. Conflict Part

VICC use time slot anti-collision algorithm, it is including the one slot and 16 slots. By comparing the request part of the UID value to judge whether it is the selected card. If the selected card was using one slot, that would direct response. If 16 slots was been used, that through the corresponding high four UID values to determine the response slot. VICC anti-collision process is shown in Fig. 4.
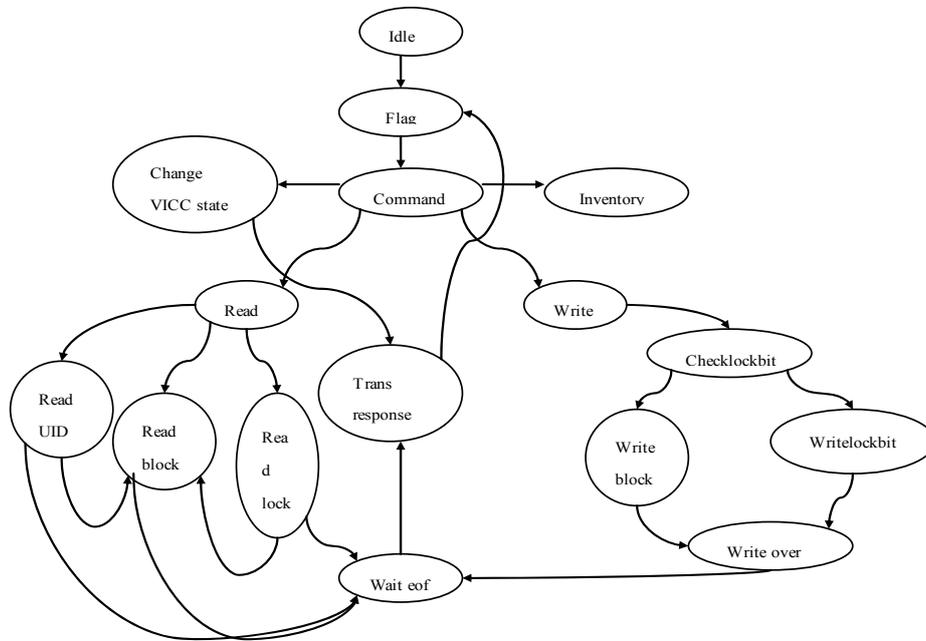
Fig. 3. State diagram of Master control block.
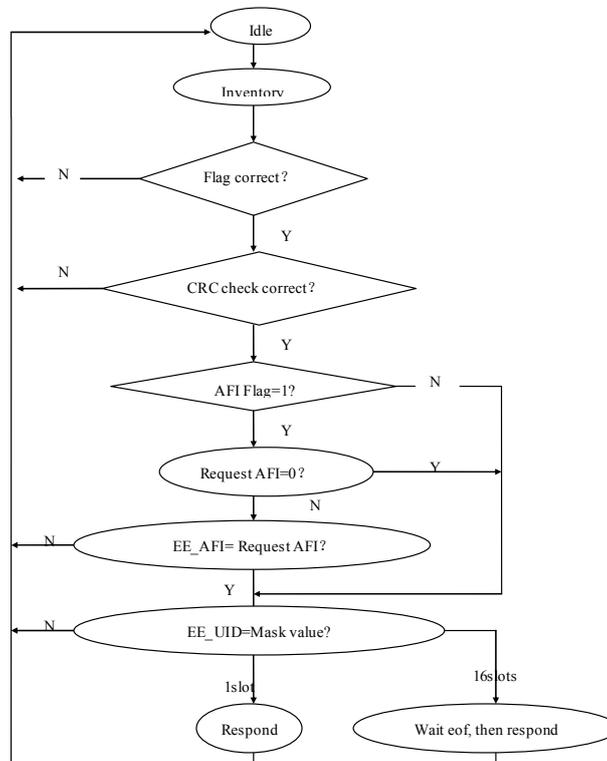
Fig. 4. State diagram of Inventory.

3.3. Coding Block

Data from analog front end would be process before decoding, which was been shown in Fig. 5.
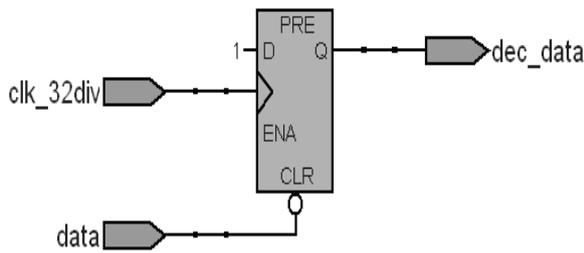
Fig. 5. Circuit of Data process before decoding.

It made count1 register add one as the time of 9.44 us in decoder. It got decoding data by identifying the distance of adjacent grooves. The decoding process state diagram was been shown in Fig. 6.

Pipeline operation was been used in encoder to reduce the use of registers and also do not need to cache, greatly reduced the power consumption of the encoder and usable floor area. The encoding process state diagram was been shown in Fig. 7. In this part Protocol extensions was been used double rate as high as 53 kbps.
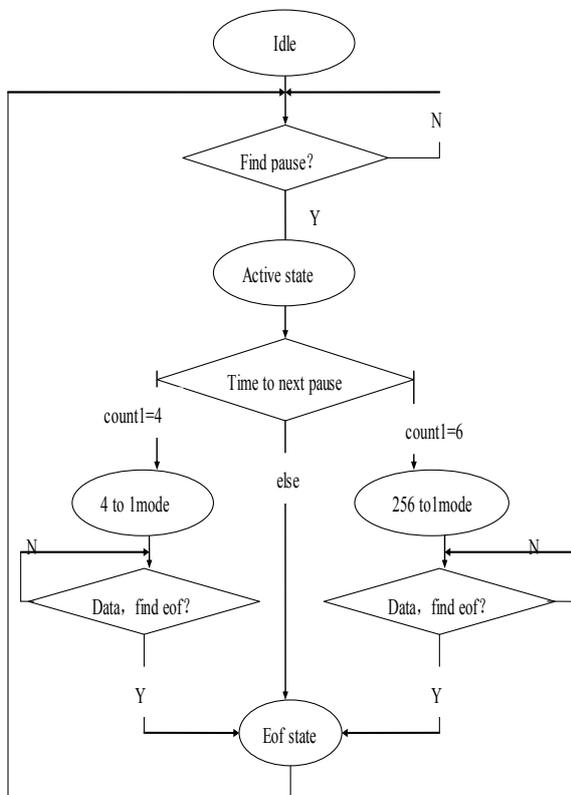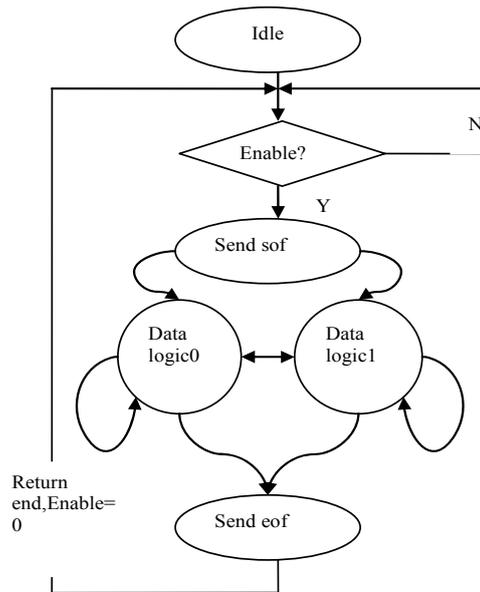

Fig. 6. State diagram of Decode.

Fig. 7. State diagram of Encoder.

4. Simulation and Verification

4.1. The System Function Simulation

Digital system as the core of the RFID chip control unit is the brain of the chip. The stand or fall of the design of digital part was concerning to the success of the whole chip. Its validation work is very important. Digital system according to the way of top-down design, validation will be synchronized with the design.

Using the Modelsim simulation to get the waveform as been shown in Fig. 8.

In Fig. 8 "r_RF_CLK" is the input system clock, the frequency is 13.56 MHz; "R_RF_POR" is a system reset signal, VICC just coming into the field to conduct a reset, reset for digital part of all the register; "W_RF_DO" is the carrier signal, has been through the analog front end of demodulation, here is 4 in 1 pulse modulation (PPM) signal; "W_RF_DIN" is to return the response signal, and USES a Manchester encoding; "W_RF_DEMENB" output enable signal, can make it as a high levels; Below 12 signal from top to bottom in order to receive data as a sign of 256 to1, (PPM), receiving data as a sign of 4 to1, the end of the receiving data frames, the number of bytes of data received, the received data decoding according to hexadecimal display, a sign of CRC verification (on behalf of CRC validation errors at ordinary times, high electricity VICC response) will not block, EEPROM model ('0' is not operation, '1' is read, '2' is written) block, EEPROM enabling signal block (high electricity at ordinary times, EEPROM work), block the EEPROM block address of operation, the end of the block to the EEPROM read operation can make, response data model ('10' refers to the response returned format for high speed single carrier), response data (not including CRC).
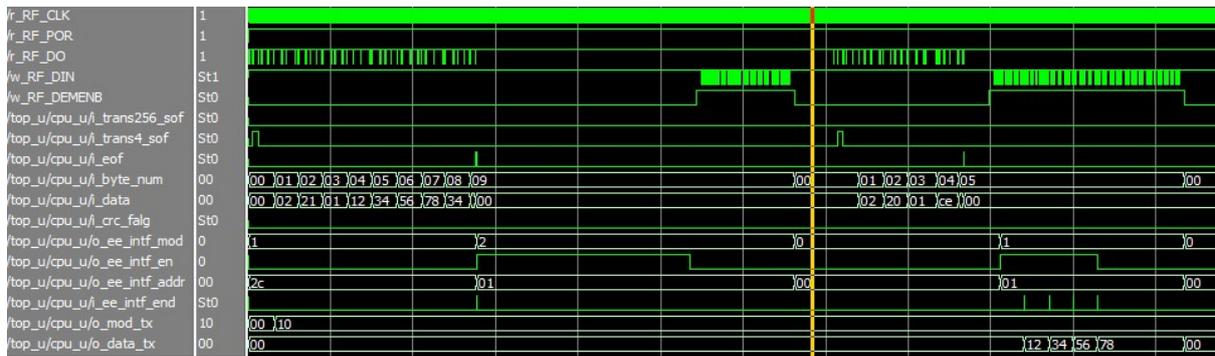
Fig. 8. Simulated Waveform of reading and writing.

It can see that send data from the waveform figure was "02,21,01,12,34,56,78,34,56" "02,20,01, ce, 41"; Its function is to write "12345678"into 01 block. Then read 01 block, read block value is "12345678".The function of the block that read and write EEPROM verify correct.

4.2. FPGA Verification

FPGA verification greatly reduces the ASIC design "one design success - First - Time " pressure, which in turn promoted the chip and system level validation of rapid, efficient and cost-effective.

RTL level behavior model, and can be integrated block of EEPROM model transplanted into Altrea DE2-115 development board, with rf front end connections, card reader, verifies the actual operation. FPGA validation test platform was been shown in Fig. 9.

The chip supply voltage by 3.3 V. Waveform of FPGA verification and PC display of FPGA verification about Inventory was been shown in Figs. 10 and 11.

Fig. 9. FPGA validation test platform.

Fig. 10. Waveform of FPGA verification about Inventory.
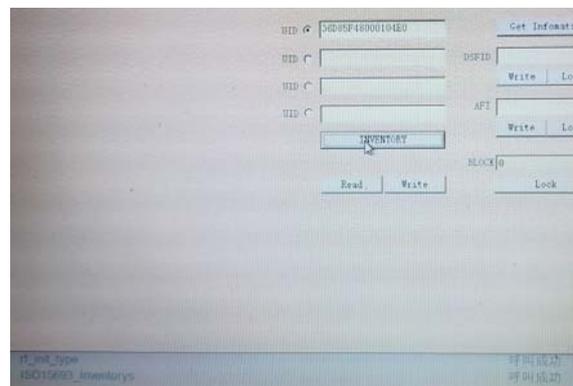

Fig. 11. PC display of FPGA verification about Inventory.

The EEPROM block in the initialization of the UID for "e0040100485fd836", in the upper machine data after decoding for "16010000392", you can know the command code "01" that is, the inventory command requests; Mask length = 0, so the conflict directly through, at slot6 return data, can be seen from the figure 10 in accordance with the above analysis. Can be seen from the figure 11 perform "inventory", after the UID is shown as "36 d85f48000104e0" consistent with our initialization value is, and the system displays call success.

5. Conclusion

In the paper, VICC digital structure, RTL modeling, functional simulation and FPGA validation were designed based on the description of the ISO/IEC 15693. Using a unique way of coding made the design simpler. And state machine design scheme was been used in all blocks, which would make the design more flexible. VICC was adapt to prevent conflict, low power consumption design and the function fully in line with the ISO/IEC 15693 for adapt to the market demand. This design also allows field upgrade flexibility, in a market where standards and designs are still evolving.

Acknowledgement

References

[1]. James C. Chen, Po Tsang B. Huang, Chien-Jung Huang, Warehouse management with lean and RFID application: a case study, *Int. J. Adv. Manuf. Technol.*, Vol. 69, 2013, pp. 531– 542.

[2]. Identification cards-Contactless integrated circuit cards-Vicinity cards, ISO/IEC, 2006.

[3]. Identification cards -Contactless integrated circuit (s) cards -Proximitycards, ISO/IEC, 2001.

[4]. Information technology- Radio frequency identification for item management - Part 3: Parameters for air interface communications at 13.56 MHz, ISO/IEC, 2004.

[5]. Liu Dong-Sheng, Zou Xue-Cheng, Yang Qiu-Ping, Xiong Ting-Wen, An analog front-end circuit for ISO/IEC 15693-compatibleRFID transponder IC, *Journal of Zhejiang University,* Vol. 7, Issue 10, 2006, pp. 1765-1771.

[6]. Talleb Hakeim, Faci, Salim Lautru, David, Investigation on an RFID planar coil for a wireless communicative aortic stent, *Comptes Rendus Physique,* Vol. 14, 2013, pp. 438-436.

[7]. Andrea Ricci, Matteo Grisanti, Ilaria De Munari, Paolo Ciampolini, Improved Pervasive Sensing With RFID, An Ultra-Low Power Baseband Processor for UHF Tags, *Transaction on Very Large Scale Integration (VLSI) System*, Vol. 17, Issue 12, 2009, pp. 1719-1729.

[8]. Jong-Wook Lee, Senior Duong Huynh Thai Vo, Quoc-Hung Huynh, Sang Hoon Hong, A Fully Integrated HF-Band Passive RFID Tag IC Using 0.18-μm CMOS Technology for Low-Cost Security Applications, *Transaction on Industrial Electronics,* Vol. 58, Issue 6, 2011, pp. 2531-2540.

[9]. M. Kothamasu and Roy Paily, Power Feeding and Digital Block design of Multi-standard passive RFID tag, in *Proceedings of the IEEE 1st Asian Himalayas International Conference on Internet (AH-ICI'09)*, 2009, pp. 1565-1570.